Sb/Te Ratio Engineering in Phase-Change Memory for High SET Speed and Large Memory Window

R. Antonelli[1,2], O. Daoudi[1], G. Bourgeois[1], A. Salvi[1], S. Gout[1], M. Bernard[1], L. Fellouh[1] J. Rottner[1], N. Castellani[1]
N. Bernier[1], Z. Saghi[1], A. Jannaud[1], F. Fillot[1], E. Nolot[1], F. Andrieu[1], A. Souifi[2], G. Navarro[1]
[1]*CEA, Leti, Univ. Grenoble Alpes 38000, Grenoble, France*
[2]*Univ. Grenoble Alpes, CNRS, LTM 38054, Grenoble, France*

***Abstract*—The article investigates the effects of Sb/Te ratio on the crystallization kinetics, programming characteristics, SET speed and endurance in GeSbTe-based Phase-Change Memory (PCM). We compare PCM devices with critical dimension down to 40 nm integrating three different compositions with increasing Sb/Te ratio: $Ge_1Sb_2Te_4$, $Ge_1Sb_4Te_4$ and $Ge_1Sb_9Te_4$. Sb increase allows to improve the reliability of SET operation, however a too high Sb/Te ratio reduces the RESET state resistance affecting the final PCM memory window. Intermediate Sb/Te ratio of $Ge_1Sb_4Te_4$ provides the best trade-off between the high SET speed of $Ge_1Sb_9Te_4$ and the large memory window of $Ge_1Sb_2Te_4$. Sb/Te ratio engineering is a key knob to improve the SET operation reliability and enhance the memory window in PCM devices.**

***Index Terms*—Phase-Change Memory, NVM, Sb/Te ratio, GeSbTe, High SET speed, Large Memory Window.**

I. Introduction

Phase-Change Memory (PCM) is a well established memory technology, proposed as a candidate for DRAM/SRAM or Flash replacement in several applications [1]. PCM offers low latency and a large resistance window, making it suitable for a wide range of applications, including Storage Class Memory (SCM) [2]. It demonstrated high maturity for embedded applications, ensuring the more strict automotive reliability specifications in advanced technology nodes [3]. PCM exploits the reversible phase transition between a highly resistive amorphous phase (RESET state) and a low resisitve crystalline phase (SET state), achieved through Joule heating by the application of a suitable programming pulse [4]. The quest for the PCM cell shrinking demonstrated the possibility to preserve the phase-change mechanism down to the nm scale [5] with an impact, however, on the crystallization kinetic and on the SET programming speed [6, 7].

Previous studies have highlighted the role of antimony addition in $Ge_2Sb_2Te_5$, enabling extremely fast SET speed due to the enhanced crystallite growth rates facilitated by the abundance of Sb-Te bonds [8, 9]. The Sb in excess can be responsible for partially filling the available structural vacancies of the stoichiometric $Ge_2Sb_2Te_5$ suppressing the metastable cubic phase and leading to a direct transition from amorphous to trigonal (or hex) crystalline phase [10]. Previous works focused mainly on Sb enrichment into stoichiometric alloys not specifically obtaining congruent compositions. In this study, we propose the investigation of congruent alloys laying on the pseudo-binary tie line connecting $Ge_1Sb_2Te_4$ and Sb (**Fig. 1a**) exploring the effects of the progressive Sb/Te ratio increase. We compare three finely tuned GeSbTe (GST) alloys: $Ge_1Sb_2Te_4$ (GST124), $Ge_1Sb_4Te_4$ (GST144), and $Ge_1Sb_9Te_4$ (GST194), with increasing Sb/Te ratio from 0.5 up to 2.25. Resistivity as a function of temperature (RvsT) measurements and Activation Energy (E_a) of the crystallization extraction, reveal a progressive increase of the stability of the alloys against nucleation with increasing Sb/Te ratio. X-ray diffraction (XRD) analyses combined with transmission electron microscopy (TEM) confirm the absence of segregation and the congruent nature of the explored compositions, highlighting a fast growth-dominated crystallization in high Sb/Te ratio alloys. Once integrated in "Wall" PCM devices (**Fig. 1b**), the increased Sb/Te ratio allows a more reliable and fast SET operation despite the decrease of the memory window (MW). For the first time at our knowledge, we could integrate GST144 alloy featuring a high SET programming speed typical of Sb-rich compositions (e.g. GST194), thanks to the suppression of cubic metastable phase, and a large MW typical

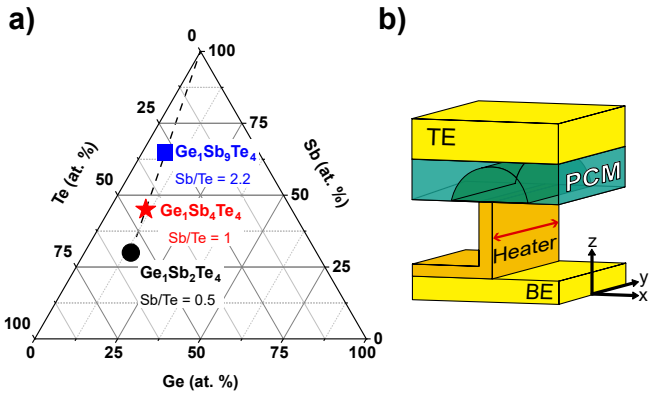

Fig. 1. a) GST ternary diagram highlighting the studied compositions along the GST124-Sb tie line. b) Simplified scheme of the "Wall" PCM device showing the top electrode (TE), PCM material, heater electrode and the bottom electrode (BE). The device critical dimension (CD) along the *y*-axis is evidenced by the red arrow. The considered nominal CDs for our tests were 40 nm and 100 nm.

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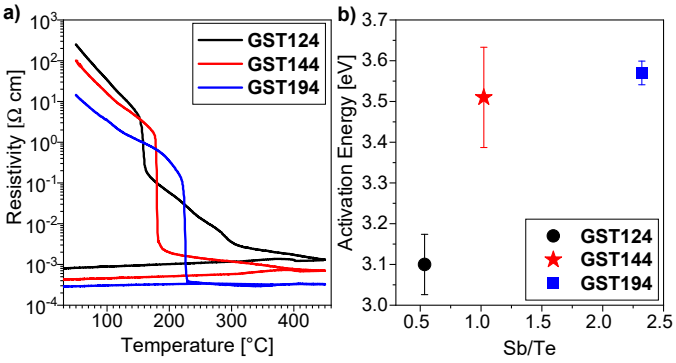
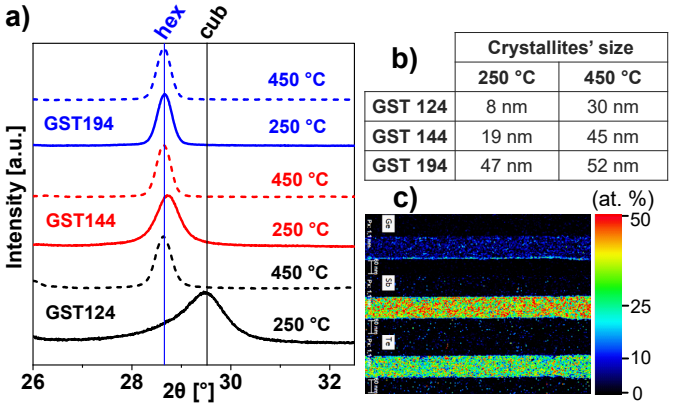


Fig. 2. a) RvsT measurements for GST as-deposited amorphous thin films. GST144 and GST194 crystallize directly into a stable hex phase, while GST124 shows the intermediate transition through a cubic phase. b) Evolution of the Activation Energy of the crystallization as a function of the Sb/Te ratio, extracted by Kissinger analysis.



	Crystallites' size	
	250 °C	450 °C
GST 124	8 nm	30 nm
GST 144	19 nm	45 nm
GST 194	47 nm	52 nm

Fig. 3. a) XRD patterns obtained after annealing at 250 °C and 450 °C. b) Crystallites' size extracted with the Scherrer equation after annealing at 250 °C and 450 °C. c) Energy-Dispersive X-ray spectroscopy (EDX) performed on GST144 after annealing at 450 °C, showing the uniformity of the layer and no elemental segregation.

of standard low Sb/Te ratio compositions (e.g. GST124). Therefore, we show how Sb/Te tuning in GST alloys represents a key knob for performance optimization in Phase-Change Memory.

II. Material Analysis

GST films deposition was performed by co-sputtering from GST124 and Sb targets. **Fig. 2a** illustrates the sheet resistance of GST thin films as a function of temperature (RvsT) at a fixed heating rate of 10 °C/min. The crystallization temperature of the GST thin films increases with the Sb content. GST124 (Sb/Te = 0.5) first crystallizes into a metastable cubic phase at 157 °C, transitioning to a stable hex phase at 290 °C. On the contrary, GST144 and GST194 (Sb/Te $\geq$ 1) crystallize directly into a low resistive hex phase. After crystallization, GST144 still show an evolution towards an even lower resistance (i.e. crystalline growth), while GST194 remains stable. Using Kissinger analysis [11], we extracted the Activation Energy of crystallization (E_a) for the first crystalline transition. **Fig. 2b** shows that E_a increases with the Sb/Te ratio. Indeed, samples with Sb/Te $\geq$ 1 require

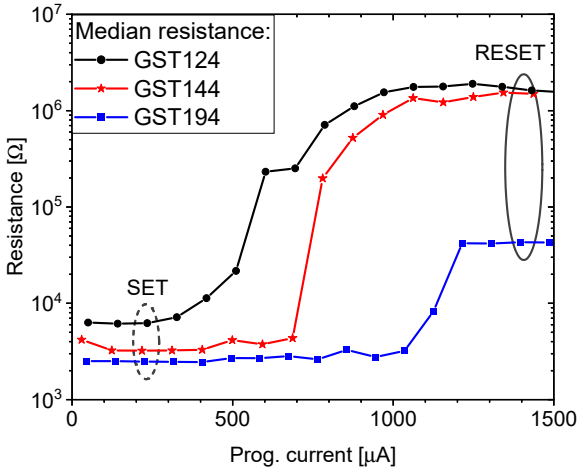


Fig. 4. Resistance as a function of I_{prog}, showing the transition from SET to RESET states for the three compositions. Median extracted from about 100 devices with a nominal CD of 40 nm.

a higher energy for nucleation, as the phase change is not mediated by the cubic phase, as observed in GST124. To confirm the nature of the crystalline phase, we performed XRD measurements on samples annealed respectively at 250 °C and 450 °C. GST124 annealed at 250 °C exhibits a cubic (cub) phase, while samples with increased Sb/Te ratio show only the Bragg peaks corresponding to a hex phase (**Fig. 3a**), consistent with previous results [12, 13]. After the annealing at 450 °C, only the hex phase peak is present in GST124 with a complete suppression of the cubic phase. GST144 exhibits an improved crystallinity, while GST194 remains unchanged upon annealing, validating the fast growth-dominated crystallization kinetic as observed in RvsT measurements (Fig. 2a) [14]. Using the Scherrer equation, we determined the grain size for the three studied samples (**Fig. 3b**). The crystallites' size increases with the Sb/Te ratio, with GST144 showing an intermediate behavior between GST124 and GST194. The properties of GST144 are very interesting for PCM applications, since it preserves a high resistivity contrast between the amorphous and crystalline phases while ensuring fast growth-dominated crystallization towards a stable hex phase. TEM-EDX analysis of GST144 annealed at 450 °C (**Fig. 3c**) shows a homogeneous phase with no elemental segregation.

III. PCM Electrical Performance

We integrated the three GST alloys in PCM heater-based devices fabricated in the BEOL of the LETI Memory Advanced Demonstrator (MAD) based on 130 nm CMOS technology, for both single device and 16 kb array statistical analysis. **Fig. 4** shows the programming characteristics for the three compositions. The programming current (I_{prog}) required to amorphize the material increases with Sb content. I_{prog} is similar between GST124 and GST144, but it exceeds 1 mA for GST194, likely due to the fast crystal growth speed which can overcome the melt-quench amorphization rate at lower currents [9]. Antimony promotes a more metallic conduction,

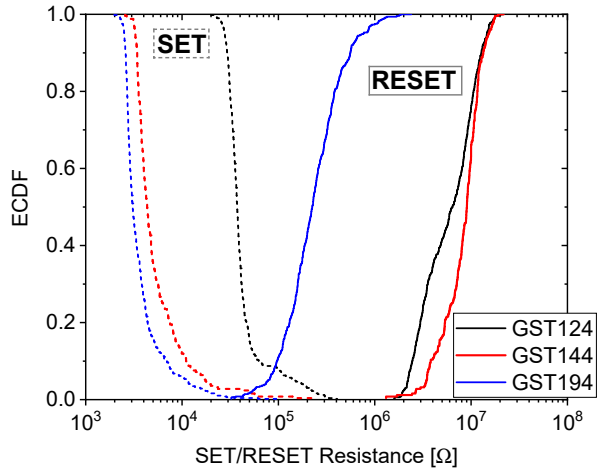


Fig. 5. Experimental cumulative density function (ECDF) for the SET (dashed line) and RESET (solid line) states. The increase in Sb content leads to a less resistive and more uniform SET state with a reduction of the MW in GST194 due to a more conductive amorphous phase. The distributions are obtained by more than 256 devices with a nominal CD of 40 nm.

leading to a much lower RESET resistance in GST194, losing nearly two orders of magnitude compared to GST124.

Fig. 5 reports the SET and RESET distributions for the three compositions. Both GST124 and GST144 exhibit a large MW, with a RESET/SET ratio of over 170 and 2000, respectively. In GST194, the lower RESET resistance limits the overall window. For high Sb/Te ratios, the SET resistance decreases and becomes less dispersed and in particular GST144 presents reduced SET tails with an additional enhancement of the MW.

We performed SET resistance cartographies to investigate the SET programming speed: varying I_{prog}, the programming pulse width (t_{width}), and the pulse fall time (t_{fall}), starting from the RESET state (**Fig. 6**). For Sb/Te $\geq$ 1, the SET operation results more reliable and fast ($t_{fall} < 5$ ns) already at low programming currents. On the contrary, GST124 requires higher programming current and a longer fall time to ensure the same programming reliability. The current-over-time decreasing rate (proportional to the material growth speed [7]) of GST144 to ensure an optimal SET operation, is extracted by linear fitting of the SET-to-RESET iso-resistance curve shown as a dotted line in Fig. 6a. It is approximately 1.7 µA/ns, higher than values previously reported for standard $Ge_2Sb_2Te_5$ (1.3 µA/ns) and Ge-rich GeSbTe (0.3 µA/ns) [7, 15] integrated in equivalent test vehicle for comparable device dimensions. This result is in line with the higher growth speed of GST144 observed by material analyses. The same extraction could not be reliably performed for GST124 due to the slower crystallization speed which limits the SET capability at low currents. The lateral confinement of the cell also limits the temperature gradient, therefore not promoting the propagation of the crystallites from the borders. In GST194, the crystallization speed is much faster making RESET operation possible only at high currents, as previously observed in programming characteristics (Fig. 4).

Endurance tests were performed by applying repeated SET and RESET writing pulses (t_{width} = 300 ns), following the

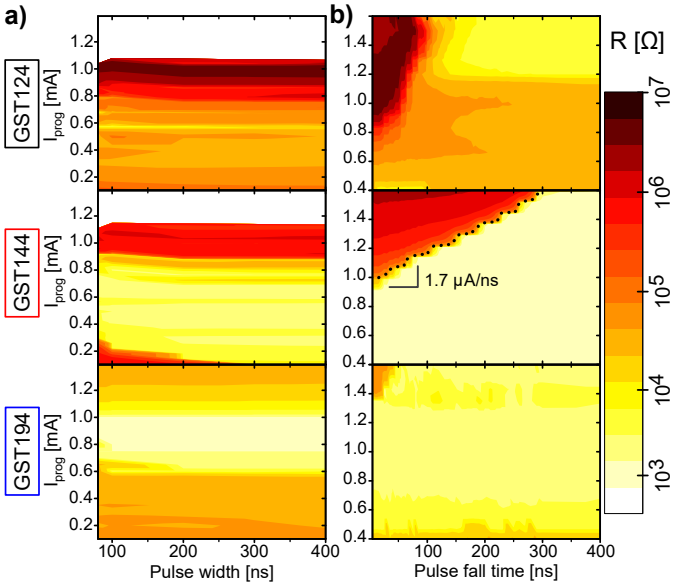


Fig. 6. SET resistance cartographies for increasing I_{prog} (y-axis) and for increasing a) t_{fall}, and b) t_{width} (x-axis). The mean SET resistance value is reported for each programming condition applied on a population from 100 to 256 devices. The devices were pre-programmed in the RESET state before each programming pulse. The dotted line represents the SET-to-RESET iso-resistive curve used for the current over time (dI/dt) decreasing rate extraction for optimal SET operation.

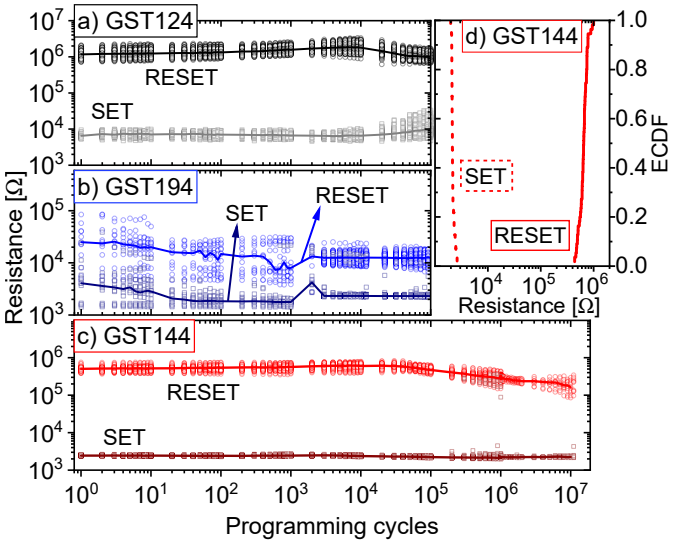


Fig. 7. Endurance tests for a) GST124, b) GST194, and c) GST144 performed on at least 10 devices for each composition. d) SET and RESET distributions (55 devices) for GST144 after 10^6 programming cycles.

evolution of the programmed resistance states. The max I_{prog} is equivalent for GST124 and GST144 devices in order to trigger the materials evolution for same programming conditions (i.e. programming energies), the GST194 required higher current to achieve a reliable RESET. GST124 is stable upon cycling, with both SET and RESET resistances evolving after 10^4 cycles (**Fig. 7a**). The devices remain functional and programmable even after 10^5 iterations. GST194 shows a higher starting resistance variability that reduces along cycling, likely related to elemental reorganization happening in the active region.

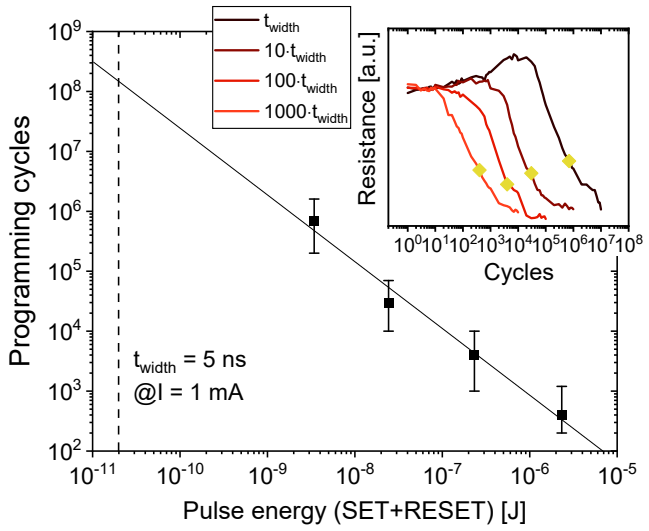


Fig. 8. Number of max SET/RESET cycles for a given programming energy (SET + RESET energy) before the starting of the resistance states evolution in GST144. The dashed vertical line represents the energy of a short 5 ns pulse (e.g. RESET). The inset reports the endurance result performed with increasing pulse width time (t_{width} = 300 ns). The yellow diamonds are the points of RESET halved resistance, used for the material stability estimation.

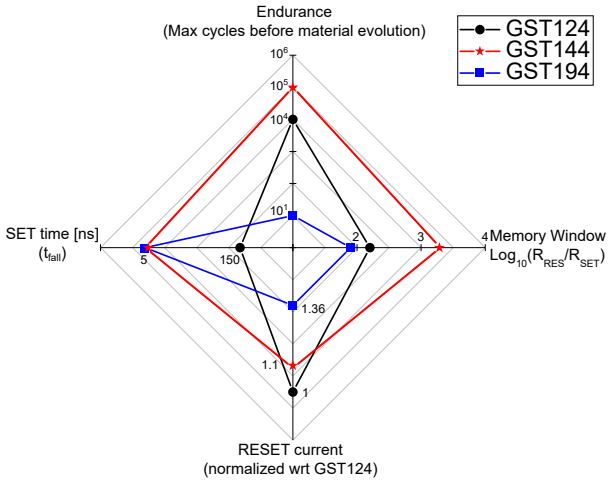


Fig. 9. Radar plot of PCM device performance metrics for GST124, GST144, and GST194. GST144 is the optimal trade-off featuring the high programming speed of GST194 and the large MW of GST124. Data extracted from 256 devices.

The MW is preserved after 10^5 cycles (**Fig. 7b**), with a starting of RESET degradation. GST144 shows the lowest SET and RESET variability, with an excellent stability upon cycling. The RESET resistance decreases to about 100 kΩ after 10^5 cycles but the devices preserve a reliable MW up to 10^7 cycles, where heater metal degradation is the likely cause of open failures (**Fig. 7c**). The good performance of the GST144 devices after 10^6 writing cycles is confirmed by the distributions in **Fig. 7d**, which remain largely unaffected compared to the not cycled ones (Fig. 5).

Material evolution is triggered by the total energy provided to the system during programming (**Fig. 8**). For GST144, in the case of fast programming pulses of 5 ns allowed by its high SET speed (Fig. 6), the material evolution in the active region is not expected before more than 10^8 cycles. By EDX analyses (not reported), we could appreciate an enrichment of about +25% in Sb content and a reduction of about -15% in Te content in the active region of the device after cycling (Fig. 7c) with almost no Ge evolution, without compromising the cyclability of the device. A summary of the electrical results for the three alloys is reported in **Fig. 9**, where the performance of the GST144 stands out, gathering the best features respectively from GST124 and GST194.

IV. Conclusions

In this article, we compared the physical and electrical properties of three GST congruent alloys, namely $Ge_1Sb_2Te_4$ (GST124), $Ge_1Sb_4Te_4$ (GST144), and $Ge_1Sb_9Te_4$ (GST194), with increasing Sb/Te ratio. We performed RvsT and XRD measurements on thin films, demonstrating the suppression of the cubic phase and the stabilization of the trigonal (hex) phase in alloys with Sb/Te ratio equal or higher than one, that feature a high crystal growth speed. We integrated these alloys into 16 kb arrays with critical dimensions down to 40 nm. Our results show that the SET programming speed and reliability (i.e. lower variability) is increased with the increase of the Sb/Te ratio, leading to a full crystallization with a pulse fall time shorter than 5 ns. However, the memory window (MW) is degraded in GST194 for a too high Sb/Te ratio. For the first time at our knowledge, we report the performance of GST144 congruent composition with Sb/Te ratio of 1. This alloy offers extremely fast SET speed and SET programming reliability, typical of high Sb/Te ratio compositions, and a MW compatible with standard GST124 (i.e. more than 3 orders of magnitude), representing an optimal trade-off for PCM applications. GST144 material shows stability in our test vehicle up to 10^7 pulses with reduced SET variability, good MW and limited elemental evolution into the active volume. Our findings support the tuning of Sb/Te content in GeSbTe alloys as a viable path for high-performance Phase-Change Memory.

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