# A Ka-Band Bidirectional Active Phase Shifter with Reciprocal I/O Techniques Achieving <1.9°/<0.5dB RMS Phase/Gain Errors Over 36% Bandwidth

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***Abstract*—This paper presents a Ka-band bidirectional active phase shifter (PS) with reciprocal input/output (I/O) techniques in 65-nm CMOS. To eliminate the need for reconfigurable matching networks when toggling between forward and backward modes, a bidirectional variable gain amplifier (BVGA) with bilateral impedance-matched capacitors is proposed, achieving consistent I/O impedances and enhancing BVGA stability. Moreover, a symmetry-enhanced quadrant-selection double-pole double-throw (DPDT) switch is proposed to improve I/O reciprocity. Based on the proposed BVGA and DPDT switches, an I/O reciprocal bidirectional PS is realized, exhibiting wide bandwidth and low RMS phase/gain errors. Measurements show the PS achieves 6-bit phase control with -4 dB peak gain, >-4.3 dBm $IP_{1dB}$, <1.9°/<0.5 dB RMS phase/gain errors across 25-36 GHz in both forward and backward modes, with a power consumption of 13 mW. Benefitting from the reciprocal I/O architecture, the average forward and backward gain and phase imbalances are suppressed to <0.24 dB and <0.8°, respectively.**

***Keywords—bidirectional, phase shifter, coupler, variable gain amplifier (VGA), millimeter-wave, wideband, CMOS***

## I. Introduction

Phased array techniques, which support beamforming and high-gain capabilities, have attracted significant attention in 5G millimeter-wave (mm-wave) and Ka-band satellite communications. However, to overcome the severe free-space path loss at these high frequencies, large-scale phased array transceivers are necessary. For cost-efficient and accurate beamforming transceivers designs, high-performance bidirectional phase shifters (PSs) are gaining popularity due to their potential to minimize transceiver area and cost.

PSs, which can be categorized into passive and active structures, have attracted significant attention and undergone extensive research. Passive PSs, including switched filter types [1], reflective types [2], and passive vector modulators (PVMs) [3]-[5], offer high linearity, zero power consumption, and bidirectional capability. However, they typically require a large chip area and exhibit high insertion loss. To compensate for these losses, variable gain amplifiers (VGAs) with sufficient gain are typically required. However, conventional VGAs are generally unidirectional, necessitating separate VGAs for transmitter (TX) and receiver (RX) paths, which significantly increases chip area. In contrast, active PSs, mainly based on I/Q vector modulation, exhibit advantages in considerable gain and smaller area [6]-[10]. However, many of these designs are inherently unidirectional, limiting their direct application in bidirectional systems. In [9] bidirectional variable gain amplifier (BVGA) topologies with phase inversion (PI) functions are presented. However, these configurations require four times as many parallel transistors as their unidirectional counterparts to achieve bidirectional and phase inversion (PI) features. This substantial increase in device count significantly elevates parasitic effects, leading to degraded linearity, reduced bandwidth, and more complex layouts. Additionally, PI-BVGAs typically exhibit mismatched input/output (I/O) impedances, necessitating reconfigurable matching networks when toggling between TX and RX modes. This requirement increases implementation complexity, design chip area, and introduces losses due to switch usage. In [10], a switch-less three-stack staggered BVGA structure with equivalent I/O impedances is presented. However, this design is single-ended, requiring two additional hybrid couplers to control the IQ polarity for quadrant selection, which leads to increased chip area and higher insertion loss. Additionally, the gate-source capacitance ($C_{gs}$) of the on-state output transistor significantly degrades the BVGA's linearity.

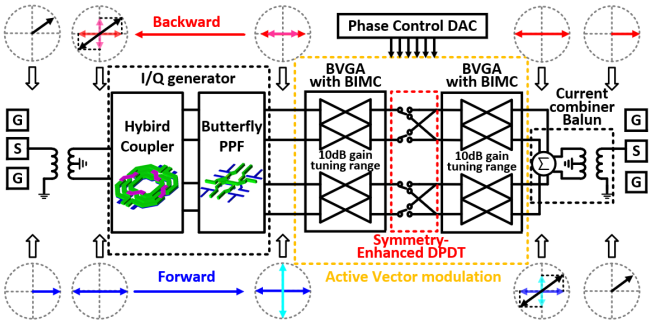
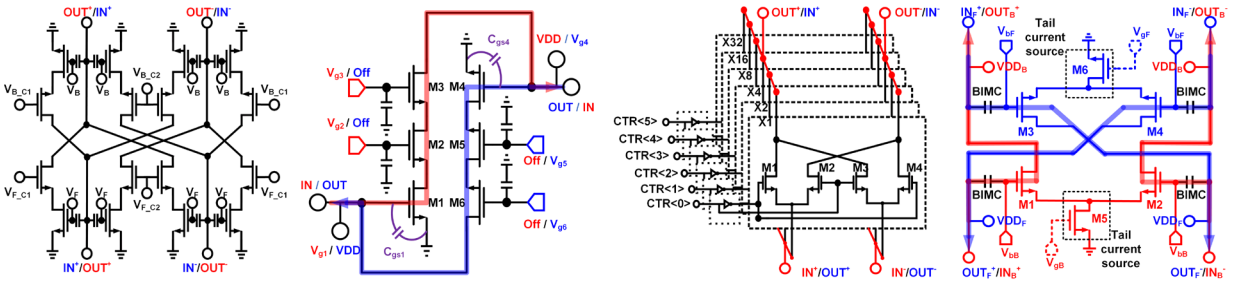


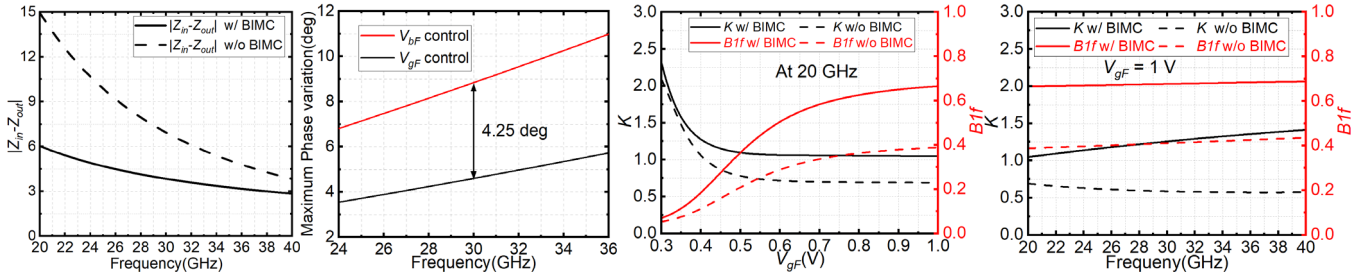

Fig. 1. Circuit block diagram of the proposed bi-directional PS.

To address these issues, this paper presents an I/O reciprocal bidirectional active PS architecture based on a proposed BVGA with bilateral impedance-matched capacitors (BIMC) and a symmetry-enhanced double-pole double-throw (DPDT) switch. The proposed PS architecture allows for the use of BVGA structures without PI functions, significantly minimizing device parasitics, enhancing BVGA linearity, and simplifying the overall design. The incorporation of BIMC improves the I/O impedance matching and stability of the BVGA, eliminating the need for reconfigurable matching networks when toggling between forward and backward modes, thereby extending the operating bandwidth. Additionally, the symmetry-enhanced DPDT structure is introduced, demonstrating excellent bidirectional performance. Thanks to the reciprocity of the proposed BVGA and DPDT switches, the bidirectional PS achieves consistent forward and backward performance over a 36% fractional bandwidth.




(a) (b) (c) (d)

Fig. 2. VGA topologies (a) PI-BVGA (b) Three-stack staggered BVGA (c) X-type attenuator (d) Proposed BVGA with BIMC




(a) (b) (c) (d)

Fig. 3. Performance comparison. (a) I/O impedance difference (b) Maximum phase variation (c) Stability vs $V_{gF}$ (d) Stability vs frequencies

## II. Circuit Implementation

Fig. 1 illustrates the block diagram of the proposed bidirectional PS. The I/Q generator based on [6], incorporating a coupler and an RC polyphase filter (PPF), is designed to provide wideband I/Q vectors. Simulation indicates the phase and amplitude imbalances are less than 2.2° and 0.3 dB, respectively, across 25 to 36 GHz. Specifically, the BVGA and the quadrant selection DPDT switches are symmetrically configured with identical I/O impedances. This symmetry allows the use of fixed (non-reconfigurable) matching networks when toggling between forward and backward modes, thereby reducing matching network losses, extending bandwidth, and simplifying implementation. Moreover, placing the quadrant-selection DPDT switch between the two BVGAs establishes a symmetrical I/O architecture, enhancing bidirectional consistency between forward and backward modes.

In the forward operating mode, the differential signal is converted into ±I and ±Q signals, which are then weighted by the BVGAs and combined through a current combiner balun to achieve the desired phase shift. In the backward operating mode, the current combiner balun functions as a power divider, splitting the signal into two identical signals. After BVGAs amplification, the signals are fed into I/Q generator, which operates as a quadrature signal combiner.

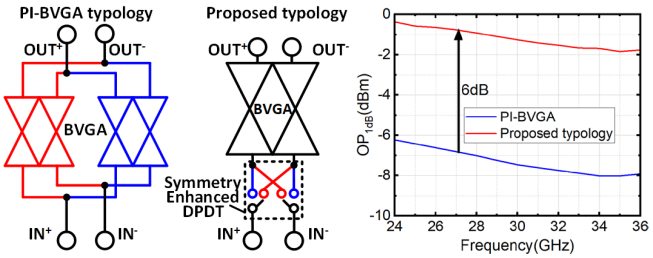
### *A. Bi-Direcitonal VGA with Identical I/O Impedance*

In conventional bidirectional vector-sum PSs, BVGA topologies with PI functions, such as PI-BVGAs [see Fig. 2 (a)], are essential for quadrant selection. However, these configurations typically require additional parallel transistors, which increase parasitics, degrade linearity, and complicate layouts. Moreover, PI-BVGAs often exhibit mismatched I/O impedances, necessitating reconfigurable matching networks when toggling between forward and backward modes. This requirement increases implementation complexity, design area, and introduces losses due to switch usage. In [10], a three-stack staggered BVGA structure with equivalent IO impedances is presented [see Fig. 2 (b)]. However, the $C_{gs}$ of transistor M4/M1 in forward/backward mode significantly reduces the BVGA gain and linearity. In [3]-[5], passive X-type attenuators are employed [see in Fig. 2 (c)] to ensure reciprocity and enable bidirectional operation but suffer from high insertion loss. To compensate for these losses, VGAs with sufficient gain are required. However, conventional VGAs operate unidirectionally, necessitating separate VGAs for TX and RX paths, which significantly increases chip area.

In this design, a BVGA structure with BIMC is proposed [see Fig. 2(d)] to achieve identical I/O impedances and enhance stability. The BIMC also function as DC-blocking capacitors, preventing undesired turn-on of the off-state transistors under large signal conditions and thereby improving the BVGA's linearity. To minimize phase variation during gain tuning, the BVGA gain is controlled by adjusting bias voltage ($V_{gF}$/$V_{gB}$) of the tail current source, rather than gate voltage ($V_{bF}$/$V_{bB}$) of common-source stage. Fig. 3 (a) and (b) show the simulated I/O impedance difference and maximum phase variation (MPV) with and without the BIMC. As observed, with BIMC, the I/O impedance difference of the BVGA ($|Z_{in}$-$Z_{out}|$) are minimized, and the MPV is reduced by 4.25° using tail current control. Due to the mismatch between the gate-drain capacitance ($C_{gd}$) of the off- and on-state transistors, the $C_{gd}$ of M1/M2 and M3/M4 cannot fully neutralized in either forward or backward mode. As a result, the BVGA may not maintain unconditional stability. Fig. 3 (c) and (d) show the stability factors $K$ and $B1f$ of the proposed BVGA versus $V_{bF}$/$V_{bB}$ and frequency. With the BIMC, the BVGA maintains unconditional stability across the 20-40 GHz during gain tuning.

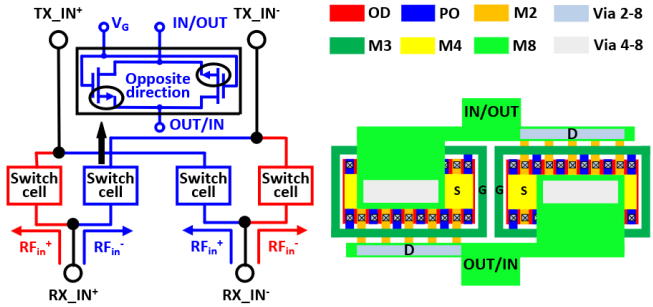
### *B. Symmetry-Enhanced DPDT for Quadrant Selection*

To achieve a 360° phase shift, vector-sum phase shifters require a 180° inversion of both the I and Q signal paths to implement quadrant selection. In conventional quadrant selection design of vector-sum PSs, PI-VGA topologies-utilizing a pair of paralleled differential VGAs-are typically preferred to eliminate the need for extra phase-selecting circuits [see Fig. 4(a)]. However, these topologies significantly increase the parasitics in the layout, resulting in reduced bandwidth and increased RMS phase/gain errors, particularly in BVGA. Moreover, the increased parasitics



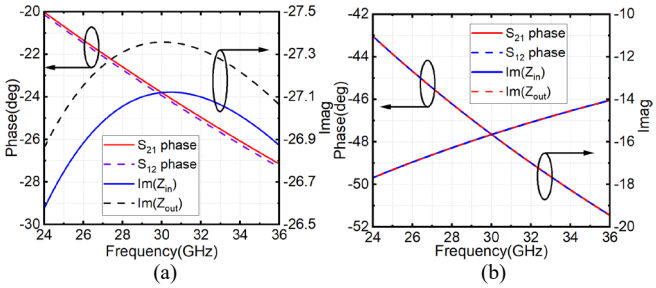

(a) (b)

Fig. 4. (a) Quadrant selection typologies. (b) Simulated $OP_{1dB}$ comparison.




(a) (b)

Fig.5. (a) Symmetry-enhanced DPDT architecture. (b) Switch cell layout.




(a) (b)

Fig. 6. Simulated $S_{21}/S_{12}$ phase and imaginary part of I/O impedances of (a) conventional w/o interconnects and (b) proposed switches w/ interconnects.

further degrade BVGA linearity. To address these issues, a BVGA combined with a symmetry-enhanced DPDT architecture is proposed for quadrant selection, as shown in Fig. 4 (a). Fig. 4 (b) compares the simulated $OP_{1dB}$ of the proposed architecture with that of the conventional PI-BVGA. As observed, the simulations indicate that the proposed design achieves a 6 dB improvement in $OP_{1dB}$. Additionally, the maximum available gain (MAG) of the proposed architecture remains comparable to that of the conventional PI-BVGA. This is because the parasitics in the PI-BVGA reduce its MAG, offsetting the insertion loss introduced by the DPDT switch in the proposed design.

In conventional DPDT switch, switch transistors are typically assumed to exhibit reciprocal behavior between their source and drain terminals. However, due to the intrinsic asymmetry in transistor layout, especially at mm-wave frequencies, this assumption does not hold. To improve the I/O symmetry of the DPDT switch, a symmetry-enhanced DPDT structure is proposed, as shown in Fig .5. The DPDT switch cell comprises a pair of parallel switch transistors with their source and drain terminals connected in reverse. Fig. 6 compares the simulated $S_{21}/S_{12}$ phase and imaginary part of I/O impedances of the conventional and proposed DPDT switches. As observed, the proposed structure, including the interconnects [see Fig. 4 (b)], demonstrates excellent bidirectional performance. It should be noted that the simulation results in Fig. 6 (a) do not include the interconnects; thus, the actual performance may be further degraded when interconnect effects are considered.

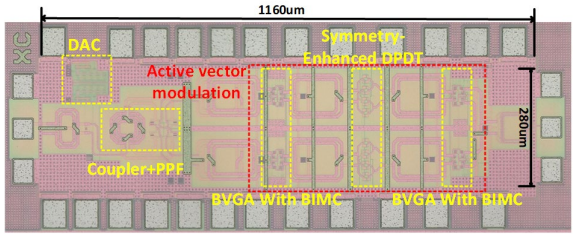
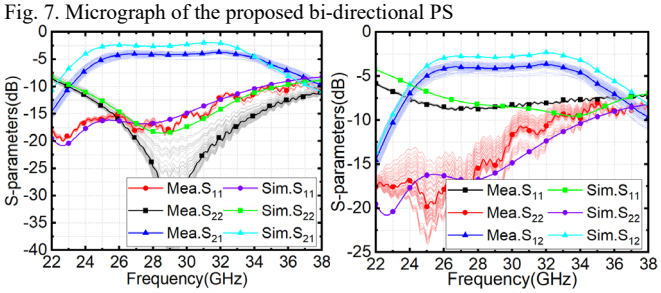
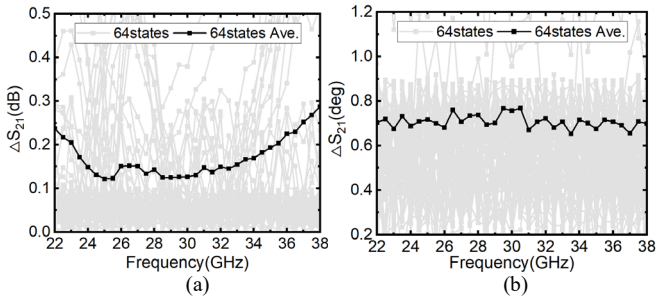



Fig. 7. Micrograph of the proposed bi-directional PS



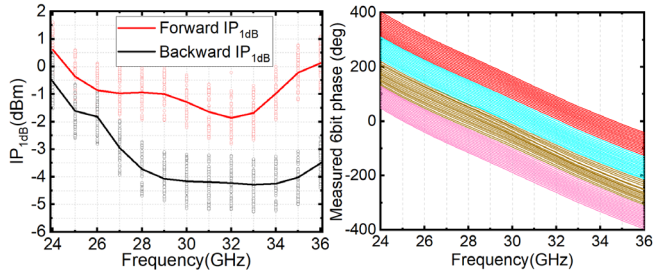

(a) (b)

Fig. 8. Simulated and measured S-parameters (a) in forward mode, and (b) in backward mode.



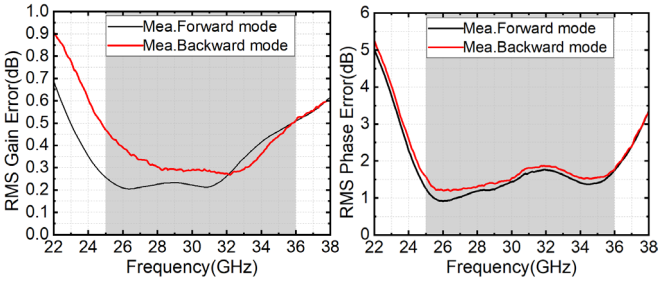

(a) (b)

Fig. 9. Measured forward and backward imbalances across 64 phase states. (a) Magnitude imbalance. (b) Phase imbalance.




(a) (b)

Fig. 10. (a) Measured $IP_{1dB}$. (b) Measured relative phases.




(a) (b)

Fig. 11. Measured (a) RMS phase error and (b) RMS gain error.

## III. Measurement Result

The proposed active bidirectional PS was implemented in a 65-nm CMOS process. Fig. 7 shows the chip microphotograph of the bidirectional PS including I/Q generator, BVGAs, DPDT switches, and the control DAC. The core size excluding the pads is 1160 × 280 μm$^2$ (0.32 mm$^2$). The supply voltages for RF and IO circuits are 1 V, and the dc power consumption is 13 mW.

TABLE I. PERFORMANCE COMPARISON WITH STATE-OF-THE-ARTS MM-WAVE BIDIRECTIONAL PHASE SHIFTERS

| | IMS'23 [3] | TCAS I'22 [4] | JSSC'20 [8] | TCAS II'25 [9] | TMTT'24 [10] | **This work** |
|---|---|---|---|---|---|---|
| Technology | 40nm | 28nm | 28nm | 28nm | 28nm | **65nm** |
| Resolution(bits) | 6 | 7 | 6 | 4 | 6 | **6** |
| Topology | PVSPS | PVSPS | AVSPS | ASTPS | AVSPS | **AVSPS** |
| Frequency(GHz) | 26-32 | 32-40 | 26.5-29.5 | 26-30 | 13-15 | **25-36** |
| FBW | 20.69% | 22.22% | 10.71% | 14.28% | 14.28% | **36.06%** |
| Peak Average Gain(dB) | -19 | -16.9 | 0 | 2 | -5.4 | **-4** |
| DC Power(mW) | 0 | 0 | 20 | 40 | 15.8 | **13** |
| RMS Gain Error(dB) | <1.2 | <0.36 | <0.4 | <1.1 | <0.55 | **<0.5** |
| RMS Phase Error(deg) | <2.6 | <1.6 | <2 | <9.5 | <2.4 | **<1.9** |
| $IP_{1dB}$(dBm) | >14 | >10.2 | >-9.6* | >2.3 | >-11.9 | **>-4.3** |
| Core Chip Size($mm^2$) | 0.15 | 0.14 | 0.3 | 0.21 | 1.35$ | **0.32** |
| Core size factor | 3 | 3 | 1 | 1 | 1 | **1** |
| $FoM_1$ | 3.83 | 23.68 | 191.52 | 58.01 | 17.79 | **375.92** |
| $FoM_2$ | 19.06 | 23.28 | 19.11 | 13.47 | 13.67 | **25.01** |

* -9.6dB addition from $IIP_3$; $ Including pads

$$FoM_1 = \frac{f_0(GHz)\times G_{AV}(abs)\times B_{3dB}(GHz)\times Resolution(bits)}{RMS\ phase\ error\ in\ B_{3dB}(\deg)\times RMS\ gain\ error\ in\ B_{3dB}(lin)},\quad FoM_2 = 10\log\frac{FBW(\%)\times Res.bits}{RMS\ phase\ error\ in\ B_{3dB}(\deg)\times RMS\ gain\ error\ in\ B_{3dB}(\mathrm{lin})\times Core\ size\ factor\times Core\ Chip\ size}$$

Fig. 8 shows the measured S-parameters of the active bidirectional PS across all 64 phase states in forward and backward modes. The peak average gain is -4 dB with a 3-dB bandwidth from 25 to 36 GHz, and the measured $S_{11}$ and $S_{22}$ are lower than -7.5 dB for both forward and backward modes. Fig. 9 demonstrates the measured gain and phase imbalances between forward ($S_{21}$) and backward ($S_{12}$) of all 64 phase states. Benefiting from the symmetric design of the BVGA and the quadrant selection DPDT switches, the average gain and phase imbalances are suppressed to <0.24dB and <0.8°, respectively.

Fig. 10 (a) presents the simulated and measured $IP_{1dB}$ across all phase states in forward and backward modes. In the frequency range from 24 to 36 GHz, the measured results show an average $IP_{1dB}$ of >-4.3 dBm in both modes. The measured relative phases shown in Fig. 10 (b) reveals full 360º phase shift with 6-bit resolution. Fig. 11 shows the measured RMS phase/gain errors of the bidirectional PS in forward and backward modes. The measured RMS phase/gain errors are <1.9° and <0.5 dB across 25-36 GHz in both forward and backward modes, respectively.

Table I summarizes the performance of the proposed active bidirectional PS and its comparison with state-of-the-art bidirectional PSs. For a fair comparison with passive PSs, figure-of merits $FoM_2$ is derived from the typical PS $FoM_1$ in [7], taking into account the core size factor. Since the passive PSs require additional amplifiers, typically unidirectional, to compensate the losses, their core size factor is considered to be 3 (i.e., passive PS + unidirectional amplifier × 2 = 3) [10]. Clearly, the proposed PS exhibits the largest operating bandwidth and highest PS FoMs.

## IV. CONCLUSION

A 25–36 GHz 6-bit bidirectional PS is presented. Based on the proposed BVGAs with BIMC and symmetry-enhanced DPDT switches, the PS achieves wide bandwidth, low insertion loss, high linearity, low RMS phase/gain errors, low power consumption, as well as excellent bidirectional functionality. With these distinctive features, this design is expected to be one of the promising candidates for future cost-efficient and compact phased array systems.


## ACKNOWLEDGMENT

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