A 24-MHz BW, 97-dB SFDR, CT ΔΣ Modulator with a Jitter Robust Shunt Current Steering DAC

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***Abstract*—A 1.6 GHz continuous-time Delta Sigma modulator with increased robustness toward clock jitter is presented. It achieves a 67.6 dB dynamic range (DR) and a spurious-free dynamic range (SFDR) of 97 dB in a 24 MHz bandwidth (BW). A novel return-to-open (RTO) shunt current-steering digital-to-analog converter (SCS-DAC) combined with a clock jitter cleaner allows for large rms jitter without a significant impact on performance. The modulator is designed for process-voltage-temperature (PVT) robustness, for very low sensitivity to mismatch, and no linearity calibration is employed. It has been fabricated in a 28 nm CMOS technology. The 1 V core consumes 29.9 mW and occupies 0.21 mm^2.**

***Index Terms*—CTΔΣM, DAC, Linearity, RTO, Jitter**

I. Introduction

In many wireless applications, where the physical channel is simultaneously shared with a multitude of users, signals from adjacent channels cause large interferers and mostly dominate the requirements on the receiver analog-to-digital converter (ADC). This happens mainly due to non-linearity in the line-up, which mixes out-of-band (OOB) tones back to the frequency range of interest. The linearity of the receiver is thereof of utmost importance, whereas the full-band resolution in terms of signal-to-noise ratio (SNR) can be compromised. For the band of interests of tenths of MHz, continuous-time (CT) Delta-Sigma-Modulator (ΔΣM) have the potential to achieve such demanding linearity and ADCs with extended linearity have been variously shown [1] [2].

In a CTΔΣM, the linearity is mostly dominated by the linearity of the input stage, i.e. the first filter stage and the outermost digital-to-analog converter (DAC).

Multi-bit DACs allows good SNR at low oversampling ratio (OSR) but have limited linearity due to element mismatch. The conventional linearization techniques have drawbacks: dynamic element-matching (DEM) causes increased activity, worst inter-symbol-interference (ISI), and is not suitable for high-speed due to latency; calibration requires additional circuitry and extensive digital computation [3], often performed off-chip [4]. Thus, when area, complexity, and robustness for high linearity are targeted, single-bit designs have been employed in the state of the art (SoA) [1] [5].

However, due to its larger steps and dynamics, the use of single-bit DACs increases the linearity requirement on the loop-filter and shows a largely increased sensitivity to clock jitter, tightening the requirements on the on-chip frequency

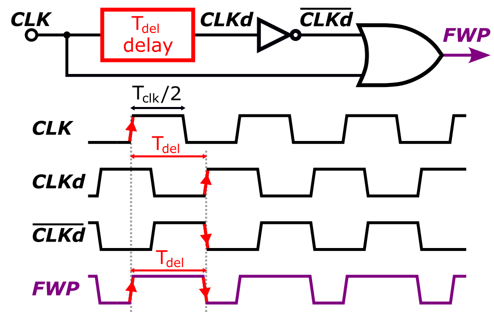

Fig. 1. Fixed-width pulse clock generator.

generator and clock distribution line. A technique beneficial to improve both effects consists in applying a finite impulse-response (FIR) filter to single-bit DAC. This makes the output resemble that of a multi-bit DAC, with the associated benefits [6]. However, the FIR is effective in reducing the jitter sensitivity only when a non-return-to-zero (NRZ) pulse shape is used, while it is less beneficial for a return-to-zero (RTZ), and equivalently a return-to-open (RTO). A NRZ DAC has lower jitter sensitivity, but it suffers strongly from ISI, which is also affecting the linearity. The conventional DAC types used to implement NRZ and RTZ(RTO) are current steering (CS) and resistive. Resistive DACs have the lowest noise, but they put strong requirements on the reference generation (e.g. bandwidth (BW) and Power Supply Rejection Ratio (PSRR)) [1] [5]. CS designs are worse in noise but result in relaxed and more robust reference generation. Another way to reduce the jitter sensitivity is to use a switched-capacitor-resistor (SCR) DAC [7], which has an exponentially decaying pulse shape. It is robust to ISI and jitter, but requires much higher BW in the integrator amplifier, precise reference generation, and reduces the implicit aliasing rejection of CTΔΣMs [8].

From this, it is obvious that achieving high linearity is not straightforward when simultaneously other specifications (jitter sensitivity, PSRR, aliasing-rejection, etc.) must be met and robustness for industrial application must be achieved. When building a complete system all the necessary circuitry must be taken into account, therefore power-outsourcing to calibration, clock generation or reference generation to the periphery of the ADC are not feasible, even though they beneficially improve the figure-of-merit (FoM) of the ADC core. Finally, when a robust design is required, not a single best performing device for publication can be targeted, but power consumption must be generously traded for high yield.

In this work, a clock jitter cleaner is employed that improves jitter sensitivity similarly as shown in [9]. Moreover, a novel 3-level RTO shunt current steering (SCS) DAC architecture is employed to achieve robust and intrinsically linear operation in combination with a FIR feedback. The manuscript is organized as follows: Section II introduces both clock jitter cleaner and SCS-DAC techniques. Section III shows the implementation of this DAC in a CTΔΣMs realized in a 28 nm CMOS technology. Section IV discusses the comparison with the SoA.

II. Jitter sensitivity reduction

A. Fixed-Width-Pulse Clock Generator

The jitter sensitivity of a NRZ or RTZ DAC is due to the fact that the shape of the current pulse is affected by the time instant of the transitions. A RTZ DAC is worse in terms of jitter sensitivity, since it features two transitions in each period regardless of the code [10], such that the activity factor is larger. Moreover, the RTZ amplitudes are larger compared to the equivalent NRZ, leading to larger jitter-related errors. The integrated current pulse is then randomly changed by the jitter introducing charge noise, and it reduces the SNR of the ΔΣM.

Whereas most SoA techniques for improving jitter sensitivity, such as multi-bit DAC, shaped waveforms, or FIR DAC, aim to reduce the effect of clock jitter, another possibility is to employ an on-chip clock jitter cleaner [9]. The idea is to allow for large jitter values from the clock generator, but use the clock to create a fixed-width pulse (FWP) to control the feedback DAC. This can be done using the circuit in Fig. 1 combining the input clock CLK with a delayed and inverted version of itself using an OR gate. The resulting output clock FWP then has a falling edge which is separated from the rising edge by a constant delay, obtaining a fixed-width. The position of the FWP pulse within the period is still varied by the jitter, but as only the area of the outermost feedback pulse matters in a CTΔΣM [10], the performance becomes independent from the main clock jitter: by preserving the total charge, no error is introduced by the DAC. In an actual implementation, the delay cell and the gates will obviously introduce noise by themselves, which causes residual jitter. This noise can be traded against power consumption in the clock jitter cleaner. The delay can be realized as an inverter chain or, to have less dependency on the supply voltage, with RC delay cells. This idea, originally introduced at the simulation level in [9], was extended in [11], where 4 FWPs were generated and combined to form a triangular DAC shape. In the following, we implement the clock cleaner circuit from [9] in combination with a novel CS DAC that can fully exploit its benefits.

B. Novel RTO Shunt Current Steering DAC Architecture

In order to benefit from the reduced jitter sensitivity of FWP, the novel 3-level RTO shunt current steering DAC (SCS-DAC) architecture [12] in Fig. 2 is used. Transistors M_1-M_4 are biased in saturation region and constitute the PMOS and NMOS cascoded current sources, as in a conventional CS DAC. The switches S_1-S_6 are used to steer the current, and are controlled by the mutually exclusive digital signals P, Z, and N to convert the data codes +1, 0 and -1 respectively. S_7, S_8 and S_9 are transmission gate switches, controlled by $\overline{FWP}$ (inverted FWP), which are used to turn off the cascode devices M_2 and M_3, shunting the current to create the open state. P, Z, and N are controlled in a NRZ fashion. $\overline{FWP}$ is aligned to be active when the data signals are switching. When $\overline{FWP}$ is active, the nodes V_{xP} and V_{xN} are shorted together, and to a reference voltage V_{CM}. This turns off the cascode devices, blocking any current from flowing through. In this state, the current sources are kept on and their current flows through S_7. S_8 and S_9 are sized to be more resistive than S_7, and have the purpose of preventing nodes V_{xP} and V_{xN} from drifting away from the middle voltage point, even in presence of mismatch between the currents of M_1 and M_4.

The strong advantages of this architecture come from the fact that the steering switches S_1-S_6 are switched at zero current. This means that their dynamic switching behavior does not affect the pulse shape. Therefore, any dynamic mismatch caused by the threshold variation of the switches S_1-S_6, or any mismatch and jitter in their gate drivers is not important, in contrast to conventional NRZ and RTZ DACs. The dynamic behavior of I_{oP} and I_{oN} during the rising and falling edges depends mainly on M_1-M_4, and S_7-S_9. The latter are switched in each period, thus always producing the same voltage swing at the node V_{xP}, V_{xN}, and therefore the same shape of current flowing through the cascodes M_2 and M_3, regardless of the data of the current and previous periods. This guarantees almost identical output current pulse shapes for codes +1 and -1 (with opposite polarity), ensuring a very high DAC linearity and, moreover, robustness to ISI.

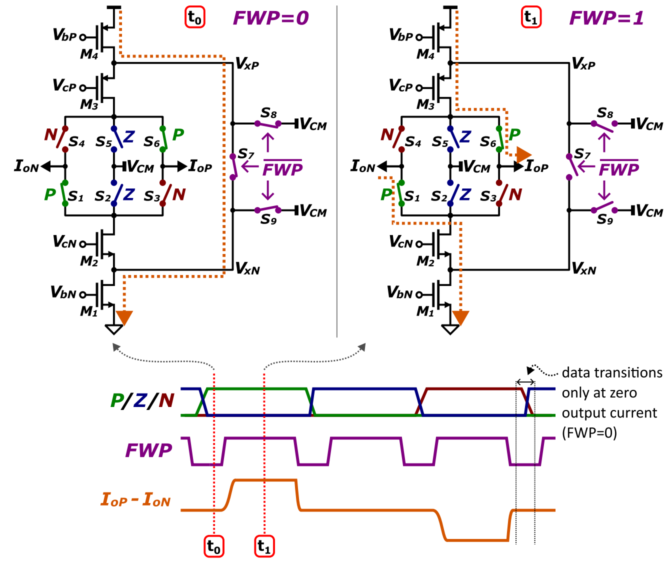

Fig. 2. Novel 3-levels RTO SCS-DAC architecture.

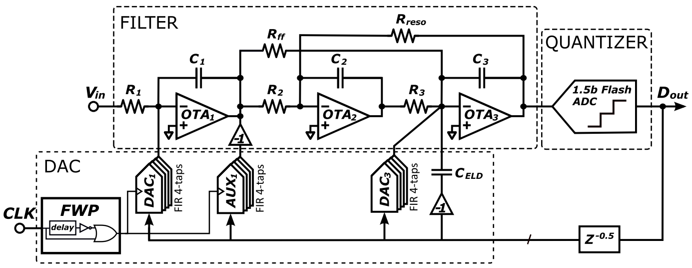

Fig. 3. 3rd order CT ΔΣ.

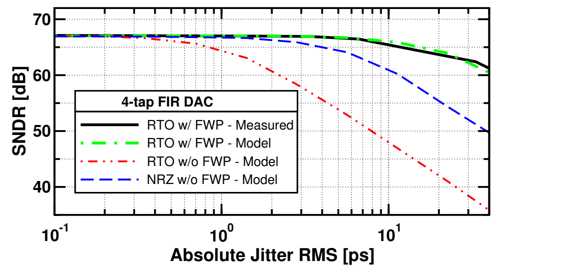

Fig. 4. Measured SNDR vs. clock absolute jitter RMS. A comparison with the SNDR predicted by a model with different types of DAC is shown. All DACs are FIR 4-taps. The SNDR has been calculated on a 20MHz bandwidth.

A second-order effect from S_1-S_6 comes from their on-resistance and charge injection mismatch, which can be lowered by increasing the switches width. Since they do not affect the dynamic behavior, the switching time is not critical and they can be sized much larger than in conventional architectures, without having to increase the gate driver strengths. The lower on-resistance allows to spare headroom for the cascoded current sources. This DAC topology is therefore suitable for robust, low supply voltage designs.

III. Implementation and Measurements

A. Modulator

The proposed DAC architecture has been implemented in a 3rd order CT ΔΣ. Fig. 3 shows the equivalent single-ended circuit. The ΔΣM has a CRFF/FB architecture, chosen to avoid excessive Signal Transfer Function (STF) peaking. It is clocked at 1.6 GHz and has a signal BW of 24 MHz, corresponding to an OSR value of 33.3.

The loop-filter is realized using active integrators, due to the stringent linearity and robustness requirements, and the conventional RC tuning is implemented. The high linearity performance must be achieved in the temperature range -50 °C to 150 °C, and over voltage and process variation. This requires an over-design of the operational transconductance amplifiers (OTAs) in the nominal case, leading to a significant increase in current consumption.

The feedback DAC in the outermost loop uses a 4-tap FIR filter, where every tap uses the proposed 3-level RTO SCS architecture. The FIR filter was chosen to smooth the feedback and enhance the linearity of the first integrator. The clock jitter cleaner generates the RTO pulse, and its RC delay line is tuned to restore the correct modulator gain over process variation. To further help the first OTA (OTA_1) deal with the RTO current, an assisting DAC AUX_1 [13] is connected at its output. AUX_1 is a copy of DAC_1 (connected with inverted polarity) and provides the current needed to charge the capacitor C_1 when a DAC pulse occurs, offloading OTA_1. This reduces the OTA virtual ground swing, improving linearity.

DAC_3 used in the fast inner path is a conventional 3-levels CS DAC, chosen for its lower latency compared to the SCS-DAC. It is realized as a 4-tap FIR DAC with unequal tap weights, and restores the original noise transfer-function (NTF). C_{ELD} is used for ELD compensation, by creating a direct path through OTA_3.

B. Jitter Measurements

To measure jitter sensitivity, a Rohde Schwarz SMA100B generator with the FM modulation option was used. The FM modulation input, band limited to 10 MHz, is driven by a white noise generator. The amplitude of the modulation has been swept and the correspondent rms jitter has been characterized with a Rohde Schwarz FSWP phase noise analyzer. Figure 4 shows the measured signal-to-noise-and-distortion ratio (SNDR) of the ΔΣM versus the rms jitter. It also shows the SNDR predicted with a Simulink model of the implemented ΔΣM for different choices of the outermost feedback DAC. The drastically improved jitter robustness is evident.

C. Linearity and SNDR Measurements

Figure 5a shows SNDR and spurious-free dynamic range (SFDR) vs. input signal level for a single-tone at 2.4 MHz. The peak SNDR is at -4.2 dBFS and is equal to 65.2 dB on a 24 MHz BW (full-scale (FS)=0.5 V). The dynamic range (DR) is equal to 67.6 dB. Figure 5b shows the spectrum for a single-tone input with frequency 2.4 MHz and amplitude -5.1 dBFS. Figure 5c shows the spectrum for a dual-tone test with input frequencies 21.0/21.5 MHz and input amplitude -10.6 dBFS. The third-order intermodulation distortion (IMD_3) are measured to be -107.5/-103.9 dBFS, indistinguishable from the noise floor. Figure 6 shows the dual-tone worst IMD_3 for 8 devices, measured in the temperature range -50 °C to 150 °C.

IV. Conclusions

A CTΔΣM with 24 MHz BW, 67.6 dB DR was built in a 28 nm technology. A novel RTO SCS-DAC was introduced and was paired with a clock cleaner. This allows to achieve a high linearity without the need for linearity calibration, even in presence of strong clock jitter, and over an extended temperature range. Table I shows the comparison with the SoA. The high design robustness comes with a large over-design of power consumption in the loop-filter, shown in the power breakdown in Fig. 7, next to a photo of the chip. The presented techniques of the RTO SCS-DAC paired with a clock cleaner have a limited impact on power consumption, while allowing to save power at system level in the clock generation and distribution, making them an attractive design choice for high-linearity ΔΣM.

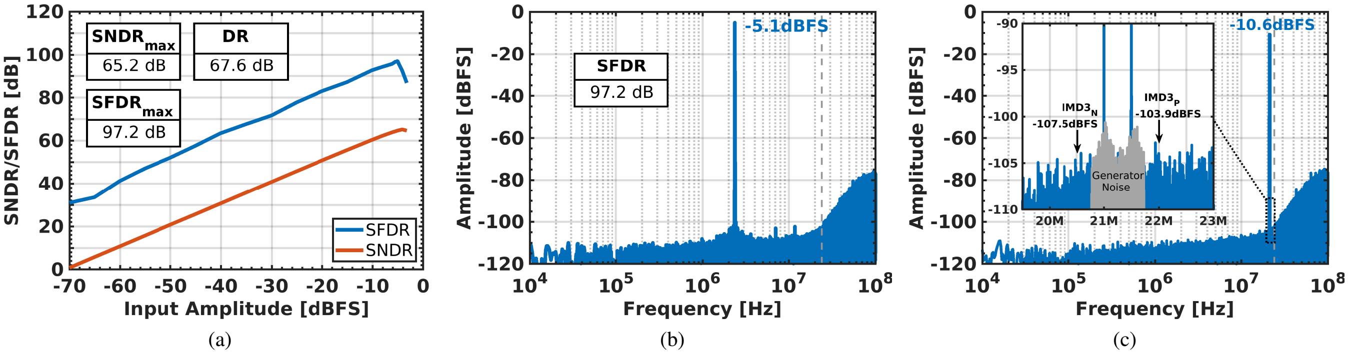

Fig. 5. (a) SNDR/SFDR vs input amplitude (single-tone at 2.4 MHz); spectrum obtained after the on-chip cascaded integrator–comb filter (decimation factor equal to 8) for: (b) single-tone at 2.4 MHz, (c) dual-tone at 21.0/21.5 MHz. The resolution bandwidth is equal to 381.5Hz

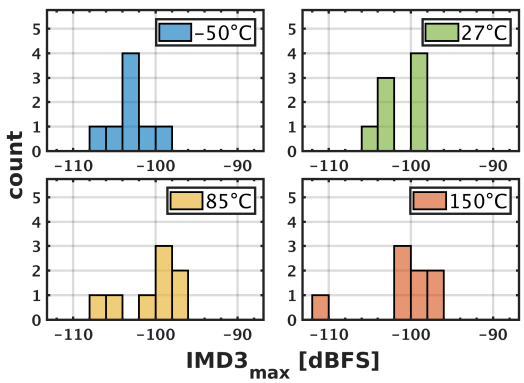

Fig. 6. Dual-tone (-10.6 dBFS) IMD3$_{max}$ for 8 devices across temperature.

TABLE I
STATE OF THE ART HIGH LINEARITY HIGH SPEED CT$\Delta\Sigma$M.

	This work	[5]	[1]	[3]	[4]
Technology	28nm	65nm	65nm	28nm	65nm
Supply [V]	1.0	1.1	1.2	0.9/1.5	1.2/1.8
DAC Type	SCS-RTO(FWP)	R-NRZ	R-RT0	R-RT0	CS-NRZ
DAC levels	3	2	2	4	16
FIR taps	4	8	-	-	-
Bandwidth [MHz]	24	20	25	120	10
Fclk [MHz]	1600	2560	2200	6000	640
SFDR [dBc]	97.2	98.6	106	102.5	92.4 w/ cal 54.4 w/o cal
Peak SNDR [dB]	65.2	82.1	77.0	72.3	79.6 w/ cal 54.2 w/o cal
DR [dB]	67.6	84.2	77.0	72.3	84.5 w/ cal
Jitter Robustness	**High**	Medium	Low	Low	Medium
Linearity Calibration	**Not Needed**	Off-chip	Not Needed	Background	Off-chip
Alias rejection [dBc]	-65	-	-	-64	-
Robustness	PVT	-	PVT	-	-
Power [mW]	29.9	11.3	41.4	108.8	5.35
FOM_{SNDR} [dB]	154.3	174.5	164.8	162.0	172.3
FOM_{DR} [dB]	156.7	176.6	164.8	162.0	177.2

$FoM_{(SN)DR}$ = (SN)DR + 10log10(BW/Power), R: resistive, CS: current steering

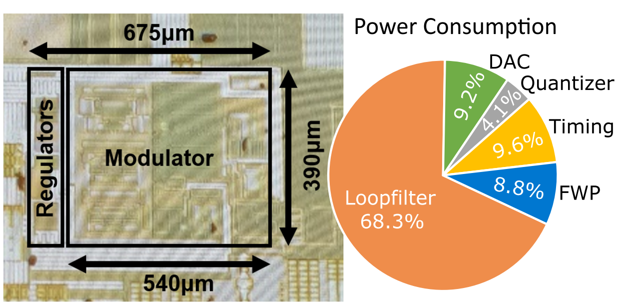

Fig. 7. Die photo and power consumption breakdown.

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REFERENCES

[1] L. Breems, M. Bolatkale, H. Brekelmans, S. Bajoria, J. Niehof, R. Rutten, B. Oude-Essink, F. Fritschij, J. Singh, and G. Lassche, "A 2.2 GHz Continuous-Time Delta Sigma ADC With -102 dBc THD and 25 MHz Bandwidth," *IEEE JSSC*, vol. 51, no. 12, 2016.

[2] M. Runge, D. Schmock, T. Kaiser, and F. Gerfers, "A 0.9V 45MS/s CT $\Delta\Sigma$ Modulator with 94dB SFDR and 25.6fJ/conv. enabled by a Digital Static and ISI Calibration in 22 FDSOI CMOS," in *IEEE CICC*, 2021.

[3] M. Bolatkale, R. Rutten, H. Brekelmans, S. Bajoria, Y. Gao, B. Burdiek, and L. J. Breems, "A 28-nm 6-GHz 2-bit Continuous-Time $\Delta\Sigma$ ADC With -101-dBc THD and 120-MHz Bandwidth Using Blind Digital DAC Error Correction," *IEEE JSSC*, vol. 57, no. 12, 2022.

[4] W. Wang, Y. Zhu, C.-H. Chan, U. Seng-Pan, and R. P. Martins, "A 5.35 mW 10 MHz bandwidth CT third-order Delta Sigma modulator with single Opamp achieving 79.6/84.5 dB SNDR/DR in 65 nm CMOS," in *IEEE ASSCC*, 2017.

[5] A. Baluni and S. Pavan, "Analysis and Design of a 20-MHz Bandwidth Continuous-Time Delta-Sigma Modulator With Time-Interleaved Virtual-Ground-Switched FIR Feedback," *IEEE JSSC*, vol. 56, no. 3, 2021.

[6] A. Sukumaran and S. Pavan, "Low Power Design Techniques for Single-Bit Audio Continuous-Time Delta Sigma ADCs Using FIR Feedback," *IEEE JSSC*, vol. 49, no. 11, 2014.

[7] M. Ortmanns, F. Gerfers, and Y. Manoli, "A continuous-time Sigma Delta Modulator with reduced sensitivity to clock jitter through SCR feedback," *IEEE TCAS-I*, vol. 52, no. 5, 2005.

[8] S. Pavan, "The inconvenient truth about alias rejection in continuous time Delta Sigma converters," in *IEEE ISCAS*, 2011.

[9] H. Chang and H. Tang, "A simple technique to reduce clock jitter effects in continuous-time delta-sigma modulators," in *IEEE ISCAS*, 2008.

[10] F. Gerfers and M. Ortmanns, *Continuous-time sigma-delta A/D conversion: fundamentals, performance limits and robust implementations*. Springer Science and Business Media, 2006.

[11] Y.-C. Chang, W.-H. Chiu, C.-C. Lin, and T.-H. Lin, "A 4MHz BW 69dB SNDR continuous-time delta-sigma modulator with reduced sensitivity to clock jitter," in *IEEE ASSCC*, 2011.

[12] M. Dalla Longa and F. Conzatti, "System and method for current digital-to-analog converter," U.S. Patent 11245410B1, Feb. 8, 2022.

[13] S. Pavan and P. Sankar, "Power Reduction in Continuous-Time Delta-Sigma Modulators Using the Assisted Opamp Technique," *IEEE JSSC*, vol. 45, no. 7, 2010.