An NIR-Enhanced BSI SPAD with an External Adaptive Active Quench and Clock Recharge Interface

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***Abstract*—A silicon-based backside-illuminated (BSI) SPAD with an external adaptive active quench and clock recharge (AAQCR) interface is presented. Optimized doping profiles and fabrication processes yield a deeper junction, resulting in reduced dark count rate (DCR) and enhanced photon detection probability (PDP) in the shortwave near-infrared spectrum for LiDAR applications. Fabricated using a 180-nm CMOS process, the AAQCR reliably drives the discrete external SPAD. Two feedback loops are integrated to optimize recharge signal duration and adapt clock frequency to a wide range of incident light intensities. Additionally, a data compression unit is incorporated to reduce output data rate. Measurement results indicate a high PDP of 32.5% at 660 nm and a low DCR of 0.7 cps/μm², with the AAQCR ensuring reliable reset and clock frequency convergence for desired counting linearity.**

Keywords—NIR-enhanced, SPAD, BSI, adaptive active quench and clock recharge (AAQCR), counting linearity

I. Introduction

Single-photon avalanche diodes (SPAD) are high-sensitivity photon detectors capable of detecting single-photon, having found widespread applications including LiDAR [1],[2], consumer electronics, and night vision detection system. The primary objective of SPAD design focuses on maximizing photon detection efficiency (PDE) by enhancing light absorption and modulating potential within the device, while simultaneously reducing dark count rate (DCR), jitter, and after-pulsing (AP). However, in sub-micrometer tech nodes, higher doping levels lead to narrower depletion width, necessitating the meticulous design of internal potentials. Therefore, a lot of work is focused on doping optimization. There have been SPAD structures composed of variety of avalanche multiplication junction including PW/NW, DPW/BNW, PLDD/HVNW in 55-nm technology [3],[4],[5]. But these structures exhibit shallow junction depths, resulting in the shorter optical path during the carrier multiplication process. This leads to a lower photon detection probability (PDP) for the SPAD in shortwave near-infrared (NIR) spectrum.

The performance of SPAD also depends on quenching and recharge circuits (QRC). An ideal QRC should rapidly terminate avalanche currents and stabilize reverse bias recovery. Among several existing QRCs, passive quench passive recharge (PQPR) and active quench active recharge (AQAR) are commonly used. The PQPR configuration is favored for its simplicity and compactness. However, it suffers from non-monotonic counting under high illumination due to SPAD paralysis. Additionally, the recharging current is limited to tens of μA for reliable quenching, causing unacceptable dead time for driving external SPADs. In contrast, AQAR circuits actively recharge the SPAD to mitigate paralysis [6]. However, AQAR implementations often require voltage-controlled delay units to achieve adjustable hold-off time, which increase area consumption and reduce the fill factor, particularly in large arrays.

A promising alternative is the synchronous clock-driven recharge scheme. Although several designs have achieved large dynamic range or short dead time [7],[8],[9], these methods rely on externally sourced recharge signals and monostable circuits. However, the optimal recharge duration time varies across SPADs due to inconsistency of capacitances, recharge strength and unpredictable loading for driving external SPADs. In additional, recharge clock frequency is not adaptive to the incident photon intensity in the previous works.

To address the aforementioned issues, an active quench and clock recharge (AAQCR) is designed to drive the external NIR-enhanced BSI SPAD. The SPAD is manufactured using a 55-nm BSI process, which can enhance the PDP in the NIR spectrum and achieve the longest possible optical path during the optical multiplication process. In addition to controlling process cleanliness, we have implemented multi-step gettering to maximize impurity removal in the active region. Due to the high cost of 55-nm BSI processes, the AAQCR chip is separately fabricated in a cost-effective 180-nm process, which provides high driving ability without sacrificing the external SPAD performance. Through two feedback loops, the circuit enables adaptive adjustment of the recharge clock frequency and optimal recharge signal width based on the incident light intensity and SPAD load conditions. Fig. 1 illustrates the test board picture, and the cross-sectional view of the SPAD and the AAQCR chip micrograph are given as well.

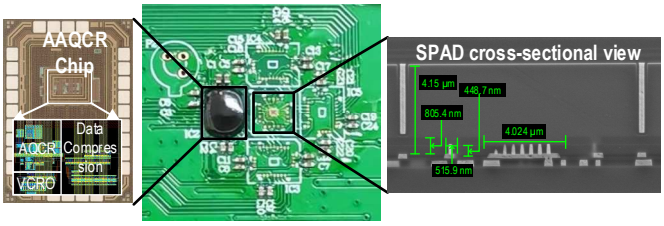

Fig. 1. Photograph of the test board along with the SPAD cross-sectional view and the AAQCR chip micrograph.

II. SPAD Design

Fig. 2 shows the structure of the proposed SPAD. The modified doping details for each well are illustrated in Fig. 3. The inherent limitations of silicon absorption coefficient have posed challenges for LiDAR, leading to low PDP in the NIR spectrum due to near-surface avalanche multiplication junctions. By positioning the multiplication junction away from the surface, the BSI structure extends the optical path,

thereby enhancing the PDP for long wavelengths. To achieve a good NIR response while reducing the doping concentration requirements for guard rings, we use a P^+/DNW junction to obtain a wider depletion region and the DNW is retrograde doped. To address the higher breakdown voltage and a lower peak electric field due to the doping concentration of DNW decreases near the surface, the junction depth of the P^+ well is adjusted to 448.7 nm through three times ion implantation. To decrease the probability of band-to-band tunneling, the P^+ well doping concentration is appropriately reduced. As a guard ring, the doping concentration and depth of the PW are modified to better suppress curvature effects, achieving a junction depth of 805 nm.

The primary sources of DCR are thermal generation, band-to-band tunneling, and deep-level traps. In this work, the increasing depth of the avalanche junction avoids surface states and high-defect regions near the surface. Additionally, the reduced P^+ well doping concentration decreases the probability of band-to-band tunneling. Nevertheless, deep-level traps might be present within broad depletion regions. These carriers induce avalanche releases and ultimately contribute to dark counts and AP. Hence, we implemented multi-step gettering after high-energy implantation to minimize injection damage within the active region. To minimize crosstalk, backside deep trench isolation (DTI) is additionally utilized to isolate the device. The DTI, approximately 3.5 um deep, is located in the middle of the isolation N-well, near its end surface. This design prevents traps from the etching and filling processes from negatively influencing the DCR and AP.

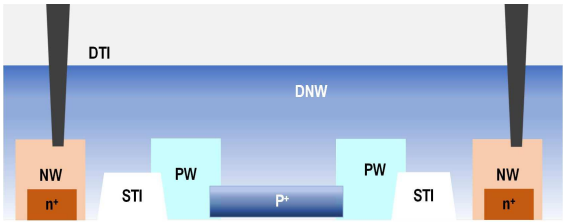

Fig. 2 Structure of the proposed SPAD.

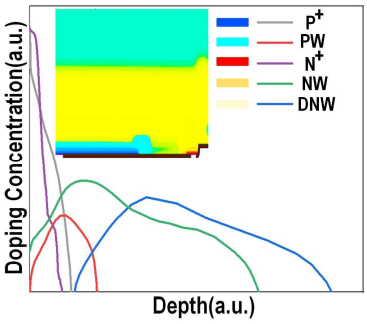

Fig. 3 The modified doping details for each well.

III. AAQCR Design

Fig. 4 shows the proposed AAQCR circuit architecture and detailed schematics of each block. The circuit comprises four parts: VCRO, AQCR circuit, data compression module, and external feedback regulation circuit. The VCRO is used to generate the recharge clock signal CLK, which periodically recharges the SPAD. A closed-loop feedback mechanism regulates the VCRO control voltage (V_{TUNE}) through real-time monitoring of the counting ratio of $SPAD_{OUT}$ to CLK, enabling dynamic CLK frequency adaptation. The data compression module is adopted to achieve a preliminary counting summation, thus reduce the output data rate. The following describes four parts of the circuit in detail.

A. VCRO

The VCRO architecture incorporates a thick-oxide transistor (M_1) with its gate terminal connected to the V_{TUNE}, which can be adjusted by the feedback loop to achieve an optimal frequency. The recharge clock can be either provided by the VCRO or external sources via a multiplexer.

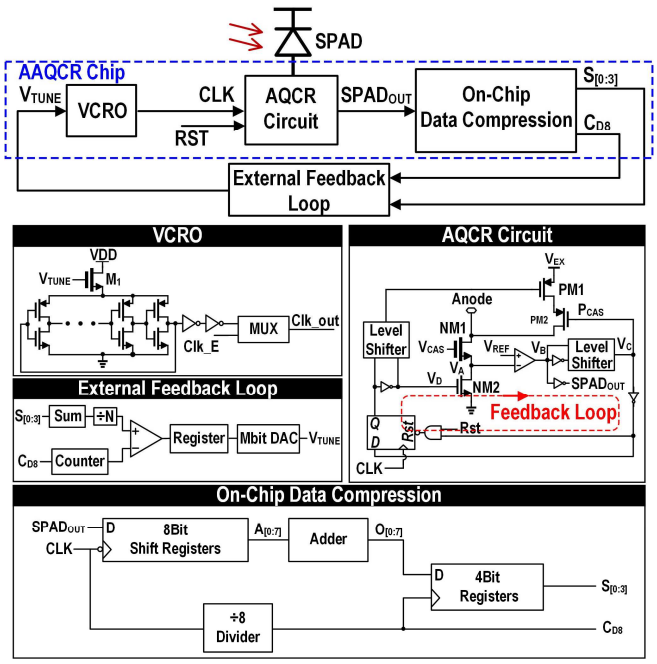

Fig. 4. System structure and detailed schematics of sperate blocks.

B. AQCR Circuit

As shown in Fig. 4, the clock signal is directly applied to the clock terminal of the D-type flip-flop (DFF). Since the DFF is edge sensitive, the input clock duty cycle is not critical. If the SPAD is triggered during the previous cycle, the D terminal of the DFF is HIGH. The recharging process starts at the rising edge of the CLK. When the voltage at node V_A crosses a preset reference threshold voltage (V_{REF}), V_B turns LOW. After a while, the DFF will be reset, thereby disarming the recharge signal. If the SPAD did not trigger a detection event in the preceding cycle, no recharge will be performed (D terminal held LOW). This conditional recharge mechanism eliminates redundant power dissipation in the recharge circuitry. Notably, NM1 is implemented as a thick-oxide transistor to support high excess bias voltages and ensure the reliable operation of the thin-oxide transistor NM2. PM1 and PM2 are used to accelerate the quenching process, which is crucial for efficiently driving external SPAD with high parasitic capacitance.

C. Data Compression Module

In each cycle, the SPAD output is either HIGH or LOW, and the data rate equals to the recharge clock frequency. Consequently, directly outputting the SPAD state of each period require a high-speed interface because the synchronous CLK should be outputted as well for data sampling. To mitigate the output bandwidth requirements, an on-chip data compression unit is implemented. The falling edge of CLK controls shift register which samples the $SPAD_{OUT}$ and generates an 8-bit parallel data word representing the SPAD

status of eight continuous periods. Full adder compresses 8-bit data to 4-bit binary number. Additionally, the clock signal is divided by 8, and the divided clock triggers the sampling of the 4-bit result in a register, thus achieving a three-fold bandwidth reduction.

D. External Feedback Loop Circuit

The external feedback loop comprises a counter, a digital comparator, registers, and a digital-to-analog converter (DAC). The outputs from the data compression module are summed to yield the total SPAD trigger count over a predefined interval. Concurrently, an 8-divided clock signal drives the counter to obtain the corresponding cycle count. The clock cycle counting result is firstly divided by N and then fed to the inputs of the comparator with the SPAD trigger counting result. The value of N is selected based on the desired counting ratio; for example, setting N = 8 corresponds to a count ratio of 12.5% (with a linearity error of 6%, see Fig. 5(b)). The output of the comparator is stored in a register, which drives the DAC to adjust the control voltage V_{TUNE}. This adjustment regulates the VCRO output frequency, causing it to converge to an acceptable range. Since the SPAD triggering process follows a Poisson distribution, the tuning process will be much more accurate with more counting events. The regulating logic employed here is similar to that of a Successive Approximation Register (SAR). Fig. 5(a) and Fig. 5(c) illustrate the flowchart and tuning voltage waveform of the clock frequency regulation process. It should be noted that power consumption is highly related to the recharge clock activity and the parasitic capicitance. A fundamental trade-off exists between power consumption and linearity performance.

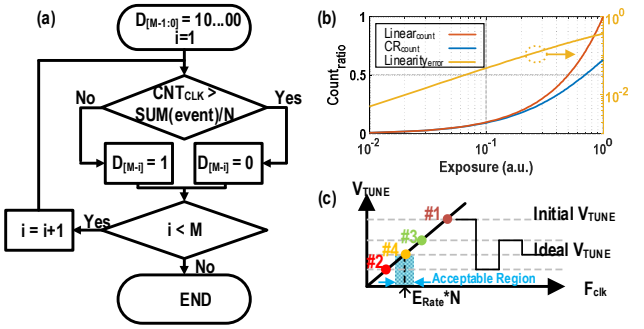

Fig. 5. (a) Flow diagram of the clock frequency regulating process. (b) Counting ratio to normalized input intensity. (c) Waveform of the tuning voltage.

IV. Measurement Results

The SPAD is fabricated and characterized by the proposed AAQCR circuit. The breakdown voltage is defined as the minimum bias voltage required to generate an output pulse minus V_{REF}, which is 22.6 V. It is slightly lower than the previous version [10], possibly due to the increased P^+ junction depth. The PDP measurements over the wavelength range of 450-1000 nm at different excess bias voltages are shown in Fig. 6. It can be observed that BSI process mitigates the standing wave effect caused by multi-layer RDL wiring. Consequently, the PDP varies smoothly with wavelength, exhibiting five PDP valleys. At a 3V excess bias voltage, the PDP achieves a maximum value of 32.5% at a wavelength of 660 nm. The DCR is counted by an oscilloscope (TektronixMS058). Fig. 7 shows the relationship between the DCR and the excess voltage. It is seen that the DCR remains low values which under 1 cps/μm^2 at a V_{ex} from 1 V to 3 V. The jitter is evaluated by a femtosecond laser. A 50 fs laser with an 87 MHz repetition frequency at a wavelength of 793 nm is generated by a Ti-sapphire laser. A fast photodiode (ALPHALAS UPD-35-UVIR, >10 GHz bandwidth) is used as a timing reference. The jitter is shown in the inset of Fig. 7. It is 75 ps at 2.5 V V_{ex}.

To investigate the SPAD output characterization, we measured the buffered SPAD output under controlled illumination using an oscilloscope. The clock frequency is set to 40 MHz in this case, and the falling edge of the clock is set as the oscilloscope trigger. As shown in Fig. 8, the orange regions indicate rising-edge positions (triggered by uncorrelated background light) randomly distributed in one clock period. The violet regions represent falling-edge positions, which is synchronous with the clock rising edges. Notably, the falling edge only occurs in the case of SPAD triggered in the previous period, therefore its probability is lower compared to the blue region.

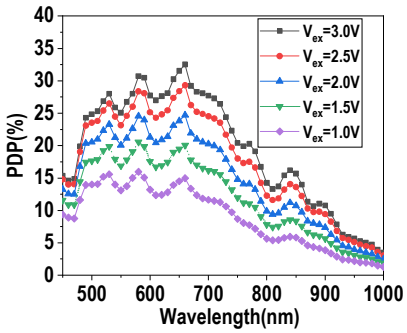

Fig. 6 PDP as a function of the wavelength at five different excess bias voltages.

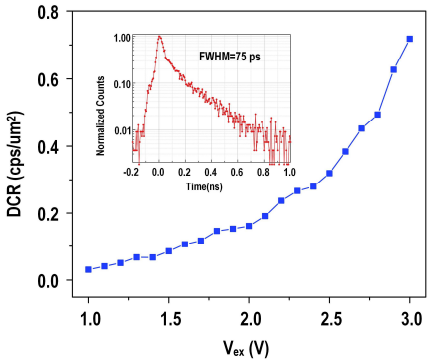

Fig. 7 DCR as a function of the excess bias voltages and jitter performance (inset).

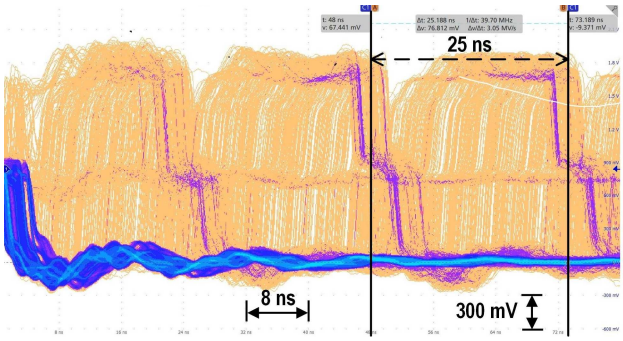

Fig. 8. Waveform of the buffered SPAD output.

Fig. 9 illustrates the measured relationship between the event count rate and the incident photon rate. When the incident photon flux is low, the counting rate increases proportionally with the photon rate. However, under

extremely high photon flux conditions, the SPAD is triggered in every clock cycle, leading to counting saturation. As a result, the maximum achievable counting rate is only limited by the clock frequency.

Table I provides a comparison of characteristics among other state-of-the-art SPADs and QRCs. Compared to other SPADs, the proposed SPAD exhibits superior performance in breakdown voltage, peak PDP, and DCR due to optimized doping profiles and fabrication processes. The most prominent feature of the proposed circuit compared to others is its adaptive functionality. Our circuit enables adaptive adjustment of the recharge clock frequency and recharge pulse width based on incident light intensity and SPAD load. This is a capability absents in existing designs.

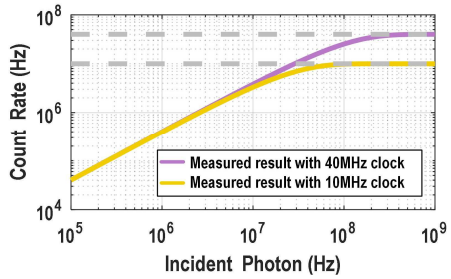

Fig. 9. The relationship diagram between the photon count rate and incident photon rate.

TABLE I COMPARISON OF STATE-OF-THE-ART SPADS AND QRCS

Parameter	SPAD				
	[3]	[4]	[10]	[13]	**This Work**
Process (nm)	55	55	55	65	**55**
V_{BK} (V)	16.1	17.1	26.1	N/A	**22.6**
Peak PDP	82% @425nm	48.9% @450nm	20.3% @660nm	29.5% @660nm	**32.5% @660nm**
DCR (cps/um^2)	44	19.1	19.1	N/A	**0.7**
Parameter	QRC				
	[8]	[11]	[12]	[13]	**This Work**
Process (nm)	22	110	350	40	**180**
QRC type	AQCR	PQAR	AQAR	PQAR	**AAQCR**
SPAD type	Integrated	Integrated	External	Integrated	**External**
Maximum counting rate (Hz)	N/A	200 M	100 M	125 M	**>200 M**
DR adaptation	No	No	No	No	**Yes**
Load adaptation	No	No	No	No	**Yes**

V. CONCLUSION

A BSI SPAD with an external AQCR circuit is presented in this paper. By optimizing the doping profile and fabrication process, a deeper junction depth is achieved, and small pixels with a radius of 2 μm are fabricated. These structural and process modifications extend the optical path length, reduce the DCR, and effectively address the low photon PDP issue in short-wave near-infrared spectroscopy. Furthermore, the proposed AAQCR enables adaptive recharge clock frequency and pulse width adjustment based on incident light intensity and SPAD load through two feedback loops. This functionality provides the circuit with adaptive dynamic range adjustment capability.

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