A 3D-Integrated, 4λ×128Gb/s WDM Si-Photonic Receiver for Chiplet Optical I/O

Sikai Chen[1,3], Nan Qi[1,2,*], Jie Peng[1,2], Haoran Yin[1,2], Menghan Yang[1,2], Minye Zhu[1,2], Yizhou Xu[2], Ruogu Deng[1,2], Guike Li[1,2], Yujun Xie[1,2], Mo Guang[4], Kaiwen Long[4], Jian Liu[1,2], Nanjian Wu[1,2], Zheyu Fang[3], Ming Li[1,2,*] and Liyuan Liu[1,2]
*Email: qinan@semi.ac.cn, ml@semi.ac.cn.
[1]Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China,
[2]University of Chinese Academy of Sciences, Beijing, China,
[3]Peking University, Beijing, China,
[4]Li Auto Inc., Beijing, China.

***Abstract*—We demonstrate a silicon-photonic (SiPh) optical receiver (ORX) for high-density chiplet I/O, consisting of photonic integrated circuits (PIC) 3D-integrated with arrayed CMOS transimpedance amplifiers (TIA). To enable wavelength division multiplexing (WDM) in a single fiber, micro-ring resonators (MRR) are employed to provide high-Q channel filtering, at the expense of degraded signal bandwidth. A wideband linear TIA is proposed with co-designed frequency equalization to enable high Baud-rate reception. Closed-loop monitoring and tuning circuits are integrated to track the wavelength of optical inputs. The TIA is implemented in 28nm CMOS, while the PIC is in 130nm. Experimental results show the proposed receiver achieves 4-wavelength O-to-E reception with 128Gb/s (PAM-4) channel data-rate. The receiving sensitivity reaches -7.3dBm, while consuming 1.04 pJ/bit power.**

Keywords—Optical receiver, silicon photonics, micro-ring resonator, optical I/O, CMOS, TIA, WDM, Chiplets

I. Introduction

Emerging AI computing demands high bandwidth, low-latency, and power efficient interconnects for the scaled-up systems. SiPh technology offers a promising way by fabricating photonic devices on CMOS-compatible process. This enables the integration of optical transceivers into xPU package, and the fiber attachment directly at the chip edge, acting as an optical I/O for data movement. Among various solutions, the micro-ring based transceiver outstands for its compact size, small capacitive loading and intrinsic WDM capability [1-3].

To fit more wavelengths within one free spectral range (FSR) of the resonator, the wavelength spacing needs to be reduced, requiring each MRR to provide sufficient channel selection. However, this introduces a design trade-off between in-channel bandwidth and cross-channel interference. The challenge in MRR filtering lies in balancing two critical performance aspects: the first is achieving a high in-channel bandwidth to support higher data rates and effectively transmit multiple channels, and the second is ensuring strong out-of-band rejection to minimize cross-channel interference. This trade-off is essential for maintaining signal integrity and achieving optimal performance in SiPh ORX.

Previous works have demonstrated MRR ORXs with up to 8 wavelengths and 32Gb/s per-λ data rate [1-3]. Cascaded ring is proposed in [4] to extend the channel BW, but the data rate is still 50Gb/s. This work explores 128Gb/s per-λ WDM and innovates at (1) SiPh high-Q MRRs with closed-loop wavelength control circuits enabling 4λ multiplexing at higher baud rate, (2) CMOS linear TIA incorporating with shunt-series inductive peaking and multi-stage co-designed EQ for extended bandwidth and improved signal integrity, (3) 3D co-packaging of the TIA with SiPh PIC enabling high bandwidth and density.

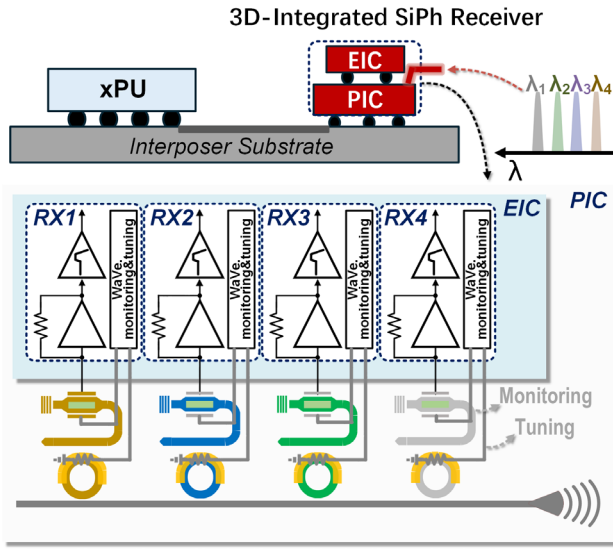

Fig. 1. Architectures of Si-photonic optical receivers with ring resonator and photodetector.

II. Proposed Architecture and Circuit Implementation

Fig. 1 shows the architecture of the SiPh ORX, which integrates MRRs, PDs, and TIAs. Following modulation, wavelengths are input into the PIC via a single-mode fiber. The EIC performs wavelength monitoring and tuning before the MRRs resonate each wavelength into individual PDs for effective signal demultiplexing. To enhance performance, the EIC RX input is strategically positioned directly above the PIC, utilizing copper pillars to minimize parasitic effects when connecting the TIA to the PD. This design contributes to low power consumption and high bandwidth, enabling output through an RF wire-to-board connector.

The PIC features a cascaded array of four silicon MRRs with a 9.6 nm FSR, each separated by a resonance wavelength spacing of 200 GHz, which helps address increasing crosstalk issues that arise with higher data rates. To mitigate crosstalk

This work was supported in part by the Beijing Natural Science Foundation (Funding No. L247013, QY23189), and in part by the National Natural Science Foundation of China (Grant 92373209, 62235017).

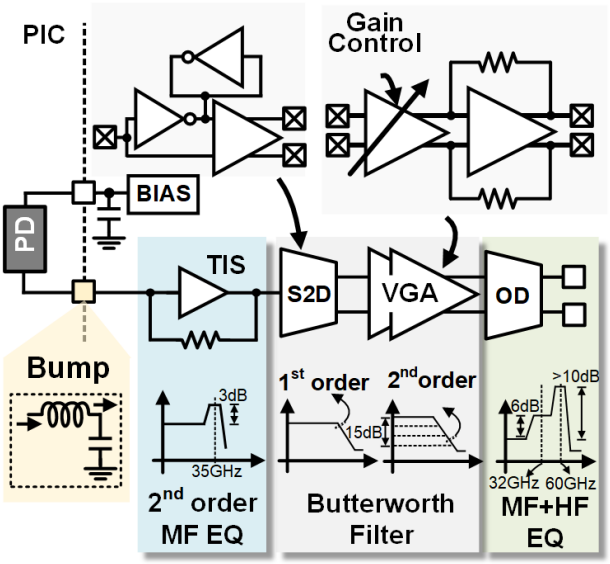

Fig. 2. Simplified schematic of the proposed linear CMOS TIA

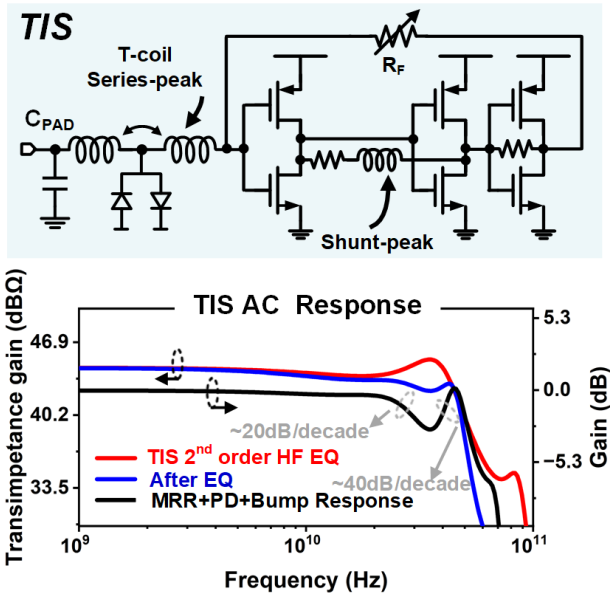

Fig. 3. TIS ac response with 2nd-order equalization at high frequency

from adjacent ORX channels, a higher-Q MRR design is employed, achieving a channel separation of 1.6 nm with crosstalk levels below 15 dB for clearer signal transmission. However, this design choice limits the MRR bandwidth to approximately 50 GHz. The PDs utilize a vertical PIN diode structure, consisting of a 220-nm-thick N-doped silicon layer and a 500-nm-thick P-doped germanium layer, resulting in a bandwidth of approximately 35 GHz for the PDs. Consequently, the insufficient bandwidth of the MRRs and the PDs requires that the EIC implement adequate equalization to optimize ORX link performance.

For wavelength monitoring and tuning, each RX channel continuously monitors the photocurrent at the anode of the RX PD. This photocurrent is amplified by a high-gain transimpedance amplifier and digitized by an 8-bit ADC. An on-chip algorithm adjusts the heater on the PIC to optimize the value of photocurrent. As a result, a channel tuning loop is implemented to align the resonance wavelength of each MRR with the laser grid by maximizing the photocurrent. A 12-bit DAC with resolution redundancy drives the MRR heater, achieving approximately 10 pm wavelength resolution and ensuring precise tuning throughout the operation.

Fig. 2 presents the schematic of the proposed linear TIA, which includes a transimpedance stage (TIS), a Single-to-Differential (S2D) stage, a variable gain amplifier (VGA), and an output driver (OD). The interconnection between the PD and the TIA is established through copper-bump bonding, which plays a crucial role in significantly influencing the overall bandwidth of the TIA.

The total parasitic elements at the RX input are characterized as a 100 fF pad capacitance and an associated inductance of approximately 100 pH. This parasitic capacitance contributes to a first-order roll-off in the electrical response of the PIC. To mitigate this undesirable effect, a series T-coil is inserted, which aids in enhancing the bandwidth of the TIA. However, the frequency response also introduces pronounced in-band gain peaking (exceeding 3 dB) due to parasitic inductance.

As shown in Fig. 3, the overall bandwidth of the PIC is approximately 30 GHz, with a peak gain observed at high frequencies due to the bump. To improve the frequency response of the TIA and reduce group delay variation, the TIS is designed to provide second-order equalization ranging from 3 to 6 dB at 30 GHz. This equalization not only addresses the first-order roll-off but also helps diminish the effects of second-order roll-off, thereby mitigating in-band gain peaking. The subsequent S2D and VGA stages further facilitate both first-order and second-order roll-off. The VGAs provide a variable gain ranging from 0 to 15 dB, ensuring a fixed output amplitude from the TIA. The implementation of a CML OD ensures effective terminal resistance matching, providing approximately 6 dB of gain boost near the Nyquist frequency for channel losses. Additionally, OD contributes over 10 dB of gain enhancement at 60GHz, effectively addressing the higher-order roll-off introduced by the preceding stages.

The proposed multi-stage feedback CMOS TIS employs a shunt inductor in the feedback loop, as shown in Fig. 3. In a traditional inverter-based TIS, the feedforward amplifier is an inverter. However, the proposed TIS features a multi-stage feedback circuit as its feedforward amplifier. Different from the TIS mentioned in [7], the proposed TIS incorporates a parallel inductor in the feedback loop of the feedforward amplifier, allowing it to provide higher bandwidth and gain. With a sufficiently high-bandwidth feedforward amplifier and the feedback resistor R_F, the stage allows for second-order equalization. The second-order equalization of the TIS minimizes in-band gain peaking and equalizes the PIC's electrical response, achieving a roll-off of 40 dB/dec with a -40 dB/dec amplitude slope.

To validate the effectiveness of the proposed TIA architecture in overcoming the bandwidth limitations imposed by MRRs, extensive simulations were conducted, as shown in Fig. 3. However, after applying the equalization techniques, the combined bandwidth of the PIC and TIS is improved to over 45 GHz, demonstrating a significant enhancement. Furthermore, the ripple within the passband is well-controlled, maintaining a level below 0.5 dB.

III. Measurement Results

The 3D co-packaging of the TIA with SiPh PIC enables high bandwidth, increased integration density, and improved overall performance. By vertically integrating the TIA and PIC, this design minimizes signal path lengths, effectively reducing latency and power consumption. Additionally, efficient thermal management is achieved as heat generated by the TIA is dissipated through the packaging structure.

As shown in Fig. 4, the 3D-integrated ORX comprises an EIC and a PIC. The EIC is fabricated using a 28 nm bulk CMOS process, allowing for high integration density. It is flip-chip attached to the PIC with copper pillars, ensuring minimal loss at the electrical and optical interfaces. Fig. 4 (a) also depicts the die micrograph of the four-stage TIA chip, which occupies a compact area of only 0.208 mm² and includes an integrated wavelength tuning control unit. Fig. 4 (b) shows the co-packaged and fiber-terminated 4-channel MRR-based optical RX system. The 4-λ WDM signal is launched from a single-mode fiber into the PIC via free-space coupling, and the RX then outputs through a connector, incurring channel losses of approximately 6 dB.

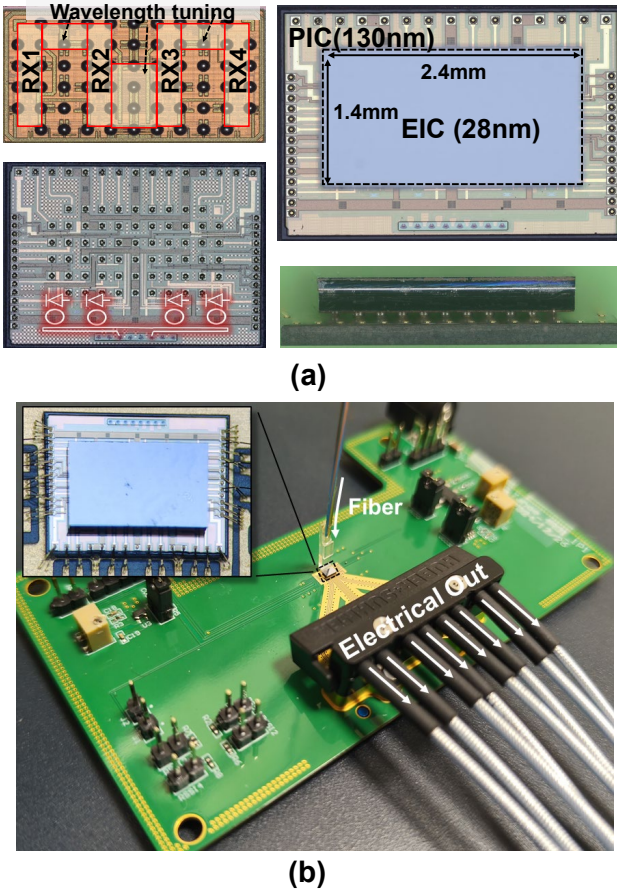

Fig. 4. (a)28nm CMOS EIC and 130nm PIC micrographs. (b) Flip-chip integrated optical receiver demonstrator with attached fiber array

Fig. 5(a) demonstrates the optical spectrum of the MRRs, showcasing a 3 dB bandwidth of 0.39 nm, which corresponds to 50 GHz. The spectrum also reveals adjacent band aliasing, with a rejection level below -15 dB at a wavelength gap of 1.6 nm. The MRR + PD were evaluated using probe and exhibited a bandwidth of 23 GHz. Following equalization by the TIA, the overall ORX achieves an enhanced bandwidth of 37 GHz,

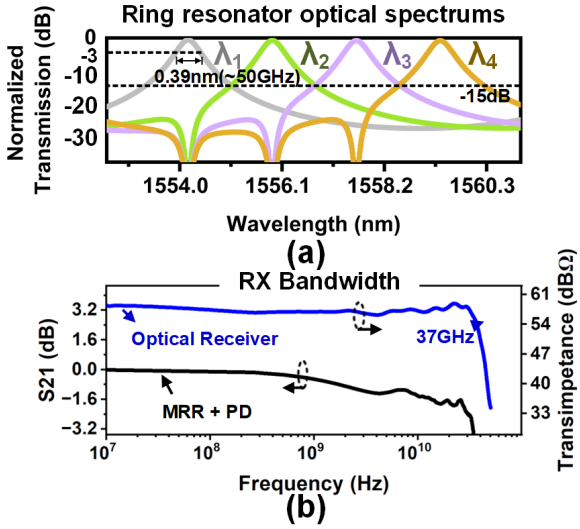

Fig. 5. Measured the RX (a) filtering responses for single-ring, (b) transimpedance gain extracted using S-parameters.

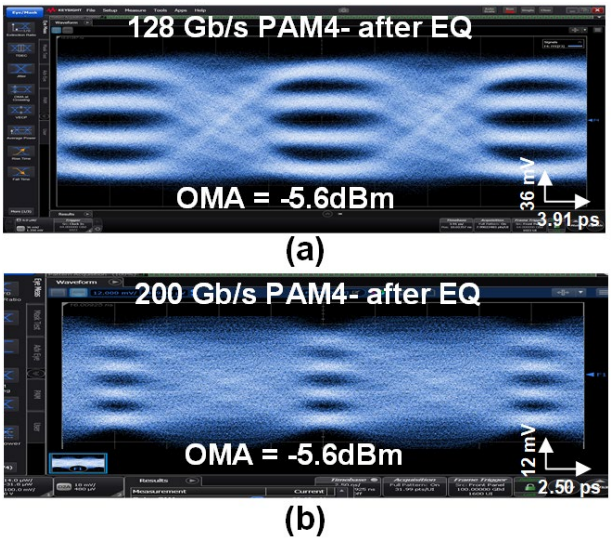

Fig. 6. Measured RX' PRBS10 output (a)128 Gb/s PAM4 eye after 4-tap FFE and 3-tap DFE and (b) 200 Gb/s PAM4 eye after 7-tap FFE and 5-tap DFE

along with a transimpedance gain of 58 dBΩ, as illustrated in Fig. 5(b).

Fig. 6 shows the PAM4 eye diagrams from the through setup (without a DUT) used for calibration. In Fig. 6(a), the 128 Gb/s PAM4 eye diagram (after 4-tap FFE and 3-tap DFE equalization) has an OMA of -5.6 dBm. Fig. 6(b) highlights the potential of the ORX, demonstrating 200 Gb/s PAM4 performance at an input OMA of -5.6 dBm, utilizing GSSG probes.

In the measurements, λ1, λ2, λ3, and λ4 are generated using a tunable laser source. The four wavelengths, after passing through MRMs, are input into the PIC via a single-mode fiber. After thermal tuning, the MRRs resonate λ1, λ2, λ3, and λ4 into the PDs. Fig. 7 shows the RX output eye diagram when a 4×128 Gb/s WDM input is formed by four TX channels modulated at 128 Gb/s with PRBS10 data.

Fig. 8 shows the measured PAM-4 BER as a function of input OMA at 112Gb/s channel speed, demonstrating –8.2 dBm sensitivity defined by the KP4-FEC limit. The sensitivity degrades to –7.3 dBm at 128 Gb/s PAM-4 input.

Fig. 9 shows the power breakdown for each TIA stage, with a total TIA power of 132.5 mW. In particular, the TIS accounts for 12.3%, the S2D+VGA (providing equalization and gain) uses 46.2%, the OD consumes 22.9%, and Wavelength tuning unit accounts for 8.7%.

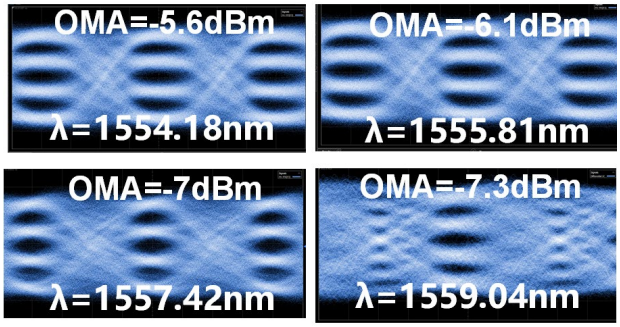

Fig. 7. RX output eye diagram measured for each of the four wavelengths input

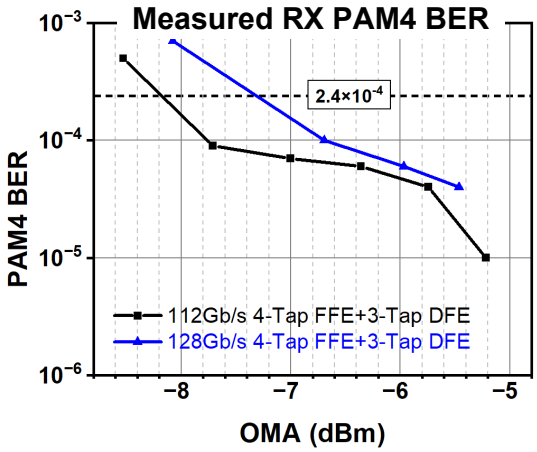

Fig. 8. Measured PAM4 BER across input OMA with 112Gb/s PAM4, 128Gb/s PAM4 input.

TABLE I. COMPARISON WITH STATE-OF-THE-ART OPTICAL RECEIVER

	This work	[2]	[4]	[5]	[6]
Technology	**28nm CMOS**	28nm CMOS	7nm CMOS	28nm CMOS	16nm CMOS
Data Rate and Modulation	**128 Gb/s PAM4**	32 Gb/s NRZ	50 Gb/s NRZ	112 Gb/s PAM4	112 Gb/s PAM4
Wavelengths	**4**	8	7	1	1
Lambda Spacing (nm)	**1.6**	1.2**	1.5	N/A	1
PD Cap (fF)	**80**	N/A	60	70	N/A
PD Resp. (A/W)	**0.9**	N/A	0.9	0.5	60
sensitivity (dBm)	**-7.3**	-10	-11.4	-5.1*	0.6
Power Efficiency (pJ/bit)	**1.04@ 128Gb/s** / **0.66@ 200Gb/s**	3.8	0.96	0.96	1.4
TIA Total Area (mm^2)	**0.208**	0.5***	0.031	0.558***	0.12***

*Simulated **Estimated from the plots *** Estimated from the micrograph

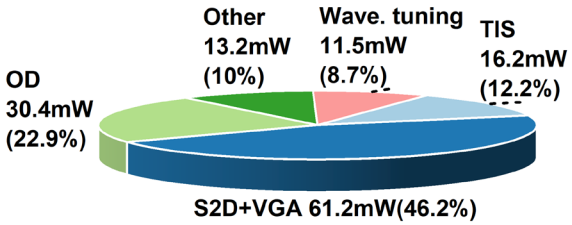

Fig. 9. Power breakdown of each TIA stage.

Under Table I, the total TIA power consumption for each stage sums to 132.5 mW. Compared to [5] and [6], our design supports 4λ reception at 1.6 nm spacing and achieves higher speed than [2] and [4].

IV. CONCLUSION

We have demonstrated a 3D-integrated, heterogeneously integrated C-band WDM Si-Ph receiver for xPU package interconnections. This ORX incorporates all the critical electrical and optical components required for WDM links, including a C-band SiPh MRR array with 200 GHz channel spacing. The electrical data path features an energy-efficient, high-swing PAM-4 TIA design in 28 nm CMOS. The CMOS IC also provides background wavelength control tuning, which is critical for robust WDM operation with ring resonators. Our high-speed link measurements show simultaneous PAM-4 transmission over four wavelengths at 128 Gbps/λ with an OMA of -7.3 dBm.

REFERENCES

[1] C. Sun, D. Jeonget, M. Zhang, W. Bae, C. Zhang et al., "TeraPHY: An O-band WDM Electro-optic Platform for Low Power, Terabit/s Optical I/O," VLSIc, 2020.

[2] Z. Xuan, G. Balamurugan, D. Huang, R. Kumar, J. Sharma, C. Levy et al., "A 256 Gbps Heterogeneously Integrated Silicon Photonic Microring-based DWDM Receiver Suitable for In-Package Optical I/O," VLSI, 2023.

[3] P. Bhargava, D. Jeong, E. Jan, D. Van Orden , D. Kita, H. Gevorgyan et al., "A 256Gbps Microring-Based WDM Transceiver with Error-Free Wide Temperature Operation for Co-Packaged Optical I/O Chiplets," 2024 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), Honolulu, HI, USA, 2024, pp. 1-2.

[4] M. Raj, C. Xie, A. Bekele, A. Chou, W. Zhang, Y. Cao et al., "A O.96pJ/b 7 × 50Gb/s-per-Fiber WDM Receiver with Stacked 7nm CMOS and 45nm Silicon Photonic Dies," ISSCC, 2023.

[5] H. Li, G. Balamurugan, J. Jaussi, B. Casper,"A 112 Gb/s PAM4 Linear TIA with 0.96 pJ/bit Energy Efficiency in 28 nm CMOS," ESSCIRC 2018.

[6] D. Patel, A. Sharif-Bakhtiar, A. C. Carusone, "A 112-Gb/s -8.2-dBm Sensitivity 4-PAM Linear TIA in 16-nm CMOS With Co-Packaged Photodiodes," JSSC, 2023.

[7] S. Chen et al., "A 2λ×100 Gb/s Optical Receiver with Si-Photonic Micro-Ring Resonator and Photo-Detector for DWDM Optical-IO," 2024 IEEE Custom Integrated Circuits Conference (CICC), Denver, CO, USA, pp. 1-2, 2024.