A 141GΩ Input Impedance Frontend IC for Biopotential Recordings with a Customized I/O Device Shielding Parasitic Capacitance

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***Abstract*—This paper proposed a low-power, high-input impedance (Z_{in}) frontend IC for biopotential readout, including two frontend amplifiers and a $\Delta^2\Sigma$ modulator. A customized I/O device by inserting and driving an additional metal plate underneath the original contact pad is exploited to shield the parasitic capacitance. Moreover, a flipped voltage follower-based core amplifier and quiet chopping scheme are used to minimize the parasitic capacitance of the readout circuit. The power consumption is minimized both in current and voltage domain. In the frontend amplifier, a signal-dependent dynamic bias scheme is proposed to support large signal amplitude with a low quiescent current. In the following delta-delta sigma modulator, a merged feedback scheme is deployed to limit the amplitude of the integrator output, allowing using a lower supply voltage. The proposed readout IC is implemented in a standard 55nm CMOS technology, with an active area of 0.12mm^2. It achieves a Z_{in} of 10.8GΩ@50Hz while consuming only 29.6μW. The frontend IC features an input referred noise of 2.5μVrms in 500Hz bandwidth and provides an SNDR of 81.2dB. It is validated with on-body electrocardiogram (ECG) and electromyogram (EMG) measurements with dry electrodes.**

Keywords—biopotential, frontend amplifier, customized I/O, input impedance, delta-delta sigma modulator

I. INTRODUCTION

Wearable monitoring of bio-potential signals, e.g. electrocardiogram (ECG), electroencephalogram (EEG) and electromyogram (EMG) is proven to be useful in improving the healthcare of human beings at a reasonable cost [1-4]. Compared with conventional Ag/AgCl electrodes requiring skin preparation, dry-electrodes and capacitively coupled electrodes can provide a comfortable and unobtrusive biopotential measurement [4-5]. A high input impedance (Z_{in}) is of significant importance for readout IC with these electrodes for better signal quality and interference rejection. Meanwhile, a large input dynamic range is required to copy with electrode DC offset (EDO) and motion artefacts, while a low power is beneficial for a long battery lifetime.

Existing solutions usually employ an instrumentation amplifier (IA) and an ADC. As shown in Fig. 1 (a) and (b), there is always a trade-off between the input range (the EDO cancellation in case of DC coupling), the gain of the amplifier, and the resolution of the ADC. A programmable gain amplifier (PGA) is referred to allow a large input signal while a high resolution of ADC is required, increasing the power [3][5-6]. A ΔΣ style direction conversion scheme with IA embedded (Fig.1 (c)), is considered in [7-9], where a reconstructed input is fed back and subtracted from the input,

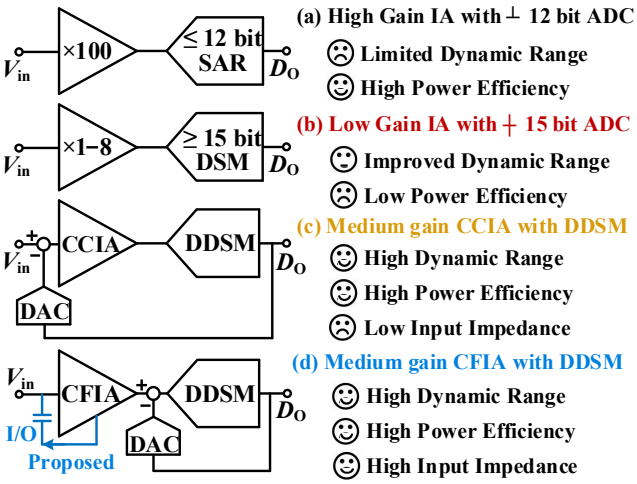

Fig. 1 Architectures of Biopotential readout frontends (a)(b) IA+ADC, (c) CCIA with DDSM, (d) CFIA with DDSM

i.e. a $\Delta^2\Sigma$ modulator (DDSM), increasing the input dynamic range. However, a capacitive coupled IA (CCIA), usually used in DDSM, leads to a limited Z_{in}, while current feedback amplifier (CFIA) can provide a much higher value. Though the Z_{in} of CFIA is intrinsically high, the parasitic capacitance of the I/O devices remains and the power is relatively high.

This paper proposed a frontend IC with a customized I/O device shielding parasitic capacitance on chip, together with a low input capacitance CFIA. As shown in Fig.1 (d), it employs a CFIA followed by a DDSM, thus achieving a high Z_{in} and a large input range at the same time. The power consumption is optimized on both system and circuit level. On system level, the reconstructed signal from the DDSM is fed back to the amplifier output, instead of the input, and thus reduces the complexity and the power of the CFIA, compared to [9]. On circuit level, a signal dependent biasing scheme is proposed for the CFIA to support a large signal amplitude with a low quiescent current. Moreover, a merged feedback scheme together with an IIR filter controlled 5-bit DAC is exploited in the DDSM to reduce the internal signal amplitude, allowing using a 1.0V supply. The proposed frontend IC is implemented in a 55nm CMOS technology with an active area of 0.12mm^2. It achieves a Z_{in} of 10.8GOhm at 50Hz, while providing a channel SNDR of 81.2dB in 500Hz bandwidth with only 29.6μW power.

The rest of the paper is organized as follows: in section II, the proposed amplifier topology is explained and compared with predecessors. In section III, the implementation of the

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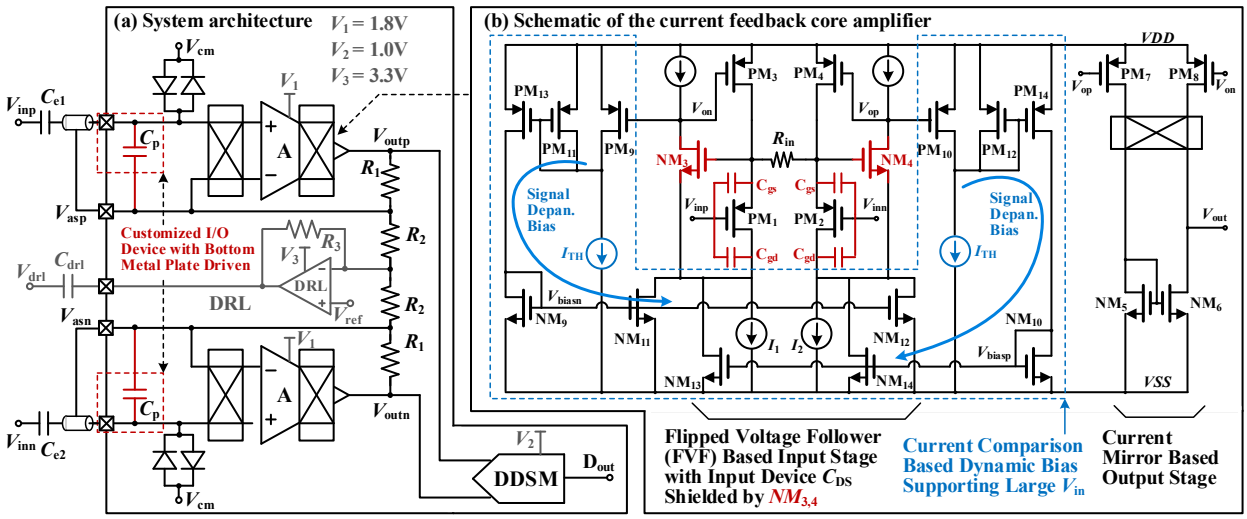

Fig. 2 The proposed frontend IC (a) System architecture (b) Schematic of the CFIA as the core of frontend amplifier

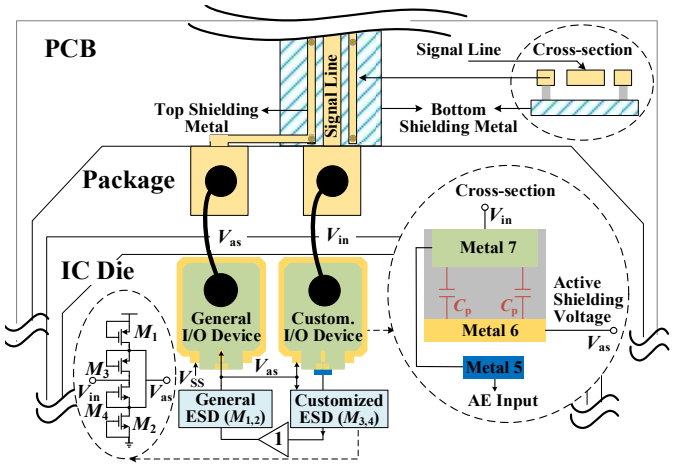

Fig. 3 The customized I/O device shielding the parasitic cap. on chip and PCB

multiple bit DDSM is presented. Experimental results are given in section IV and conclusions are drawn in section V.

II. The Proposed Low Power, High Z_{IN} Amplifier

Fig.2 (a) shows the proposed low power, high Z_{in} frontend, including two CFIAs in resistive feedback configuration, defining the amplifier gain, i.e. R_2+R_1/R_2. It also includes a driven-right-leg (DRL) amplifier to provide a low-impedance node to reject common mode interference [5,10]. The feedback node of the CFIA (V_{as}) is also used to drive the metal plate underneath the top metal of the customized I/O device as well as the shielding metal plate/trace on PCB. The following DDSM convert the signal to a 5-bit digital code. There are three different supply voltages for the CFIA (1.8V), the DRL amplifier (3.3V) and the DDSM together with digital circuit (1.0V), for power minimization. The heterogeneous techniques for impedance boosting are discussed in subsection A and power optimization of the CFIA by dynamic biasing is presented in subsection B.

A. Input impedance boosted CFIA and customized I/O

The proposed CFIA is shown in Fig,2(b), as the core of the feedback amplifier. A flipped voltage follower (FVF) based input stage is used, which converts the input voltage to current through $PM_{3,4}$. This small signal current is copied to the output stage and generate V_{out}. There are four different techniques employed to boost the Z_{in}.

First of all, with the FVF based implementation of CFIA, the C_{gs} of input devices is nulled by the differential source follower style operation where the gate of the $NM_{3,4}$ device follows V_{inp} and V_{inn}. Moreover, the C_{gd} is also minimized because the drain of $PM_{1,2}$ follows the gate of $NM_{3,4}$ and thus also follows V_{inp} and V_{inn}. Secondly, a quiet chopping scheme is used, where the differential voltage between the positive and negative input of the CFIA is very small, reducing the effective input capacitance at node V_{inp} and V_{inn} by $1/(1+A)$, where A is the gain of the CFIA. By chopping with f_{chop} at the input of the CFIA, the Z_{in} can be maintained at $A/2\pi f_{chop}C_p$, where C_p is the parasitic capacitance of the CFIA input, already minimized by the FVF.

With the aforementioned two techniques, the Z_{in} at CFIA input can be already boosted to 150Gohm at 10Hz, assuming a C_p of 10fF, a gain of 100 and an f_{chop} of 10kHz. In this case, the parasitic effect of the I/O device and the PCB will be the bottleneck for increasing the Z_{in}. Therefore, as the third technique, a customized I/O device is introduced, as shown in Fig. 3. The bonding wire is connected to the top metal plate as usual, while the metal plate underneath it (Metal 6) is actively driven by a shielding voltage V_{as} to cancel the effect of parasitic MIM capacitor. The signal is connected to metal 5 with a much smaller metal area, avoiding reducing the Z_{in}. Moreover, the ESD device $M_{3,4}$ for the customized I/O is also driven by the same V_{as}, cancelling its parasitic capacitance. These two deivces are sandwiched in the common ESD device $M_{1,2}$ of the I/O device beside it, which is shown as general I/O in Fig.3. In case of a charging/discharging event, the excess charge can still be released through $M_{1,3}$ or $M_{2,4}$.

Finally, the parasitic effect of the PCB can be minimized by shielding the signal trace with V_{as}, which approximately equals to V_{in}. Thanks to these boosting techniques, the Z_{in} of the amplifier is made beyond the state-of-the-art.

B. Signal-dependent dynamic biasing scheme

As shown in Fig.2(a), the CFIA needs to drive $R_{1,2}$ resistors, which can contribute to the input noise. Thus, it is optimal to use 100kohm level resistance. Assuming a 0.5V differential input, it requires a 5μA output current from CFIA, increasing its power. Since the CFIA employs a power

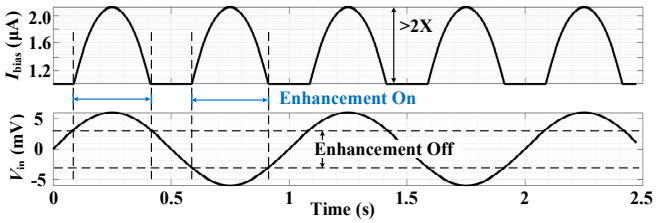

Fig. 4 Simulation of input signal and dynamic biasing current of the CFIA

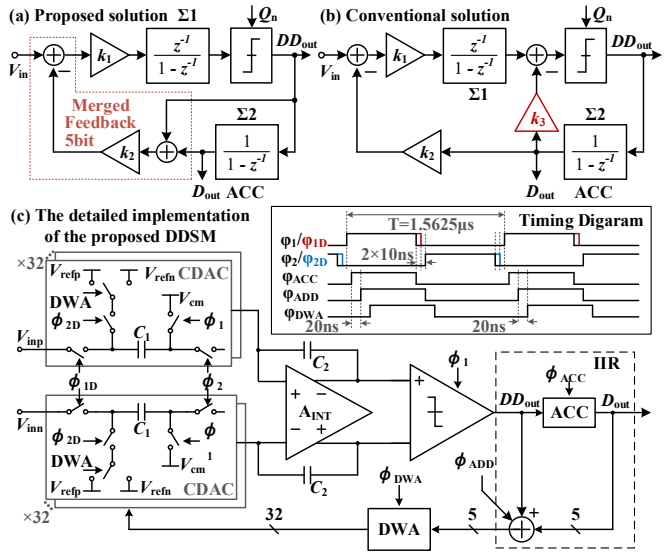

Fig. 5 (a) Proposed DDSM with merged feedback (b) Conventional DDSM (c) Detailed implementation of the proposed DDSM with timing diagram

consuming class-A output stage, a signal dependent biasing scheme is proposed.

This biasing scheme includes a current-comparison branch, consisting of $PM_{9,10}$, I_{TH} and an enhancing branch, consisting of $PM_{11,12,13,14}$ and $NM_{9,10,13,14}$ at both sides of the inputs, as shown in Fig. 2 (b). During operation, when the signal amplitude is within $(I_{PM3,4}\text{-}I_{TH})\cdot R_{in}$, there is no current flowing in $PM_{11,12}$, where $I_{PM3,4}$ is the quiescent bias current. Assuming a 1:1 ratio of $I_{PM9,10}/I_{PM3,4}$, when the signal amplitude becomes higher, making the current in either PM_9 or PM_{10} lower than $I_{PM3,4}\text{-}I_{TH}$, the enhancement is thus enabled. It can keep the current in $PM_{3,4}$ constant to avoid their cut-off and provide a large output current. The simulation result with an open-loop CFIA is shown in Fig. 4 including the differential input voltage and the combined current in $NM_{11,13}$, I_1 and $NM_{12,14}$, I_2. It can be observed that, an output current of >2μA can be provided with a quiescent bias of only 1μA.

III. The Low Voltage DDS Modulator

A. DDS Modulator with a merged feedback

A discrete-time (DT) multiple-bit feedback DDSM with a merged feedback is proposed as shown in Fig. 5 (a), while the conventional DDSM is shown in Fig. 5(b). Since the output of the feedback DAC equals to $V_{in}[n\text{-}1]$, subtracting it from the input can eliminate EDO from the system and thus increase the dynamic range. Moreover, the system employs a 5-bit DAC controlled by an IIR filter, with transfer function $(2\text{-}z^{-1})/(1\text{-}z^{-1})$, reducing the quantization noise [11]. There are two advantages of this modulator, as shown in Fig. 5 (c) with more details, compared to the conventional solutions.

First, this solution requires only one DAC, while the conventional solution needs to use two of them, reducing the complexity and chip area. Second, the merged feedback

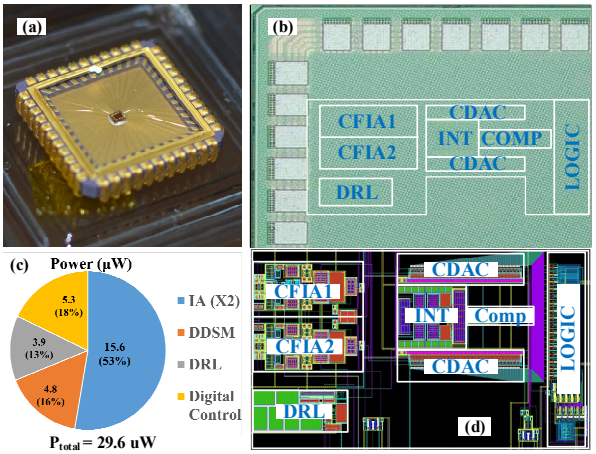

Fig. 6 (a) The packed chip (b) The die-photo including metal fillings (c) The power distribution of the proposed fronted IC (d) The layout

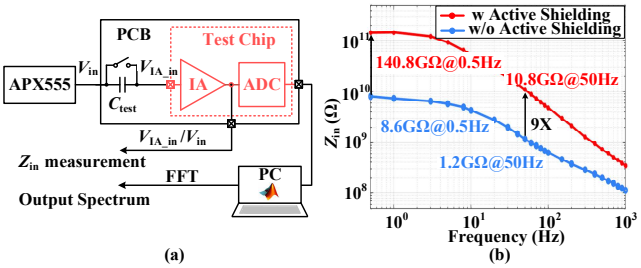

Fig. 7 (a) The input impedance measurement setup (b) The measured input impedance at different frequency

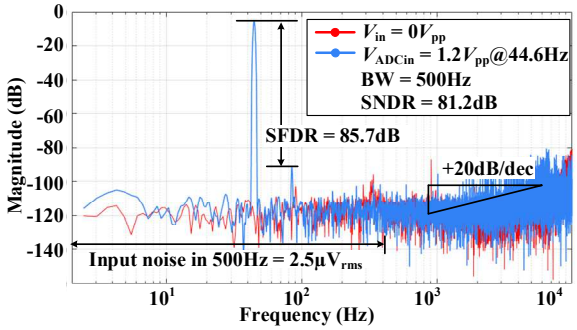

Fig. 8 The measured input referred noise spectrum and power spectrum with a 96mV$_{pp}$ input signal at CFIA input (1.2 V$_{pp}$ at ADC input)

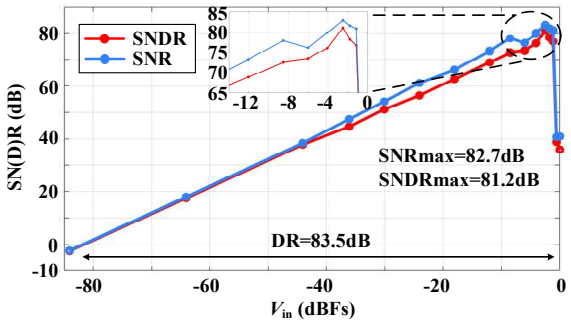

Fig. 9 The measured (with IA) SNR, SNDR and DR across the input range

signal can follow the input more accurately, and together with the 5-bit DAC, it reduces the amplitude of the integrator by around 60%. During operation, the signal amplitude is merely 200mV$_{pp}$ at this node, allowing use a 1.0V supply for the DDSM, the same as the digital circuit, to reduce the power.

TABLE I PERFORMANCE SUMMARY AND COMPARISON

Parameter	**This Work**	JSSC 15[1]	ISSCC 18[12]	TBCAS 19[5]	JSSC 20[8]	ESSCIRC 23[13]	JSSC 24[14]
Technology (nm)	**55**	180	40	180	180	180	180
Supply Voltage (V)	**3.3/1.8 /1**	1.2	1.2	5	1.2	1.8	3/1.8
Topology	**IA+DT Δ-ΔΣM**	IA+DT ΔΣM	IA+CT ΔΣM	IA[#]	DT Δ-ΔΣM	CT-DT Δ-ΔΣM	Two-step ΔM
Z_{in} (Ω)	**140.8G@DC**	-	1.5G@DC	400G@DC	1.465G@DC	-	26G@DC
	10.8G@50Hz	500M@50Hz	1G@50Hz	4G@50Hz	-	11G@10Hz	1.25G@50Hz
Input Noise (μVrms)	**2.5 (0.5-500Hz)**	0.62 (500Hz)	6.35 (0.1-5kHz)	3.7 (0.5-100Hz)	1.6 (1-500Hz)	4.27 (500Hz)	2.2 (0.5-125Hz)
Peak SNDR (dB)	**81.2**	84.3/(SNR)	78	-	69.7	87	102
CMRR (dB)	**81**	110	-	70	**>** 70	80	86
Input Range (mV_{pp})	**250/500**	30	200	220	-	700	3560
Power (μW)	**29.6**	56	7.3	155	1.7	88.4	67
Channel area (mm^2)	**0.12**	7	0.11	0.44	0.023	0.83	1.2

*IA gain = 12.5/6.25, [#]Only IA included

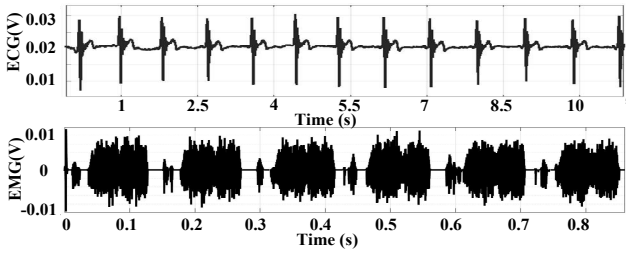

Fig. 10 On-body measured ECG and EEG waveforms by dry electrodes

B. Digital Control Circuits

The proposed DDSM requires an accumulator (ACC), an adder, a data weighted averaging (DWA) controller and a timing signal generator. The ACC is a rising-edge triggered 5 bits up-down counter, while triggered, it adds one to the output. The adder generates 5 bits output from the ACC and the comparator output, and it keeps the value once the upper or lower limits are reached. A 5-bit CDAC is used with DWA to improve the linearity of the modulator.

IV. IMPLEMENTATION RESULTS

The proposed Frontend IC is implemented in a standard 55nm CMOS technology and characterized experimentally. The packaged and naked die-photo of the chip is shown in Fig. 6 (a)(b), the power consumption is shown in (c) and the layout is shown in (d), respectively. Fig. 7 shows the measured Z_{in} of the frontend, with 140.8GOhm@DC, 52.3GOhm@10Hz and 10.8GOhm@50Hz. Fig. 8 shows the measurement input referred noise spectrum and power spectrum with a $96mV_{pp}$ input signal at the CFIA input, achieving a channel SNR of 82.7dB and a SNDR of 81.2dB. Fig. 9 shows the measured SNR and SNDR across the input range, the distortion increases drastically beyond ~$1.3V_{pp}$. Fig.10 shows the measured ECG and EEG waveforms with dry electrodes, validating the proposed frontend IC.

V. BENCHMARKING AND CONCLUSION

The performance of the proposed frontend IC is summarized and compared to the state-of-the-art in Table I. The proposed amplifier achieves a 10.8GOhm Z_{in} at 50Hz, which advances the state-of-the-art, thanks to the proposed booting techniques including the use of a customized I/O. The achieved SNDR and input referred noise are in line with other works while both the power consumption of 29.6μW and the channel area of $0.12mm^2$ are among the lowest. The supported input range is sufficient and it can be further increased if a lower gain in the amplifier is used. The excellent performance including the Z_{in}, resolution and power consumption makes the proposed frontend IC suitable for wearable bio-potential readout with dry or capacitive electrodes.

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