A 60V Chopper Instrumentation Amplifier with 54V/µs Common-Mode Transient Tolerance and 115dB DR for High-Side Current Sensing

Runhao Zhang, Shiqi Zhang, Shen Ye, Kaiwen Zhou, Zhiliang Hong and Jiawei Xu
State Key Laboratory of Integrated Chips and Systems, Fudan University, Shanghai, China.
Email: jwxu@fudan.edu.cn

***Abstract*—This paper presents a high-voltage instrumentation amplifier (HV-IA) for high-side current sensing. To achieve low noise while improving the common-mode (CM) transient tolerance, the IA utilizes a HV transient-tailored (HV-TT) PMOS input pair, as well as a bidirectional transient level shifter (BTS) in the input chopper, achieving a CM transient tolerance of 54V/µs across a wide input CM voltage range of 0.7V-56.3V. Furthermore, the CM-input-dependent gain error, caused by the input CM voltage variations, is reduced to ±0.2% by employing a segmented gain adjustment technique. Last, to extend the current sensing range, the IA uses an automatic gain control (AGC) loop to achieve a cross-scale dynamic range (DR) of 115dB. Fabricated in a 0.18µm BCD process, the HV-IA exhibits 19nV/√Hz input referred noise, 140dB CMRR and 10µV offset, while consuming 305µA from a 60V/4.2V dual power supply.**

***Keywords*—high-voltage, instrumentation amplifier, current sensing, common-mode transient, automatic gain control (AGC), chopping, dynamic range (DR).**

I. Introduction

Accurate high-side current sensing with wide dynamic range (DR) has been widely used in solenoid control, battery chargers, and overcurrent protection. In particular, high-side sensing is a preferable solution when minimal ground disturbances and load-short detection are necessary. However, the main challenge of high-side sensing is the high common-mode (CM) voltage that the instrumentation amplifier (IA) can withstand [1]. In addition, high-slew-rate CM disturbances, such as the switching of PWM motor drive, short circuit faults in the power distribution system, and battery discharging, requires the IA to respond quickly to CM transients to avoid signal delays or distortion. Last but not least, high DR and low noise are required to handle potentially significant changes in load current while capturing small current changes for precise closed-loop control.

State-of-the-art high voltage IAs (HV-IAs) tend to employ low-voltage (LV) devices to optimize speed and chip area. The isolation between HV CM input signal and LV devices can be implemented by capacitive coupling [2]-[5] or cascode DMOS protection [6][7]. Nevertheless, limited CM transient response is still one of the bottlenecks. Even with the HV-CM feedforward loop [5], chopper-stabilized capacitive-coupled amplifiers may not able to tolerate fast-varying HV-CM transients. In contrast, the current-balancing instrumentation amplifier (CBIA) [7] can convert signals between input transconductance (TC) stage and

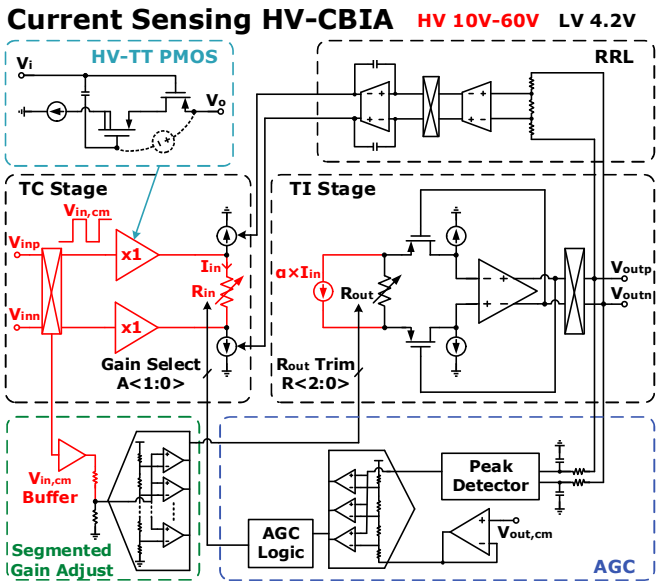

Fig. 1. Architecture of the proposed HV-CBIA

output transimpedance (TI) stage by means of current, providing higher slew rate to tolerate transient CM voltage, while its open-loop architecture ensures excellent bandwidth-power efficiency. A recent reported chopping CBIA [7] verifies its feasibility in HV applications by employing adaptive input bias and HV input chopper.

For high side current sensing, however, the ability to respond large and fast CM transients in a HV environment remains one of the necessary features that CBIA lacks, especially when input chopping is present. Meanwhile, to accommodate both standby and peak current sense, the CBIA must have a wide DR without compromising the noise and linear input range.

This paper presents a CM-transient tolerant chopping CBIA (Fig.1) that uses a bidirectional transient level shifter (BTS) in the input chopper and a HV transient-tailored (HV-TT) PMOS input pair, respectively, to enhance their immunity to HV CM transients, enabling a wide input common-mode voltage range of 0.7V to 56.3V. The voltage gain error caused by CM fluctuations is compensated by a segmented gain adjustment scheme. Finally, according to the output signal amplitude, the input resistor and CBIA gain can be dynamically adjusted by an

automatic gain control (AGC) loop to achieve 115dB DR while retaining a nearly constant SNR.

II. System Architecture

Fig. 1 shows the proposed HV-CBIA. The modulated input voltage is buffered and converted into a balanced current I_{in} on R_{in}. The replicated current flows through R_{out} to generate the output voltage. A differential source-input buffer is used to improve the drive capability of the CBIA with moderate noise contribution [7]. A ripple reduction loop (RRL) extracts output ripple and feeds back a compensation current to null the CBIA offset before it is up-modulated.

A. HV Input Chopper

Conventional HV chopper may experience breakdown in the presence of HV CM transients. A clamp protection [2] can help, but the control logic of the chopper switch will also be disturbed by the CM transient. In contrast, we propose a BTS-based HV chopper (Fig. 2) that can withstand both rising and falling HV CM transients while ensuring a correct control logic of chopper switches. This technique maintains great signal integrity without introducing large spikes during HV CM transients.

As shown in Fig.2 (bottom right), the HV clock generator utilizes a capacitively coupling latch [2], where its local supply and ground (V_{max} and V_{min}) are generated by the BTS, shown in the bottom left of Fig.2. The BTS extends a conventional source follower path (M_{p1}, M_{n1}) with two complementary fast-charging branches (FCB), consisting of M_{p2}, C_{f2} and M_{n2}, C_{f1}. In case of a falling CM transient, though M_{n1} fails to pull down V_{max}, M_{p2} can generate an instantaneous large current through C_{f2}, quickly lowering V_{max}. Similar principles apply to M_{n2} and C_{f1} when CM transient rises. The BTS provides high slew rate for fast rising or falling CM transient, and the steady-state voltages of V_{max} and V_{min} remain not affected. Therefore, the HV chopping clock can closely follow the input CM without corrupting the chopping during CM transients. In addition, series Schottky barrier diodes (SBDs) clamp the V_{ds} of chopper switches to prevent accidental breakdown.

B. High-Voltage CM-Transient Tolerant CBIA

The middle and bottom of Fig.3 show the TC and TI stages of the HV-CBIA, respectively. In the TC, two flipped-voltage-followers (FVF) convert the input voltage into a current, which is replicated to the output via $M_{p3\text{-}6}$. To get better matching and low offset, a LV CMOS input pair rather than DMOS is used. However, since the maximum common-mode voltage range can go up to around 55V, the drain of M_{p1} and M_{p1} have to be float biased. However, conventional floating bias circuits are usually unable to handle fast CM transients beyond 10V/µs.

In this work, a compound HV-TT PMOS is proposed as the input pair (Fig. 3, top left). It ensures a wide CM voltage range, maintains excellent matching, and handles bidirectional HV CM transients effectively. In this structure, both M_1 and M_3 are LV 5V PMOS, protected by DMOS M_2 and M_4. In the steady state, M_4 detects the voltage at nodes A and B and ensures a fixed V_{ds} for M_1 through M_2 and M_3. Although M_4 can quickly pull up its source but lacking the pull-down capability, this is risky for HV falling transients. Therefore, C_1 is utilized as a feedforward path to pull down the gate voltage of M_2, generating an instantaneous large current to discharge the parasitic capacitance of the source of M_1 and thus preventing its breakdown.

To increase the drive capability of the TI stage in high noise-power efficiency, this work employs a differential source-input buffer [7], shown in the bottom of Fig. 3. Since the source and gate of M_{p7} and M_{p8} act as the input and the feedback terminals of the driver loop, noise introduced by the source-input buffer is reduced by half compared to voltage followers with dual input pairs. The Class AB stage no longer uses a complete multi-stage amplifier, but is simplified to a single-stage cascode amplifier, further improving efficiency with sufficient loop gain.

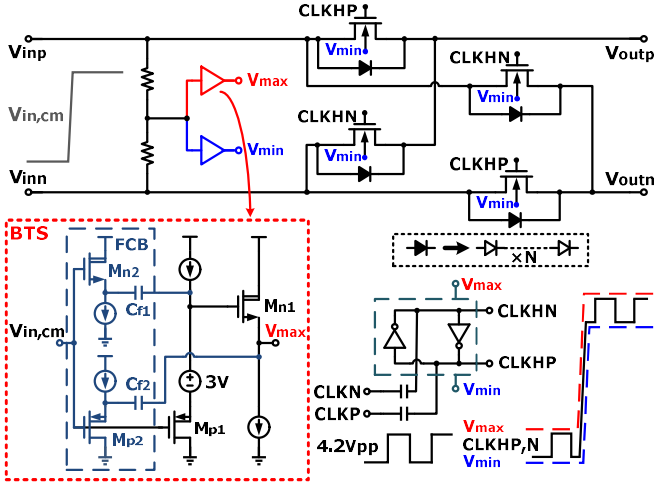

Fig. 2. The HV chopper and bidirectional transient level shifter (BTS)

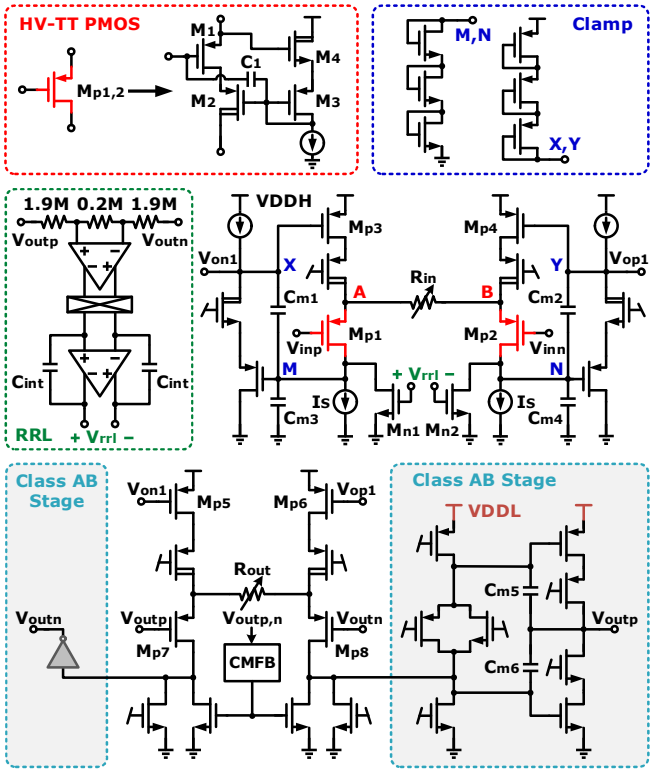

Fig. 3. Input stage and output stage of proposed HV-CBIA

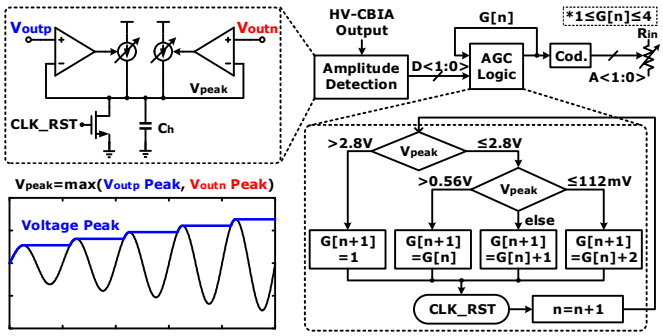

Fig. 4. The proposed AGC

A ripple reduction loop (RRL), as illustrated in the middle left of Fig.3, is used to suppress the chopping-induced ripple. The output signal with ripple is attenuated by 20× to relax the required input signal range of the voltage-to-current converter. The down-modulated current is integrated and fed back to the TC stage via M_{n1} and M_{n2}, nulling the offset in current domain.

C. Automatic Gain Control (AGC) for DR Enhancement

The maximum differential input voltage range of the CBIA is usually limited by the bias current I_S and the input balancing resistor R_{in} (Fig.3). Hence, there is a trade-off between the noise and linear input signal range. In this design, we increase the DR through automatic gain control (AGC) of the CBIA according to the output voltage amplitude.

To estimate the output signal amplitude, as shown in Fig.4, a peak detector detects the higher peaks of V_{outp} and V_{outn}. When $V_{outp,n}$ rises, the current source is enabled to charge C_h, making V_{peak} to follow the higher output. When $V_{outp,n}$ falls, the current source is disconnected to hold the V_{peak}.

According to the quantized output of V_{peak}, i.e., D<1:0> and the CBIA's gain settings, a digital logic module (right of Fig.4) updates the control code A<1:0> to reconfigure input resistor R_{in} at 20kHz by periodical reset of CLK_RST. The logic guarantees that the output amplitude is within a fixed voltage range between $0.56V_{pp}$ to $2.8V_{pp}$, thereby ensuring an optimal SNR. When an output amplitude exceeding $2.8V_{pp}$ is detected, the gain is first set to 1 and then leveled up to the most appropriate gain to avoid possible saturation. Although the operation of setting the gain to 1 first will increase the transition gain of one cycle, it still speeds up the potential delay of the gradual gain transition in case the signal saturates. Compared to a fixed-gain CBIA, the AGC can prevent saturation due to large signal input, and increase gain for SNR optimization when the input signal amplitude is low.

D. Segmented Gain Adjustment

For input devices using floating bias, their parameters vary with the input CM voltage. This results in a non-negligible gain error for the CBIA. The segmented gain adjustment scheme can compensate for this error by quantizing the input CM voltage and configuring R_{out} accordingly (Fig.1). Note that the input CM voltage, extracted from the HV input chopper, is also attenuated by 20× first to the LV domain and then quantized by a 3-bit flash ADC. According to the mapping relationship between the digital output and gain fluctuation obtained by simulation, we adjust the resistance value of R_{out} accordingly to compensate for the gain error.

III. Measurement Results

The HV-CBIA was fabricated in a 0.18μm BCD process and the chip area is 3mm² (Fig. 5, left). It is packaged in DIP48 and consumes 305μA from 60V/4.2V supply (Fig. 5, right).

Thanks to the BTS and HV-TT PMOS, in Fig.6, for a $20V_{pp}$ CM transient voltage, the CBIA can withstand CM transients of 54V/μs (rising) and 56V/μs (falling), respectively. At output, the maximum spike is less than $75mV_{pp}$.

Fig. 7 compares the output waveforms with and without the AGC. Enabling the AGC effectively prevents signal saturation and the output signal amplitude is adjusted to the fixed 0.56Vpp to 2.8Vpp range. It should be noticed that signal is only affected at the two transients during the gain switching. The remaining output amplified with different gains can still be reconstructed in the digital domain.

In Fig.8, when AGC is enabled, for a 7kHz input signal, the CBIA achieves a cross-scale DR of 115dB in 10kHz bandwidth. This is a 40dB improvement with respect to the fixed high gain setting. When the input signal is 200kHz, the DR is still 98dB in a 500kHz noise bandwidth.

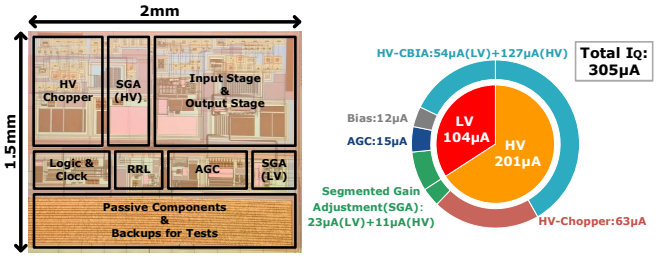

Fig. 5. Die micrograph and power consumption distribution

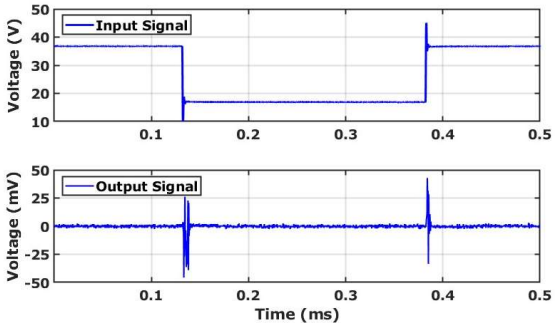

Fig. 6. Response of HV CM Transient

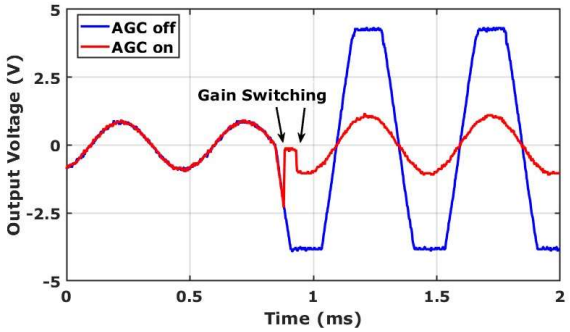

Fig. 7. Output waveform w/i and w/o AGC

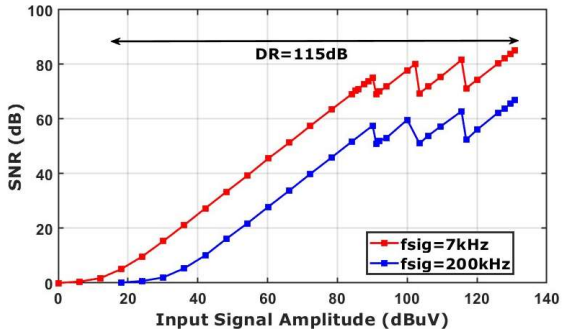

Fig. 8. SNR and DR of proposed HV-CBIA

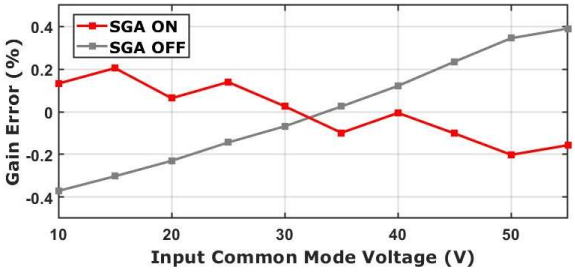

Fig. 9. The CM-dependent gain error

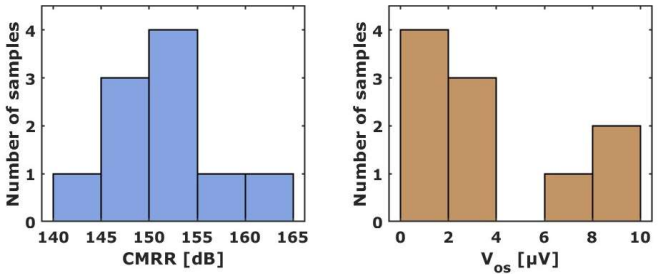

Fig. 10. Measured CMRR and offset of 10 samples

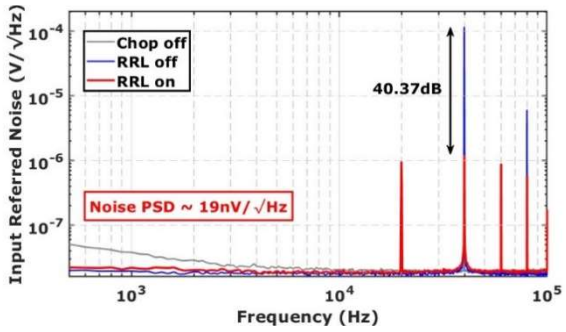

Fig. 11. Input referred noise PSD

Benefiting from the segmented gain adjustment (SGA), over a wide input CM voltage range of 10V to 55V (Fig.9), the gain error is reduced by 50% to less than ±0.2%.

Fig. 10 plots the CMRR and input offset distributions of 10 samples. The proposed HV-CBIA achieves a lowest CMRR of 140dB and maximum offset of less than 10μV. Fig. 11 shows the measured input referred noise PSD. Chopping at 40kHz can significantly reduce the flicker noise and achieve a noise floor of 19nV/√Hz. The RRL suppresses the ripple by 40dB without noise penalty. Note that the 20kHz harmonic in spectrum is due to the AGC refresh clock.

Table I compares this work with state-of-the-art HV-IAs and -OPAs. By improving CM transient tolerance to both the input chopper and CBIA input stage, this work achieves the best-in-class CM transient tolerance of 54V/μs and low input referred noise of 19nV/√Hz. The CBIA gain variation is limited to 0.2% without trimming. Thanks to the AGC, this CBIA exhibits a high DR of 115dB, which is 13dB higher than [7]. Finally, this work also shows competitive GBW and CMRR.

TABEL I. COMPARISON WITH STATE-OF-THE-ART

Parameter	[4]	[5]	[6]	[2]	[7]	This work
Year	2015	2024	2009	2012	2025	2025
Topology	OPA	OPA	Three-opamp	CCIA	CBIA	CBIA
Technology	0.18μm BCD	0.18μm BCD	0.35μm HV CMOS	0.7μm CMOS	0.18μm BCD	0.18μm BCD
Supply[V]	60	50	36	30/3	36	60/4.2
Input CM Voltage Range [V]	0-58.5	0-47.65	2-34	±30	0-34.5	0.7-56.3
CM transient tolerance [V/μs]	0.4	1.3	N/A	0.002	N/A	**54**
CMRR [dB]	145	140	120(G=1)	160	140(G=1)	**140(G=1)**
DR [dB] *	NS	NS	83(G=128)	91	102(G=50)	**115**
e_{n-n} [nV/√Hz]	6.8	14	19(G=128)	31	39(G=50)	19(G=100)
Input offset [μV]	5	NS	20	5	5	10
Gain error (CM-dependent) [%]	NS	NS	NS	NS	NS	**±0.2**
GBW [MHz]	3.1	3.55	8	1	280(G=50)	**40(G=100)**
I_Q [mA] **	0.84	1.15	2.2+0.75	0.026	0.7	0.2+0.1
GBW/I_Q [MHz/mA]	3.7	3.1	2.7	38.4	400	**133**

NS=Data not shown *Calculated in 10kHz bandwidth **LV Current + HV Current

IV. CONCLUSION

To withstand the high-amplitude, fast varying CM transient in high-side current sensing, this paper proposes CM transient tolerant techniques in both the CBIA and input chopper. The complementary capacitive feed-forward path has been used to increase the slew and prevent the breakdown of LV transistors. Furthermore, the CBIA gain accuracy and DR are enhanced by segmented gain adjustment and AGC techniques, respectively.

ACKNOWLEDGMENT

This work was supported by the National Natural Science Foundation of China (Grant No. 62474046), and Jiashan Fudan Institute, Jiashan, 314100, Zhejiang, China.

REFERENCES

[1] J. F. Witte et al., "A current-feedback instrumentation amplifier with 5μV offset for bidirectional high-side current-sensing," ISSCC Digest, pp. 74-596, Feb. 2008.

[2] Q. Fan et al., "A capacitively coupled chopper instrumentation amplifier with a ±30V common-mode range, 160dB CMRR and 5μV offset," ISSCC, pp. 374-376, Feb. 2012.

[3] C. Birk et al., "A 60V capacitive gain 27nV/√Hz 137dB CMRR PGA with ±10V inputs," Digest of ISSCC, pp. 376-377, Feb.2012

[4] Y. Kusuda " A 60V Auto-Zero and Chopper Operational Amplifier With 800 kHz Interleaved Clocks and Input Bias Current Trimming," IEEE JSSC, vol. 50, no. 12, pp. 2804-2813, Dec. 2015.

[5] S. Zhang et al., "A 50V chopper operational amplifier with 1.3V/μs common-mode transients tolerance," ESSERC, pp. 49-52, Sep. 2024.

[6] V. Schaffer et al., "A 36V programmable instrumentation amplifier with sub-20μV offset and a CMRR in excess of 120 dB at all gain settings," IEEE JSSC, vol. 44, no. 7, pp. 2036-2046, Jul. 2009.

[7] S. Ye et al., "A 36V current-balancing instrumentation amplifier with ±24V input range, 5.6 MHz BW, and 140dB CMRR at all gain settings," ISSCC, vol. 68, pp. 1-3, 2025.