A 111-µW 100.8-dB DR Audio Continuous-Time Delta-Sigma Modulator Using Positive Feedback Amplifier

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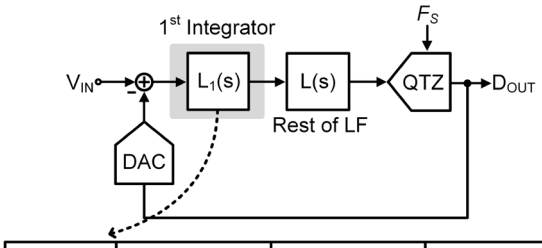
***Abstract*—This paper presents an audio continuous-time delta-sigma modulator (CTDSM), whose first integrator is implemented with a positive feedback amplifier (PFA), resulting in high energy efficiency. The gain of the PFA reduces the in-band quantization noise and the input-referred noise of the subsequent loop filters. The use of an 8-tap FIR DAC and chopping further improves the linearity and noise of the CTDSM while maintaining the energy efficiency of a PFA-based integrator. The prototype CTDSM is implemented in a 65nm CMOS process and occupies an active area of 0.3mm². It achieves a 97.7dB SNDR and 100.8dB DR within a 24kHz bandwidth while consuming only 111µW from a 1.2V supply. This results in a competitive Schreier's FoM of 184.1dB.**

Keywords*—*Continuous-time delta-sigma modulator, audio, positive feedback amplifier (PFA), PFA-based integrator, gain enhancement, in-band quantization noise, input-referred noise, noise attenuation, high linearity, flicker noise, chopping, and energy efficiency.

I. Introduction

Continuous-time delta-sigma modulators (CTDSMs) are widely used for audio applications due to their inherent anti-aliasing property and easily driven resistive inputs. To achieve high linearity (SFDR > 100dB) and wide dynamic range (> 100dB), a highly linear first integrator is essential, which directly affects the linearity of the CTDSM. Fig. 1 shows the strengths and weaknesses of CTDSMs with different types of first integrators. Active RC integrators are commonly used due to their high linearity and excellent in-band quantization noise (QN) suppression, but their relatively high-power consumption poses a challenge to the design of energy-efficient amplifier [1-5]. Another approach is the use of passive RC integrators, which not only increase the order of the loop filter but also significantly reduce the signal swing. This relaxes the linearity requirements of the subsequent loop filter, thus enabling good energy efficiency [6]. However, passive integrators compromise the loop gain compared to their active counterparts, increasing both the in-band QN and the input-referred noise (IRN), thus degrading the SNDR performance.

To address these challenges, this paper proposes a positive feedback amplifier (PFA) as the first integrator in the CTDSM. By exploiting the PFA, the DC gain of the first integrator is significantly boosted, enabling low in-band QN and low IRN. The use of an inverter-based PFA relaxes the complexity of the first integrator, resulting in lower power consumption compared to active RC integrators. The rest of this paper is organized as follows: Section II presents the proposed PFA-based integrator and its application into CTDSM. Section III describes the circuit implementation. The measurement results are presented in Section IV, followed by a conclusion in Section V.



$L_1(s)$	Active RC Integrator	Passive RC Integrator	PFA-based Integrator
In-Band QN	☺	☹	☺
IRN	☺	☹	☺
Power	☹	☺	☺

Fig. 1. CTDSMs with different types of first integrators.

II. Proposed PFA-Based Integrator

A. Concept of the PFA-based Integrator

Fig. 2 shows the proposed PFA-based integrator. Without the PFA, the proposed integrator exhibits the same behavior as the passive RC integrator with its pole at $1/2R_1C_1$, where R_1 is the input resistor, and C_1 is the integration capacitor. Although the passive RC integrator introduces a pole in the loop filter, which increases the order of the loop filter, its unity DC gain limits the loop gain. However, by employing the PFA, the transfer function can be modified as follows:

$$H_{w/PFA}(s) = \frac{1}{(2R_1C_1)s+(1-G_mR_1)}, \quad (1)$$

where G_m is the effective transconductance of the PFA. When G_mR_1 gets close to 1, the loss term $(1-G_mR_1)$ can be eliminated and the integrator's pole moves toward DC, resulting in high DC gain. However, unlike the active RC integrator, the required G_m in the PFA-based integrator depends on R_1, thereby allowing the use of a simple and energy-efficient amplifier for the PFA. Thanks to the modified transfer function of the PFA-based integrator, the IRN of subsequent loop filters ($v^2_{n,sub}$) is attenuated by the gain of the integrator, thereby reducing the total IRN.

B. Proposed CTDSM Architecture

Fig. 3 shows the proposed CTDSM, which consists of a 3rd order CIFF-B loop filter with a PFA-based first integrator and a 1.5-bit quantizer. Although the PFA boosts the DC gain, a large output swing of the PFA may cause nonlinearity.

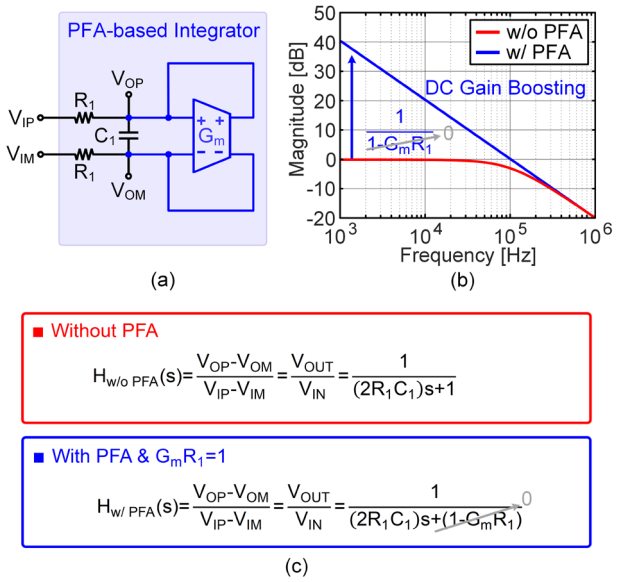


Fig. 2. (a) Proposed PFA-based integrator, (b) magnitude response of the proposed integrator with and without the PFA and (c) the transfer function of the proposed integrator with and without the PFA.

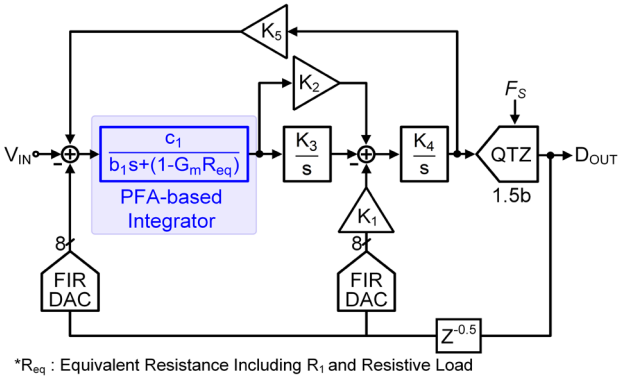


Fig. 3. The proposed CTDSM architecture.

In particular, the effective G_m of the PFA varies with the integrator's output swing, which may degrade the SQNR. Since the output swing of the PFA-based integrator decreases as C_1 increases, increasing C_1 helps to suppress the G_m variations of the PFA. However, as shown in Fig. 4(a), to meet the target SQNR of 108dB, a large C_1 of more than 1.35nF is required only for the tri-level DAC, leading to a significant area penalty. To further reduce the swing without area overhead, a FIR-DAC is utilized, which also offers a high DAC linearity. Fig. 4(b) shows the required C_1 according to the number of FIR taps (= N) to meet the target SQNR. For N = 8, the value of C_1 can be as low as 135pF, which is 1/10 of the area required when without using the FIR-DAC.

C. *SQNR and IRN Tolerance over G_m Variation*

Considering the practical circuit implementation, the required G_m is $1/R_{eq}$, where R_{eq} is the effective resistance including R_1 and the resistive load of the first integrator. If the G_m deviates from $1/R_{eq}$, the integrator's gain decreases and the pole shifts to higher frequency, resulting in a SQNR loss. As shown in Fig. 5, the simulation results show that the SQNR of over 115dB can be achieved within the target ΔG_m range of ±5%. Even under the G_m variations of ±10%, the simulated SQNR has a sufficient margin of more than 5dB.

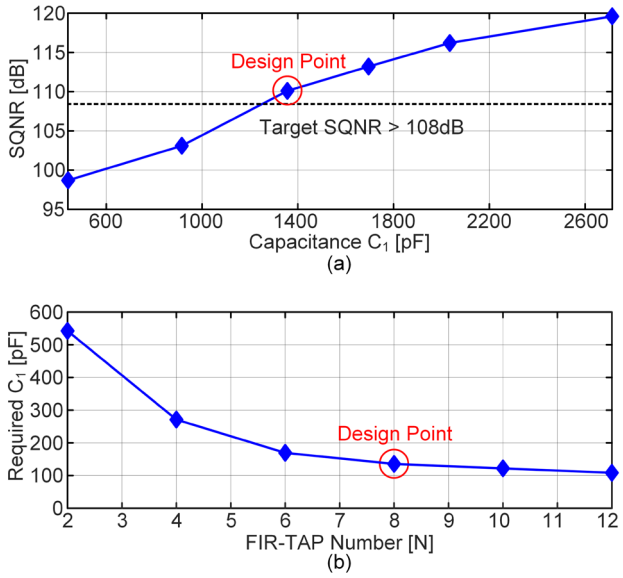


Fig. 4. (a) SQNR vs. C_1 without FIR-DAC and (b) required C_1 vs. FIR tap number N.

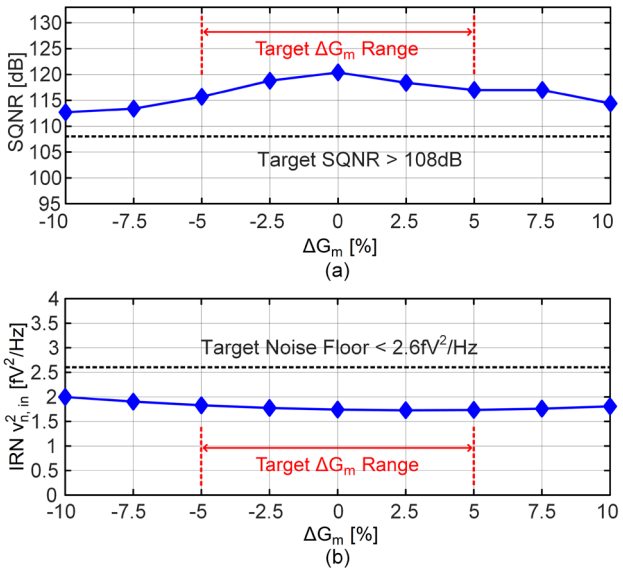


Fig. 5. (a) SQNR vs. G_m variations and (b) IRN vs. G_m variations.

Additionally, the IRN also varies with respect to G_m variation. However, within the target ΔG_m range of ±5%, the IRN remains lower than 2fV^2/Hz and thus SNR varies less than 0.64dB. As can be seen, the PFA-based integrator shows a sufficient tolerance of the SQNR and IRN with respect to the G_m variations.

III. Circuit Implementation

Fig. 6 shows the overall schematic of the proposed CTDSM with a PFA-based integrator. It operates at a sampling rate F_s of 8MHz. An out-of-band gain (OBG) of 1.7 is chosen to achieve a -2.0dBFS maximum stable amplitude (MSA). The input resistance R_1 of 12kΩ is chosen to achieve the target DR of 100dB. The first integrator is implemented with a PFA-based integrator. The second and third integrators are implemented with inverter-based active RC integrators. The tri-level RDAC is implemented with 8-tap FIR filter to improve the linearity of the loop filter as well as jitter sensitivity. Thanks to the FIR DAC, the value of C_1 is 135pF

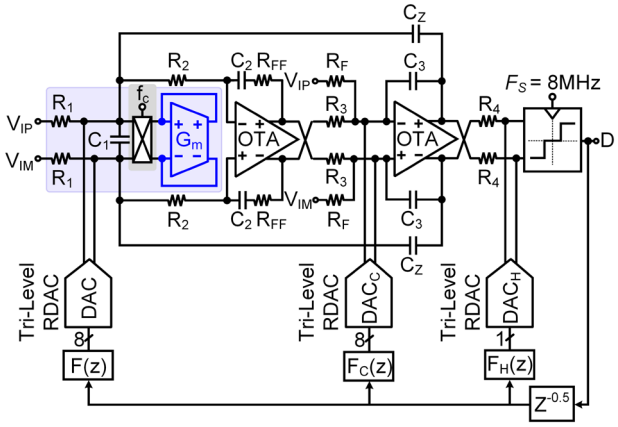


Fig. 6. The overall schematic of the proposed CTDSM.

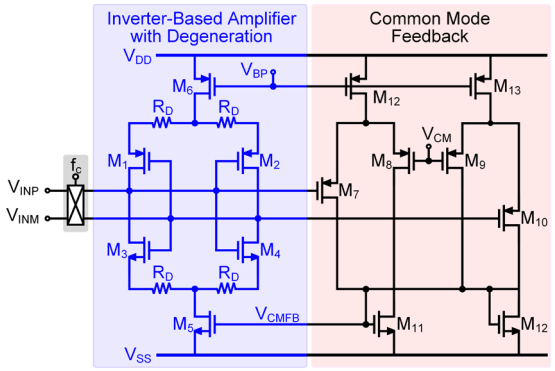


Fig. 7. The schematic of the proposed PFA.

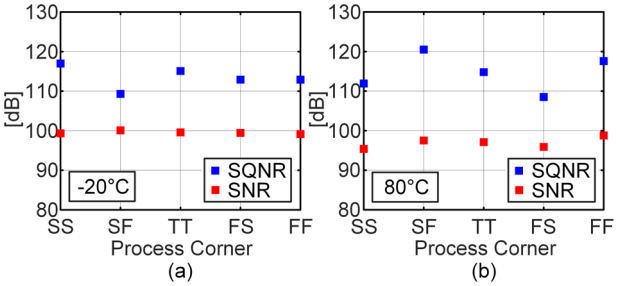


Fig. 8. Simulated SQNR and SNR over temperatures ((a) -20°C and (b) 80°C) and process corners after one-time corner calibration at each corner.

and the output swing of the PFA-based integrator is less than 40mV_{pp}. The PFA is chopped to suppress 1/*f* noise. Chopping frequency of F_s/16 is chosen, whose ripple is aligned with the notch frequency of the FIR filter, avoiding quantization-noise aliasing. The modified NTF due to the FIR filter transfer function F(z) is restored with a compensation FIR filter $F_C(z)$. An excess-loop-delay (ELD) of 0.5T_s is realized by a direct feedback path around the quantizer with a passive adder. A direct feedforward path from the input is implemented with feedforward resistors R_F (= 214kΩ) to reduce the internal swing of the second integrator and the loop filter's zero is optimized through feedback capacitors C_Z (= 255fF).

Fig. 7 shows the schematic of the proposed PFA. The PFA is implemented with an inverter-based amplifier with source degeneration. The common mode voltage of the PFA is stabilized with a common-mode feedback (CMFB) circuit. The required effective G_m for the PFA, is approximately 93μS, considering $1/R_{eq} = 1/(R_1 \parallel R_{DAC} \parallel R_2)$, which is implemented only with 21μA. Chopping mitigates the intrinsic 1/*f* noise of the PFA, thereby allowing the use of

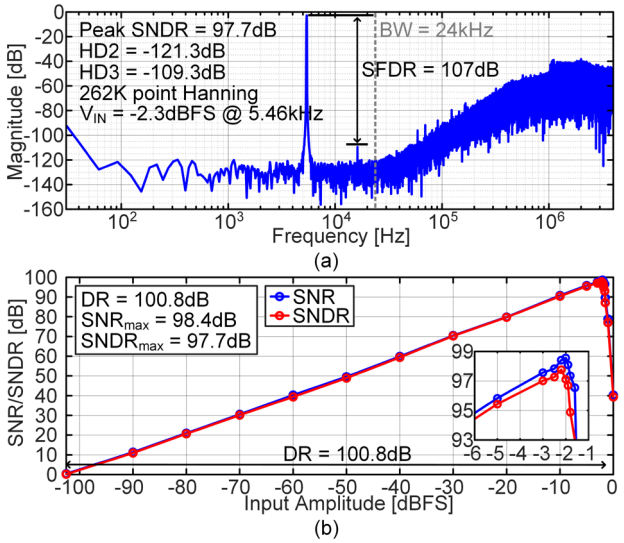


Fig. 9. (a) Measured PSD and (b) SN(D)R vs. input amplitude.

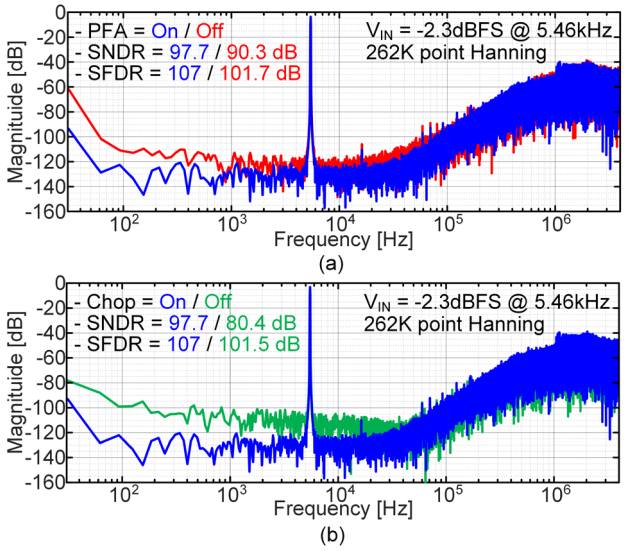


Fig. 10. (a) Measured PSD with and without the PFA and (b) measured PSD with and without chopping.

small input transistors ($LW_{M1,\ M2}$ = 3.6μm², $LW_{M3,\ M4}$ = 1.8μm²). Despite the relatively small transistor sizes, the Monte-Carlo simulation results show that the 3σ variation of G_m remains within ±2.7%, which ensures a DC gain greater than 30dB. Thanks to the DC gain of the PFA, the noise from the subsequent loop filter is effectively mitigated, resulting in an IRN of less than 2.6fV²/Hz. Therefore, the dominant noise sources are R_1, R_{DAC}, and the PFA. Fig. 8 shows the simulated SQNR and SNR over different temperatures (-20°C and 80°C) and process corners after one-time calibration at each corner by adjusting capacitor banks and trimming the bias current. Monte-Carlo corner simulations confirmed that the mismatch between the G_m and $1/R_{eq}$ remains below ±5% across the temperature range of -20°C to 80°C. Even with the temperature and process variations, low in-band QN and IRN are preserved, validating the effectiveness of the PFA-based integrator.

IV. Measurement Results

The prototype CTDSM is fabricated in a 65nm CMOS process and occupies a core area of 0.3mm² (Fig. 12). It draws only 111μW from a 1.2V supply voltage (Fig. 11(d)). At an

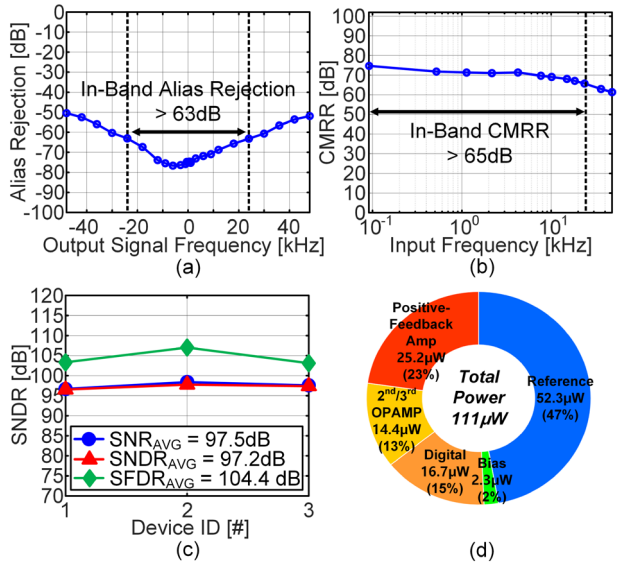


Fig. 11. (a) Measured in-band alias rejection, (b) measured CMRR, (c) measured peak SNR, SNDR and SFDR and (d) power breakdown.

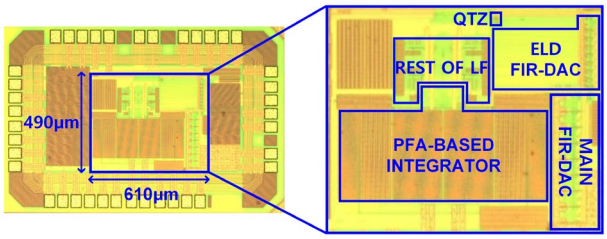


Fig. 12. Chip micrograph.

input frequency of 5.46kHz, the measured peak SNDR, SNR and SFDR are 97.7dB, 98.4dB and 107dB, respectively (Fig. 9(a)). The measured DR is 100.8dB. Fig. 10 shows the measured output spectrum with and without the PFA and chopping. Thanks to the gain enhancement with the PFA, the subsequent loop filter's noise is alleviated while compensating for the loop gain. Consequently, employing the PFA offers a 7.4dB SNDR improvement, validating the effectiveness of the PFA. Moreover, the SNDR of 17.3dB is improved by the chopping of the PFA. The measured in-band alias rejection ratio and CMRR are above 63dB and 65dB, respectively (Fig. 11(a), (b)). The performance of 3 devices is measured and the SNDR variation is less than 1.2dB (Fig. 11(c)).

Table I shows the performance summary and comparison with the state-of-the-art CT audio ADCs [2], [4], [5], [6]. Compared to CT ADCs with an active RC first integrator [2], [4], [5], the PFA consumes less than a 1/4 of the total power, validating its high energy efficiency. Compared to [6] which uses PFA-based first integrator, this work achieves 2.5× lower IRN and higher DR without beyond-the-rail operation. Finally, this work achieves competitive Schreier's FoM_{DR} of 184.1dB and FoM_{SNDR} of 181.0dB.

V. Conclusion

This paper presents an audio CTDSM with a PFA-based integrator. Thanks to the PFA, the in-band QN is significantly suppressed by boosted DC gain, and the noise of the subsequent loop filter is well attenuated by the PFA gain. This allows the power scaling of the subsequent integrator,

Table I. Performance Summary and Comparison

	This Work	VLSI'24 [6]	JSSC'21 [5]	JSSC'20 [4]	JSSC'20 [2]
CTDSM Architecture	**CTDSM FIR DAC**	CTDSM	CTDSM FIR DAC	CT FIR MASH	CT ZOOM
Integrator Type	**PFA**	PFA	Active RC	Active RC	Active RC
Process [nm]	**65**	65	65	180	160
Area [mm^2]	**0.3**	0.28	0.28	0.65	0.27
Bandwidth [kHz]	**24**	24	24	24	20
F_s [MHz]	**8**	6.144	8	6.144	5.12
Supply [V]	**1.2**	1.0	1.2	1.8	1.8
Power [μW]	**111**	80.7	134	265	618
SNDR [dB]	**97.7**	99.2*	99.4	100.9	106.4
DR [dB]	**100.8**	100*	102.8	104	108.5
$V_{IN@PEAK, SNDR}$ [V_{pp}]	**1.84**	3.25*	1.8	3.23	3.54
Estimated IRN [fV^2/Hz]	**2.55**†	6.32†	1.69†	3.67†	1.21†
1st Int Power [μW]/[%]	**25.2**†† **(22.7%)**	20†† (24.8%)	55.6†† (41.5%)	68.9†† (26%)	204†† (33%)
FoM_{SNDR} [dB]	**181.0**	184.0*	181.9	180.5	181.5
FoM_{DR} [dB]	**184.1**	184.7*	185.3	183.6	183.6

*Beyond-the-Rail

†Estimated IRN = $(\frac{\text{Signal Power}}{10^{SNR/10}})$/Bandwidth, ††Calculated Power

thereby improving overall energy efficiency. Moreover, since the G_m of the PFA is determined by the equivalent resistance of the integrator, the design complexity is significantly reduced compared to the conventional integrators. This allows the amplifier to be implemented with a simple inverter-based amplifier and consumes less power. As a result, the prototype CTDSM achieves a competitive Schreier's FoM_{DR} of 184.1dB. Given the measured performance, the proposed PFA-based integrator offers great promise in realizing energy-efficient audio CTDSMs.

Acknowledgment

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