A 25–31-GHz 0.98-mW Dual-Ellipse Vector-Summing Variable-Gain Phase Shifter With Current-Reusing Enabling Calibration-Free Orthogonal Phase and Gain Control

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***Abstract*—This paper presents a compact sub-mW variable-gain phase shifter (VGPS) for mm-wave beamformers. A dual-ellipse vector summation is proposed to achieve low gain variation during phase shifting, enabling calibration-free orthogonal phase and gain control. Fabricated in 28-nm CMOS, the proposed VGPS achieves a 3-bit gain control and a 6-bit phase shift with rms errors of $<$0.32 dB and $<$1.47° from 25 to 31 GHz, respectively. Moreover, thanks to the proposed current-reuse structure with an ultra-compact folded transformer, this work only consumes 0.98 mW and occupies a core area of 0.188 mm^2.**

***Keywords*—Beamforming, current reuse, folded transformer, mm-wave, phased array, variable-gain phase shifter (VGPS)**

I. Introduction

Phased-array beamformers, widely used in 5G networks and satellite communications, enable high-data-rate and long-range wireless links through beam steering and sidelobe suppression. A critical circuitry in this system is the variable-gain phase shifter (VGPS), which integrates both phase shifter (PS) and gain controller (GC)[1] functionalities.

Among the various reported VGPS topologies, the vector-summing architecture generates the desired vector by weighting quadrature signals in Cartesian coordinates. However, such an interdependent phase and gain control scheme typically requires complex calibration to realize phase-gain orthogonality [1]–[4]. Direct generation in polar coordinates can be achieved through orthogonal DACs; however, nonidealities of complex DACs degrade the orthogonality between PS and GC [4], [5]. Maintaining orthogonal control of phase and gain is crucial to ensure the independent operation of beam steering and sidelobe suppression [6]. The cascaded PS and GC offer better orthogonality by physically separating the gain and phase control [7], but this incurs significant area and power.

Furthermore, there is a growing demand for compact and energy-efficient beamforming systems. The constraint of half-wavelength antenna spacing puts tough restrictions on the area per element, a limitation that becomes particularly significant as operating frequencies increase into mm-wave bands. Meanwhile, in a low-earth-orbit small-satellite-communication phased-array receiver, for instance, each element requires an ultralow power consumption below 4 mW [8]. Therefore, a compact and low-power VGPS is highly desirable. However, achieving both goals is non-trivial, as passive components such as I/Q generators and inter-stage matching networks typically occupy substantial area, while transistor nonlinearities under ultralow power induce significant phase and gain errors. Thus, most prior implementations occupy considerable chip area and consume more than 7 mW [1]–[5], [7], [9].

[1]The GCs refer to circuits such as VGAs and attenuators.

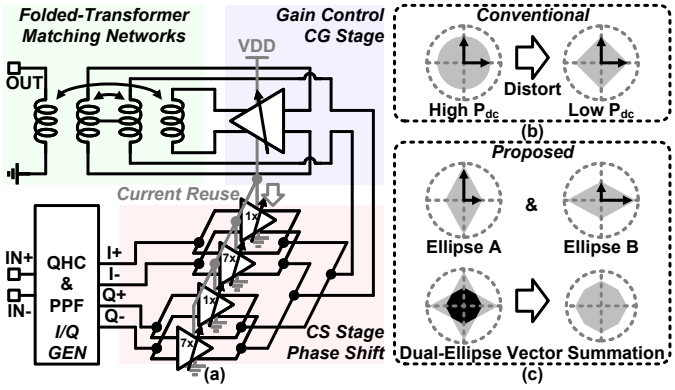

Fig. 1: (a) Block diagram of the proposed VGPS; (b) conventional scheme, and (c) proposed dual-ellipse vector summation for g_m nonlinearity compensation.

To address the aforementioned challenges, we propose a compact 25–31 GHz VGPS that enables calibration-free orthogonal phase and gain control with low error while consuming sub-mW power.

II. Dual-Ellipse Vector-Summing VGPS

A. Current-Reuse and Dual-Ellipse Vector Summation

Fig. 1(a) shows the block diagram of the proposed dual-ellipse vector-summing VGPS, where the PS and GC are separate and cascaded in the ac path but stacked in the dc path for current reuse. To minimize mutual interference and maintain orthogonality, the current through both blocks must remain constant during the phase and gain changes. A Gilbert cell–based common-source (CS) VGA is employed in the PS for its constant total dc current, low phase and gain errors, and low power consumption [1], [4].

For conventional Gilbert cell-based PSs, transistors in the strong inversion region exhibit the opportune relationship between the small-signal transconductance (g_m) and the bias current (I_d) as $g_m \propto \sqrt{I_d}$. Thus, the total transconductance across the I and Q paths satisfies $g_{\mathrm{m,tot}} = \sqrt{g_{mI}^2 + g_{mQ}^2} \propto \sqrt{I_I + I_Q} = \sqrt{I_{\mathrm{tot}}}$. Ideally, $g_{\mathrm{m,tot}}$ remains constant when I_{tot} is fixed and the state points are arranged as a circle on the

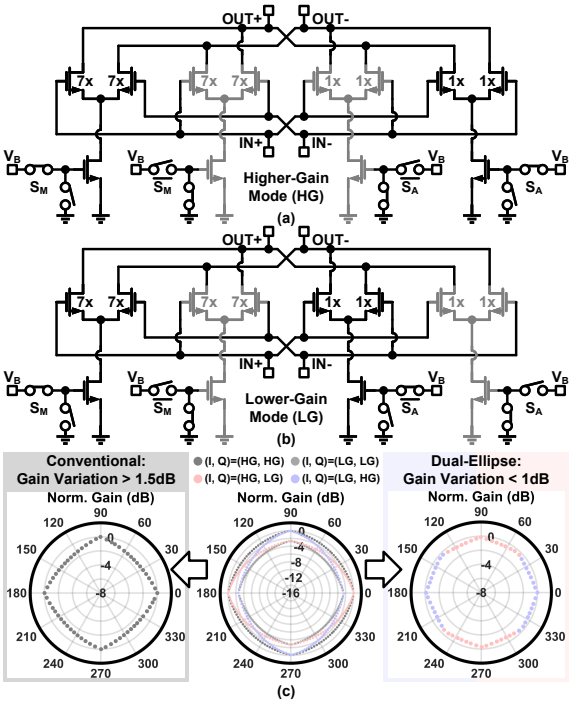

Fig. 2: Operation modes of the ultra-low-power VGA in the PS: (a) higher-gain mode (HG), (b) lower-gain mode (LG); (c) simulated vector constellations of different vector-summation methods with I-VGA and Q-VGA configured in different modes.

vector constellation. However, maintaining strong inversion typically requires approximately 10 mW or more of dc power [4], [5], [9], which is excessive for low-power beamformers. At sub-mW power levels, as necessary in large arrays, transistors enter the weak inversion region where $g_m \propto I_d$, leading to $g_{\mathrm{m,tot}} \propto \sqrt{I_I^2 + I_Q^2} = \sqrt{k^2 + (1-k)^2} \times I_{\mathrm{tot}}$, in which $k = I_I / I_{\mathrm{tot}}$ varies with phase states. This g_m nonlinearity becomes more pronounced when the fraction of the I (or Q) path current is small. As shown in Fig. 1(b), the vector constellation deviates from an ideal circular shape to a rhombus, resulting in significant gain error during phase control.

To address this issue, a dual-ellipse vector summation is proposed to compensate for the g_m nonlinearity caused by the low bias current, as shown in Fig. 1(c). The proposed topology comprises the main Gilbert unit (7× size) and the smaller auxiliary Gilbert unit (1× size), enabling the operation in higher-gain and lower-gain modes. In the higher-gain mode, the main and auxiliary units operate with the same polarity, as shown in Fig. 2(a), while they operate with the opposite polarities in the lower-gain mode, as shown in Fig. 2(b). The architecture mitigates the g_m nonlinearity particularly when the current ratio in the I (Q) path is small, where the g_m degradation becomes more significant. This is achieved by setting the I (Q) path VGA to a higher-gain mode while configuring the Q (I) path VGA to a lower-gain mode accordingly.

Fig. 2(c) plots the simulated vector constellation of the proposed VGPS when it consumes <1 mW. The conventional configuration, in which only the higher-gain mode is used, exhibits a gain variation exceeding 1.5 dB. In contrast, when the

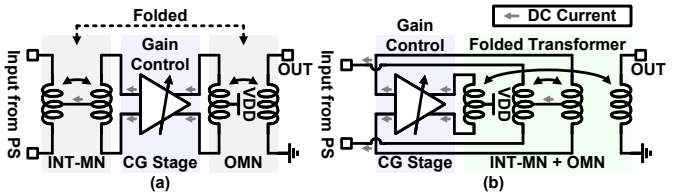

Fig. 3: Interstage (INT-MN) and output matching networks (OMN) (a) before and (b) after folding the transformers.

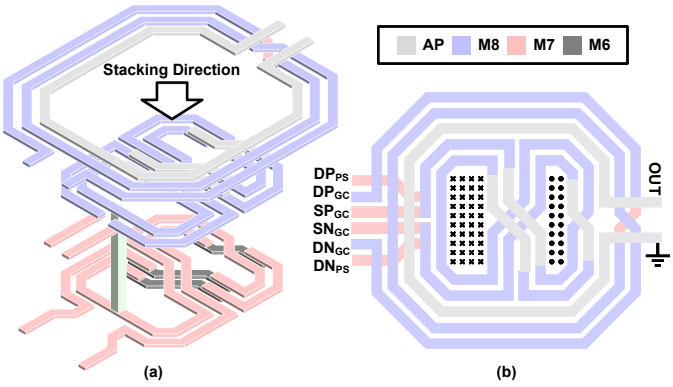

Fig. 4: Folded interstage and output transformers: (a) 3D stacking and (b) planar-view layout.

two VGAs operate in different modes, elliptical constellations aligned with the I or Q axis are formed. By selecting optimized states from both ellipses, a near-octagonal constellation with gain variation reduced to below 1 dB is achieved. A low gain variation enables reduced coupling between PS and GC, leading to improved orthogonality in the proposed VGPS.

B. Folded-Transformer-Based Wideband Matching Networks

The proposed VGPS is a cascade of CS and common-gate (CG) stages to enable the inter-block current-reuse between the dc-wise staked-up PS and GC, as shown earlier in Fig. 1. Commonly, an inductor would be inserted in series between the CS and CG stages to enhance the gain and reduce the phase variation by resonating out the interstage parasitic capacitance [7], [10]; however, as a 2nd-order network, it exhibits a narrow bandwidth. In this work, an interstage matching network employing a transformer is proposed. It introduces a 4th-order broadband network between the CS and CG stages, boosting the gain, reducing the phase variation, and providing separation between the ac/dc paths over a wide bandwidth.

To save the chip area incurred by the interstage transformer, folded transformers are employed to achieve an ultracompact layout. Fig. 3, Fig. 4(a), and Fig. 4(b) respectively show the schematic, the 3D stacking, and the planar-view layout of the ultracompact folded transformer, where the interstage transformer is twisted into an "8" shape and embedded within the output transformer [11]. The 8-shaped interstage transformer, though overlapped with the output-stage transformer, introduces no interference due to its self-canceling magnetic field. Additionally, the "8" shape's center axis is slightly shifted to minimize the inter-transformer coupling coefficient, namely the inter-transformer interference. Furthermore, in the 8-shaped interstage transformer, the center taps of the primary

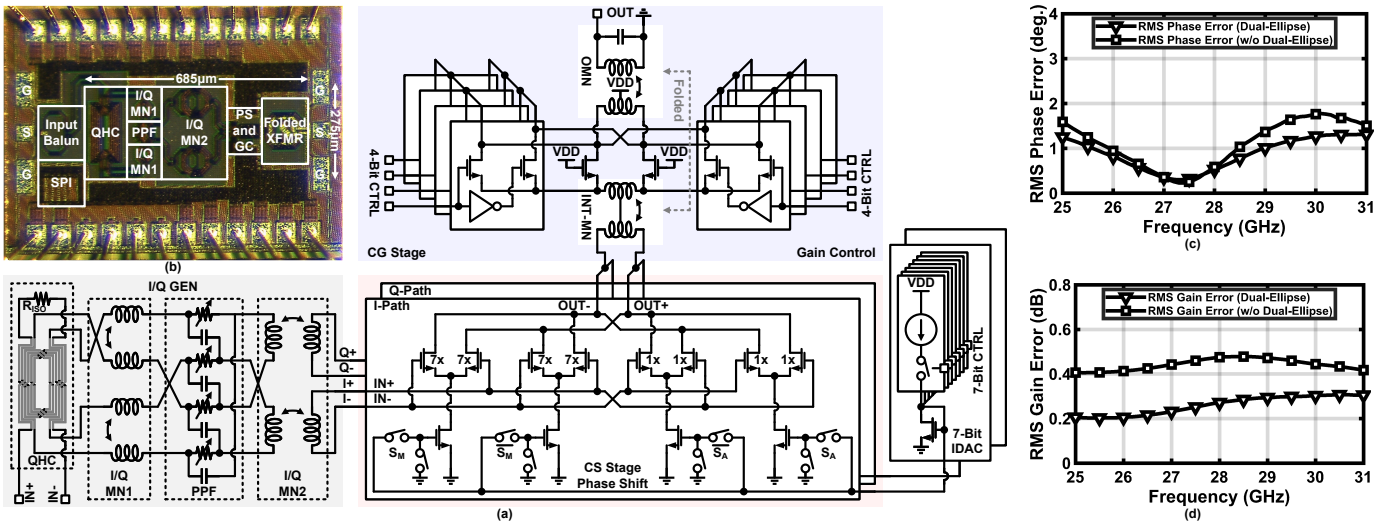

Fig. 5: (a) Detailed schematic, (b) die micrograph, (c) measured rms phase error, and (d) rms gain error of PS under the maximum gain state with/without engaging dual-ellipse vector summation.

and secondary coils are connected locally through M8-M7 vias, realizing current reuse easily without extra routing and thus significantly reducing the IR drop. Consequently, the two transformers effectively occupy the footprint of a single transformer, eliminating the large area penalty typically associated with the conventional two-stage current-reuse designs.

C. Detailed Circuit Implementation

Fig. 5 shows the detailed schematic of the proposed VGPS. The I/Q generator comprises a quadrature hybrid coupler (QHC) and an RC poly-phase filter (PPF), enabling wideband I/Q generation with low amplitude and phase errors and offering a more compact layout compared to the two-stage QHC design [2]. The transistor in the main Gilbert unit of the PS is sized at 19.2-μm/30-nm. The tail current-source transistor is designed with an enlarged size (128-μm/300-nm) to minimize errors from the current DAC (IDAC). The 7-bit IDAC employs PMOS current sources, with the current diverted through switches into NMOS current mirrors for the I and Q paths. The transistor sizes in the current-steering GC follow the ratio of 1:2:3:4, with the minimum unit size being 1.2-μm/30-nm. Additionally, a fixed unit with a transistor size of 19.2-μm/30-nm is incorporated to improve the GC precision. During a gain adjustment, the total number and size of transistors switched on/off at the interstage node remain constant, as seen from the GC. Consequently, the parasitic capacitance at the interstage node remains approximately unchanged, which helps to reduce the phase variation in the VGA [10].

III. Measurement Results

The prototype of the proposed VGPS is implemented in TSMC 28-nm HPC+ CMOS, as shown in Fig. 5(b). Thanks to the folded-transformer technique, the core area is only 0.188 mm^2, excluding pads and on-chip input balun. Its dc power consumption is 0.98 mW at 0.9 V.

Fig. 5(c) and Fig. 5(d) show the measured rms phase and gain errors of the PS at the maximum gain state, which are

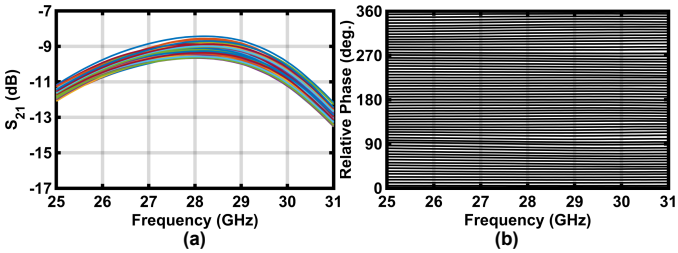

Fig. 6: Measured (a) S_{21} and (b) relative phase of 64 phase-shift states.

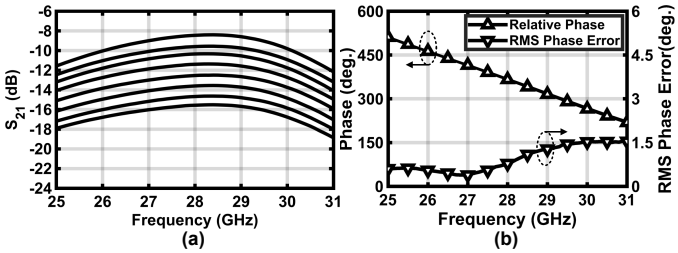

Fig. 7: Measured (a) S_{21} and (b) phase variation of gain-control stage.

<1.30° and <0.30 dB across 25–31 GHz, respectively. This is to be contrasted with the phase and gain error reaching up to 1.76° and 0.48 dB without engaging the g_m compensation by the proposed dual-ellipse vector summation, demonstrating its effectiveness in improving the phase-gain orthogonality.

Fig. 6 shows the measured gain and relative phase of the 64 states across frequency. The gain variation is <1.4 dB within 25–31 GHz, and a full 360° phase shift range with a step of 5.625° are achieved. Fig. 7(a) plots the 8 gain states with a resolution of 1 dB. The peak gain is -8.4 dB, excluding the 3-dB insertion loss of the input balun. Considering the extremely low DC power consumption, the proposed VGPS maintains relatively high energy efficiency, and its loss can be readily compensated by subsequent amplification stages of high-efficiency within the system. The measured rms phase error of the gain control stage is 0.38°–1.55° across 25–31 GHz, as shown in Fig. 7(b).

Fig. 8(a) and Fig. 8(b) show the measured rms phase and

TABLE I: COMPARISON OF PERFORMANCE METRICS

Reference	This Work	[1] CICC'24	[2] TMTT'24	[3] TCAS-II'22	[5] TMTT'21	[7] MWTL'23	[4] JSSC'23	[9] JSSC'23
Technology	28-nm CMOS	0.13-μm SiGe	40-nm CMOS	65-nm CMOS	65-nm CMOS	55-nm CMOS	65-nm CMOS	65-nm CMOS
Frequency (GHz)	25–31	32–38	20.8–43.5	24–28	52–64	23–44	26.5–29.5	18–26
Peak Gain (dB)	-8.4[a]	-1.6	-5.6	-7.4	-7.6	0	N/A	-6.2
PS Range (°)	0–360	0–360	0–360	0–360	0–360	0–360	0–360	0–360
PS Resolution	6-bit	7-bit	6-bit	6-bit	6-bit	6-bit	6-bit	3.75°
PS rms Phase Error (°)	0.29–1.30[b] 0.28–1.47[c]	0.33–1.61[b] 0.57–1.92[c]	<2[b]	1.4[b, d]	<3.3[c]	<3.2	<1.4[c]	0.75–2.08
PS rms Gain Variation (dB)	0.19–0.30[b] 0.17–0.32[c]	0.10–0.72[b] 0.18–0.93[c]	<0.25[b]	0.25[b, d]	<0.5[c]	<1.4	<0.21[c]	0.8–0.95
GC Range (dB)	0–7	0–7.5	0–6	0–8	0–14.8	0–8	0–8	N/A
GC Resolution	3-bit	4-bit	1-dB	0.25–dB	N/A	N/A	1-dB	N/A
GC Gain Error (dB)	0.07–0.44	0.08–0.26	N/A	0.06[d]	N/A	N/A	N/A	N/A
GC Phase Variation (°)	0.38–1.55 (rms) 1.05–4.09 (peak)	0.23–0.62 (rms)	0.8–2.2 (peak)	0.78 (rms)[d]	<5.5 (peak)	<11 (peak)	<1.4 (rms)	N/A
DC Power (mW)	**0.98**	12.2	7.8	31.9	18	45.6	44 (RX)	16
Chip Area (mm^2)	**0.188**	0.51	0.167	0.27	0.403	0.84	N/A	0.157
FoM$_1$[e]	**290.6**	57.3	143.1	5.8	27.7	24.6	N/A	15.3
FoM$_2$[f]	**497.4**	277.2	390.4	23.8	74.5	17.9	N/A	N/A

[a]Excluding input balun, [b]Maximum gain state, [c]All gain states, [d]At 26 GHz, [e]$\mathrm{FoM}_1 = \frac{f_0(\mathrm{GHz})\cdot \mathrm{BW}(\mathrm{GHz})\cdot G(\mathrm{lin.})\cdot n_{\mathrm{PS}}(\mathrm{bits})}{\theta_{\mathrm{rms\,error,PS}}(^\circ)\cdot A_{\mathrm{error,PS}}(\mathrm{lin})\cdot P_{\mathrm{DC}}(\mathrm{mW})}$ [9], [f]$\mathrm{FoM}_2 = \frac{\mathrm{FoM}_1\cdot A_{\mathrm{range}}(\mathrm{dB})}{\theta_{\mathrm{peak\,error,VGA}}(^\circ)}$

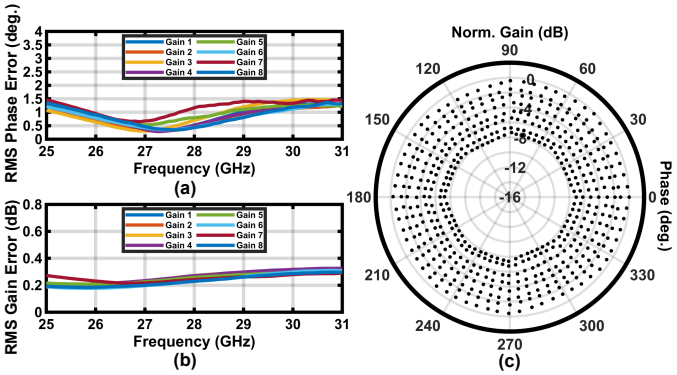

Fig. 8: Measured (a) rms phase error, (b) rms gain error of PS under different gain state settings, and (c) vector constellation at 28 GHz (without any calibration).

gain errors of the phase shift among different gain states. The phase and gain error remain $<1.47°$ and <0.32 dB, respectively, indicating high independence between the phase shift and gain control. Fig. 8(c) shows the measured vector constellation at 28 GHz. Under each gain state, the phase-state points form an approximately octagonal shape from the two ellipses, thereby minimizing the gain error without any calibration.

Table I summarizes the performance of the proposed VGPS and compares it with state-of-the-art active VGPS and PS. To the best of our knowledge, this design is the first to break the 1-mW dc power barrier among active VGPS, while maintaining the competitive error performance as well as orthogonal phase and gain controls. It also reaches the record high FoMs as defined at the bottom of Table I.

IV. CONCLUSION

This paper introduces a mm-wave current-reuse variable-gain phase shifter (VGPS) with dual-ellipse vector summation. Verified with silicon measurements, the VGPS achieves low rms phase and gain errors without any calibrations. Thanks to the current-reuse structure and compact transformer folding technique, it consumes less than 1 mW with a small form factor.

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