A 9.1% Peak Efficiency 243-318 GHz Frequency Doubler Using an In-Core Stepped-Impedance Network in 22 nm FDSOI CMOS

Finn-Niclas Stapelfeldt*[1], Thorben Schmidt*, Benjamin Schoch$, Vadim Issakov*
*Institute for CMOS Design, Technical University Braunschweig, Braunschweig, Germany
$Institute of Robust Power Semiconductor Systems, University of Stuttgart, Germany
[1]f.stapelfeldt@tu-braunschweig.de

***Abstract*— This paper presents a high-efficiency wideband frequency doubler operating above 240 GHz fabricated in a 22 nm FDSOI CMOS technology. The doubler core is based on a modified pseudo-differential common source topology. We propose an in-core stepped-impedance network, which serves several purposes: a) wideband large-signal core impedance matching for the second-harmonic (H2); b) acting as a reflector for the fundamental harmonic (H1), boosting the H1 amplitude at the gates and thereby enhancing the nonlinearity-based H2 generation at the drains; c) inherent power summation for H2 (in common-mode) and suppression of H1 (in differential mode). The presented doubler achieves a low conversion loss of 6.5 dB at 290 GHz in measurement. With a low DC power consumption P_{DC} of 10.8 mW at a P_{sat} of 3.35 dBm, this results in an outstanding peak efficiency η_{tot} of 9.1% at 290 GHz. Additionally, the circuit achieves a very wide 3-dB fractional bandwidth of 26.7%. The circuit occupies a minimal active chip area of only 0.032 mm^2. To the best of the authors' knowledge, this is the highest reported peak efficiency for a frequency doubler at frequencies around 300 GHz in an advanced CMOS node.**

***Keywords*— millimeter-wave, frequency doubler, low-power.**

I. Introduction

A wide available bandwidth is beneficial for both communication and radar systems. In wireless data applications, according to the Shannon capacity theorem, large bandwidth enables higher maximum achievable data rates. In radar systems, the range resolution is inversely proportional to the bandwidth of the transmitted signal, regardless of the modulation type (e.g., FMCW or PMCW). Higher frequency bands offer the potential for very wide unlicensed bandwidth, making the H-band (220 GHz – 330 GHz) attractive for future applications. However, it becomes increasingly difficult to achieve sufficiently high gain and P_{sat} from a transistor at these frequencies, as they approach the f_T/f_{max} limits of CMOS technologies.

Frequency multipliers are essential building blocks in millimeter-wave systems, commonly used in local oscillator (LO) signal distribution networks. Numerous works report multipliers with an output at D-band frequencies [1]. However, only few works report H-band frequency multipliers. These are typically realized in III/V processes [2] or SiGe HBT BiCMOS technologies [3], [4]. Only few works report H-band frequency multipliers in CMOS nodes [5], [6], [7]. Typically, most reported H-band frequency multipliers achieve peak efficiencies well below 3%. To address this, one can either: a) resort to III-V technologies to benefit from higher f_T/f_{max} [2], at the cost of limited integration capability; or b) employ

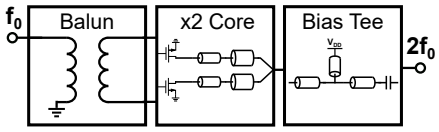

Fig. 1. Simplified block diagram of the proposed frequency doubler.

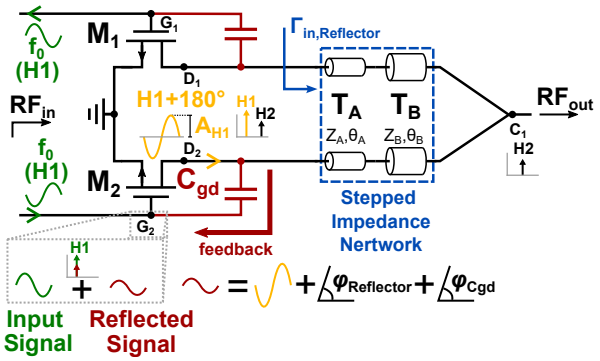

Fig. 2. Proposed doubler core with stepped-impedance network.

circuit techniques to improve efficiency and maximize P_{sat}, such as using harmonic reflectors and leakage cancellers in the frequency doubler core [6].

In this paper, we present a modified H-band pseudo-differential push-push frequency doubler. We propose incorporating a stepped-impedance network into the doubler core, as shown in Fig. 1. This enhances both P_{sat} and the operational bandwidth. Thanks to this technique, the circuit achieves an excellent efficiency of 9.1% and a P_{sat} of 3.35 dBm. To the best of the authors' knowledge, these are the highest reported values for a CMOS frequency doubler operating in the H-band.

II. Circuit Implementation

The frequency doubler in this work is based on a pseudo-differential common source push-push topology, as shown in Fig. 2. We expand the classical topology by adding an impedance transforming combiner network, which consists of stepped-impedance transmission lines. It serves several purposes: a) it enhances impedance matching for the second harmonic (H2) by presenting a more favorable load at the drains, which helps achieve wider bandwidth operation; b) it acts as a reflector for the fundamental harmonic (H1), which couples back to the gate and enhances the H1 amplitude. This enhancement, due to nonlinearity, increases the maximum achievable saturated output power at H2; and c) it inherently provides a power combining network for H2 (present in

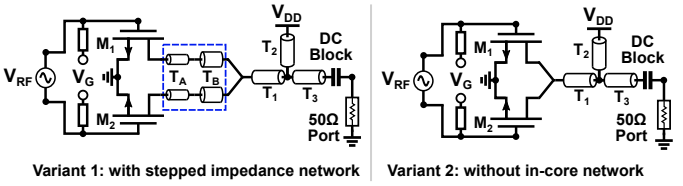

Fig. 3. Simulation testbenches to estimate the effect of in-core network.

common-mode) and a subtraction mechanism for H1 (available in differential mode).

The benefit of this approach is analyzed by a systematic comparison of the push-push doubler topology *with* and *without* the proposed in-core stepped-impedance network $T_{A,B}$ under different bias conditions. Fig. 3 shows the simplified simulation testbenches used only for the purpose of gaining an insight into this technique, where variant 1 is *with* and variant 2 is *without* the network. In these two testbenches the doubler core is driven differentially by a voltage source, applied directly at the gates of M_1 and M_2, i.e. excluding balun amplitude and phase imbalances to isolate the effects. The input amplitude was swept and at each input power level the elements of the matching network were resized to achieve best P_{sat}, as well as good small-signal conversion gain. The simulation results, depicted in Fig. 4, show that variant 2 (without in-core network) gate biased at $V_G = 0.32\,V$ reaches a P_{sat} of about $-2\,dBm$ and has a minimum conversion loss of $4.8\,dB$ at low input power levels. For a gate bias voltage of $V_G = 0.7\,V$, P_{sat} is improved significantly to around $3.2\,dBm$, yet the conversion loss is degraded to $8.9\,dB$. The higher conversion loss can be explained by the decreasing amplitude of the second order term ($n = 2$) for increasing bias voltage V_G, due to decrease of g'_m in the Taylor expansion for the drain current as function of gate voltage

$$i_D(v_G) = \sum \frac{1}{n!}\frac{\partial^n I_{D,Q}}{\partial V_{G,Q}^n} {v_G}^n = \sum \frac{1}{n!} {g_m}^{(n-1)} \cdot {v_G}^n, \quad (1)$$

where $v_G = A_{in} \cdot \cos \omega_{in} t$ and A_{in} is the input amplitude. Yet, for variant 1 this effect is mitigated, since the in-core network both boosts P_{sat} and reduces the conversion loss at any V_G. The boost is more pronounced at $V_G = 0.7\,V$, as seen in Fig. 4.

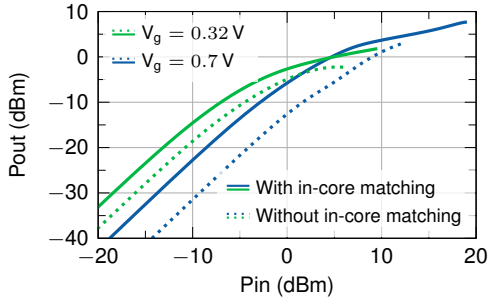

Fig. 4. Simulated P_{in} vs. P_{out} with and without in-core stepped-impedance network at two different DC gate bias levels V_G.

This effect can be explained by the properties of the proposed in-core stepped-impedance network in differential and common mode operation. Because the in-core TLine network offers a specific input impedance it can be used as a reflector. Hence, the fundamental frequency H1 is not canceled at this point, as it would be in variant 2, and it appears at the drains of M_1 and M_2 at points D1 and D2 in Fig. 2, respectively. It is then coupled back with a phase shift of φ_{refl} to the gate via the parasitic gate-drain capacitance C_{gd}, which presents a low impedance at H1. Additionally, the signal is phase shifted by the parasitic drain capacitance C_{gd} with a shift of $\varphi_{C_{gd}}$. Due to an inherent phase shift of φ_{CS} in common-source, the total phase shift of H1 in the loop is

$$\varphi_{loop} = \varphi_{CS} + \varphi_{refl} + \varphi_{C_{gd}}. \quad (2)$$

This can cause constructive interference of the reflected H1 with the input, boosting H1 at the gates of $M_{1,2}$

$$v_{G,@H1} = A_{in} \cdot \cos \omega_{in} t + A_{in} \cdot G_{loop,H1} \cdot \cos\left(\omega_{in} t + \varphi_{loop}\right). \quad (3)$$

We observe in simulation that boosting of H1 occurs not only for $\varphi_{loop} = 0°$, but over a wide range of phases

$$-120° < \varphi_{loop} < 120°. \quad (4)$$

The loop gain at H1 is below unity because of the low impedance presented by the lines $T_{A,B}$ at H1. Hence, there is no stability concern. This was verified by large-signal S-parameter (LSSP) simulation and ensuring that the μ factor is always above 1 for all input powers, as shown in Fig. 5. Stability was also verified in time domain by applying sharp pulses at all nodes and checking that no oscillations occur.

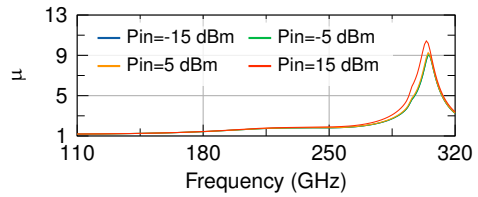

Fig. 5. Simulated μ factor under small- and large input power levels.

Next, Fig. 6 shows the amplitude of the fundamental frequency at point D_2 versus line impedance Z_A, while keeping Z_B at $80\,\Omega$. This shows that by adjusting the reflector, H1 can be boosted. Fig. 7 shows the loop phase φ_{loop} at H1. The loop phase is within the range for constructive interference.

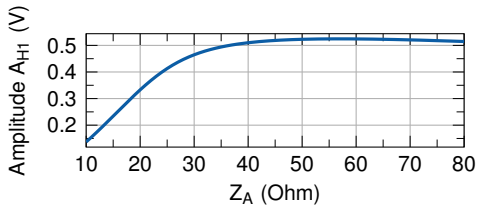

Fig. 6. Simulated amplitude of the fundamental frequency component A_{H1} at the drain of M_2 versus line impedance Z_A at a fixed impedance $Z_B = 80\,\Omega$ with electrical lengths $\theta_A = \theta_B = 45°$ at 280 GHz.

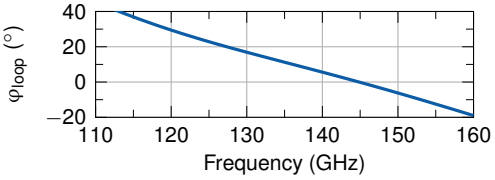

Fig. 7. Simulation of the loop phase shift φ_{loop} at H1.

Constructive interference of H1 boosts the generation of the second harmonic by increasing A_{in}, as seen by expanding Eq. 1 using trigonometric identities.

The proposed in-core network acts not only as a reflector at the drains of $M_{1,2}$, as explained previously, but also serves as an inherent power combiner network for the H2 (the desired harmonic) and provides wideband suppression for H1, as shown in Fig. 8.

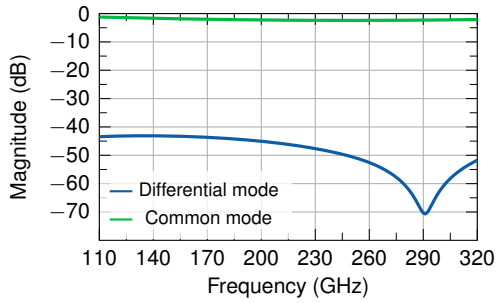

Fig. 8. S_{21} for a common and differential mode signal fed into the in-core stepped-impedance transmission lines network.

The impedance matching network can be designed for the doubler core to achieve high bandwidth, high P_{sat}, as well as low conversion loss simultaneously. Fig. 9 and Fig. 10 show heatmaps for different values of the line impedances Z_A and Z_B at a fixed electrical length (defined as $\theta = \beta \cdot l$), such that $\theta_{\text{total}} = \theta_A + \theta_B = 90°$ at 280 GHz. The heatmaps were generated for P_{sat} (Fig. 9) and the 3-dB bandwidth (Fig. 10).

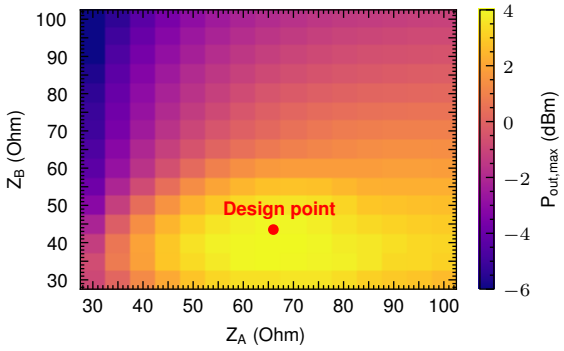

Fig. 9. Simulated maximum achievable output power $P_{\text{out,max}}$ depending on the characteristic line impedances Z_A and Z_B having electrical lengths of $\theta_A = \theta_B = 45°$ at 280 GHz.

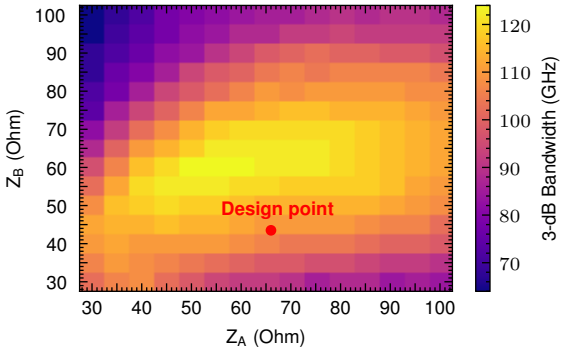

Fig. 10. Simulated maximum achievable 3-dB bandwidth depending on the characteristic line impedances Z_A and Z_B having electrical lengths of $\theta_A = \theta_B = 45°$ at 280 GHz.

The design point regarding the choice of $Z_{A,B}$ was chosen as a compromise between P_{sat} and 3-dB bandwidth.

The transistor widths of $W = 14.4\,\mu m$ and a gate length of $L = 20\,nm$ in the doubler core were chosen as a good design point for low conversion loss, high P_{sat} and low DC power consumption to achieve high efficiency. The optimal gate bias is $V_g = 0.7\,V$, while $V_{DD} = 0.8\,V$. Following Fig. 9 and Fig. 10, the line impedances Z_A and Z_B were designed to be $66\,\Omega$ and $44\,\Omega$. The lines are physically realized as grounded coplanar waveguides. The resulting physical line widths are $W_A = 2.7\,\mu m$ and $W_B = 9.7\,\mu m$ with a spacing of $S_A = 10\,\mu m$ and $S_B = 6.5\,\mu m$ to the ground walls. The electrical lengths amount to $\theta_A = \theta_B = 45°$ at 280 GHz. This design choice trades off a small amount of bandwidth to reach a higher P_{sat}.

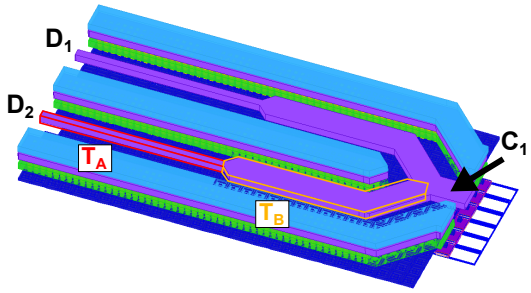

Fig. 11. Physical realization of the stepped-impedance network based on grounded coplanar waveguides in the doubler core highlighting T_A and T_B.

III. Measurement Results

The proposed frequency doubler is fabricated in a 22 nm FDSOI CMOS technology. The chip micrograph of the doubler is depicted in Fig. 12. A $0\,\Omega$ metal grid surrounds the active area to ensure a good RF ground and additional large capacitors are added to shunt low frequency noise. The design occupies an active area of approximately $0.032\,mm^2$.

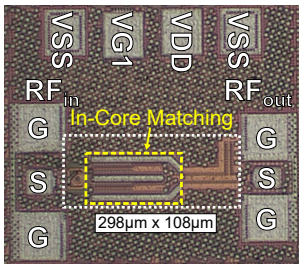

Fig. 12. Chip microphotograph (active core size $298\mu m \times 108\,\mu m$.)

A Keysight PNA-X N5244B and VDI frequency extenders are used for both small and large-signal measurements. The output port was calibrated using short, open, and load (SOL) structures on an impedance standard substrate (ISS) and an on-chip Thru both in the D-band and H-band was measured for power-loss correction for small- and large-signal measurements respectively.

Fig. 13 shows an excellent agreement between the measured and simulated output matching S_{22} for the frequency doubler in the H-band. The frequency dependent simulated and measured saturated output power P_{sat} is depicted in Fig. 14.

Table 1. Summary of measurement results and comparison with state-of-the-art frequency doublers in CMOS and BiCMOS.

Reference	[5]	[6]	[8]	[7]	[4]	**This Work**
Technology	28 nm CMOS	65 nm CMOS	90 nm SiGe	65 nm FDSOI	130 nm SiGe	**22 nm FDSOI**
Frequency (GHz)	208-232	237-263	220-250	272-341	284-328	**243-318**
Pre-driver	1-stage	No	No	5-stage	1-stage	**No**
BW_{3dB}[e] (%)	11.3	10.4	12.7	16.3	14.9	**26.7**
Peak CG (dB)	-7.2	-4	-15.5	3.8	-0.1	**-6.5**[b]
Peak η_{tot}[a]	0.1[c]	2.87	1.08	0.32[c]	0.97	**9.1**[b,e]
P_{sat} (dBm)	-4.9	0.9	1.8	-3	-0.9	**3.35**[b]
P_{DC} (mW)	26.4	37	90	159.6	84	**10.8**[e]
Active Area (mm^2)	NA	0.051[d]	0.12[d]	0.1	0.223[d]	**0.032**

[a] $\eta_{tot} = \frac{P_{out,2nd}}{P_{in}+P_{DC}}$, [b] at $f_{out} = 290$ GHz, [c] extracted from figure, [d] estimated from chip micrograph, [e] at P_{sat}

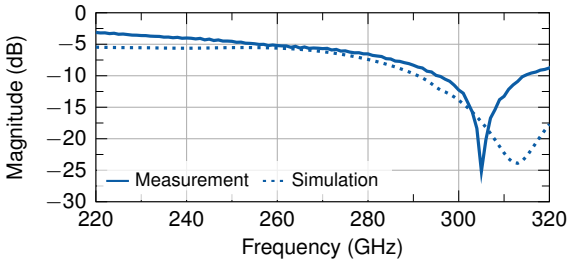

Fig. 13. Measured and simulated output matching (S_{22}).

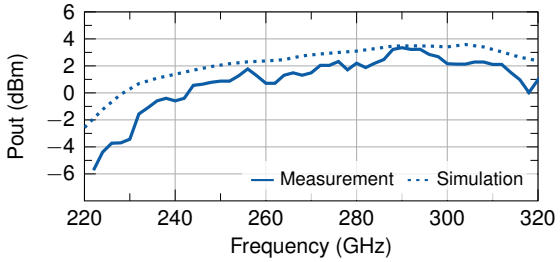

Fig. 14. Measured P_{sat} vs. output frequency.

The doubler achieves a measured 3 dB-bandwidth of 75 GHz in large-signal operation, as well as a peak P_{sat} of 3.35 dBm at 290 GHz. The measured performance matches the design considerations in Fig. 9 and Fig. 10 very closely.

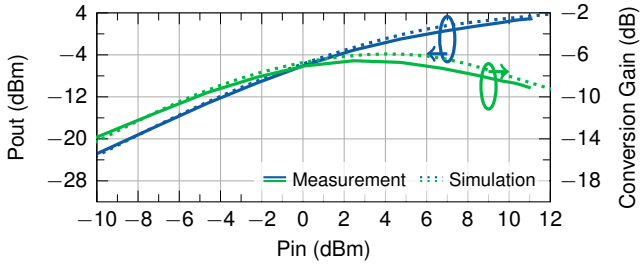

Fig. 15. Measured and simulated P_{out} vs. P_{in} at 290 GHz.

Fig. 15 visualizes the measured and simulated output power P_{out} versus the input power P_{in} at the second harmonic at an input frequency of $f_{in} = 145$ GHz. This proves the feasibility of the concept introduced in this work showing a conversion loss comparable to that of a classical push-push frequency doubler, while also achieving a high P_{sat} of 3.35 dBm and a total efficiency η_{tot} of 9.1 % with a DC power consumption of 10.8 mW in large-signal operation.

Finally, Table 1 compares the proposed frequency doubler with state-of-the-art publications. The circuit compares favorably to the state of the art in terms of efficiency, bandwidth, P_{sat} and size of the active area.

IV. Conclusion

We have presented a modified push-push frequency doubler with a stepped impedance in-core network employing feedback to boost the fundamental component, while ensuring circuit stability. A higher H1 amplitude at the gates boosts the generation of the second harmonic H2. The circuit achieves a high saturated output power P_{sat} of 3.35 dBm and a 3-dB bandwidth of 75 GHz. To the best of the authors' knowledge this work reports the highest efficiency of 9.1 % for an H-Band frequency doubler in an advanced CMOS technology node.

V. Acknowledgment

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