A 23.5-fJ/b/dB 15.2-Gb/s/pin Switched-Capacitor-Driven On-Chip Link with Half-VDD DC Biasing and ISI Mitigation

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***Abstract*— This paper presents a switched-capacitor-driven on-chip interface (S-CDI) that enhances signal integrity and maintains a stable channel DC bias at $V_{DD}/2$. It employs alternating pre-charging and charge-sharing using dual series capacitors (C_{UP}/C_{DN}). This approach enables the use of smaller capacitance while maintaining comparable signal swing to that of prior cap-driven interfaces, leading to higher bandwidth and improved eye-opening margin. Fabricated in a 28 nm CMOS process, the S-CDI achieves 15.2 Gb/s and 13.8 Gb/s over a 6-mm on-chip interconnect for PRBS7 and PRBS31 patterns, respectively. It demonstrates the fastest normalized speed among prior arts: 316 Gb/s·mm²/μm² and 286.9 Gb/s·mm²/μm² for PRBS7 and PRBS31. At 15.2 Gb/s with PRBS7, it achieves 468 fJ/b energy efficiency and a FoM_{dB} of 23.5 fJ/b/dB.**

Keywords—Capacitively-driven interface, switched-capacitor, on-chip interconnect, DC biasing

I. Introduction

Technology scaling reduces transistor delay but leads to an increase in global interconnect delay [1-2]. Segmenting interconnects with repeaters mitigates these delays but increases power consumption. Implementing a series capacitor (C_C) as source impedance (Fig. 1; top) expands bandwidth and reduces power consumption [3]. Reducing the ratio (α) of C_C over wire capacitance (C_W) enhances the pre-emphasis effect but reduces signal swing (V_{PP}), as in $V_{PP,conv} = V_{DD}\alpha/(\alpha+1)$. Also, such capacitor-driven on-chip interfaces (CDIs) leave the channel floating with undefined DC bias. Prior solutions typically used differential signaling to establish the channel DC bias (V_{CM}), which compromises pin efficiency [4-6].

Recent single-ended signaling methods (Fig. 1; bottom left) force the channel to GND at four consecutive '0's [7] or VDD at '1' detection [8]. However, GND-forcing suffers from increased channel leakage and ISI in toggling patterns, limiting its use to PRBS7 patterns [7], while VDD-forcing precludes feedforward equalization (FFE) due to insufficient timing margin [8], both constraining their effectiveness in lossy channels (e.g. DRAM global bus lines).

This paper proposes a switched-capacitor-driven on-chip interface (S-CDI) that employs dual series capacitors (C_{UP}/C_{DN}) with alternating pre-charging and charge-sharing operations to enhance signal integrity and maintains V_{CM} at $V_{DD}/2$ (Fig. 1; bottom right). When D_{IN} = 0/1, C_{UP}/C_{DN} is pre-charged to V_{DD} while C_{DN}/C_{UP} drives boosted 0/1, enabling smaller C_C for improved bandwidth with signal boosting (Fig. 2; top).

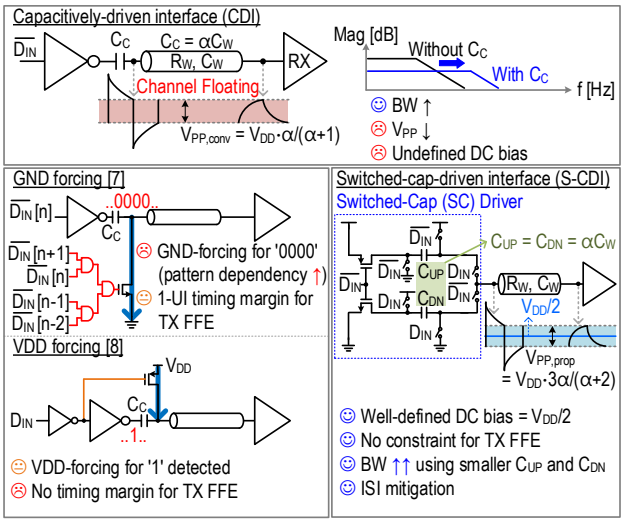


Fig. 1. Conventional CDI (top), prior art (bottom left), and proposed SC driver (bottom right).

This method enables the use of smaller series capacitances to achieve comparable signal swing to that of prior cap-driven interfaces, thereby enhancing bandwidth and eye-opening (EO) margin. Furthermore, this driver mitigates leakage and ISI in toggling patterns by setting the channel's DC bias to $V_{DD}/2$, which improves the overall signal integrity. Adjusting the ratio (α) of C_{UP} and C_{DN} to C_W, where $C_{UP} = C_{DN} = \alpha C_W$, enables the optimization of bandwidth and swing for various applications, effectively balancing performance with power consumption (Fig. 2; bottom).

II. Proposed S-CDI Transceiver

A. Analysis of Switched-Capacitor Driver

Fig. 3 shows the switched-capacitor (SC) driver's operation, demonstrating $V_{CM} = V_{DD}/2$ through pre-charging and charge-sharing, with corresponding output voltage (V_N) variations in response to the input data (D_{IN}) transitions. In the example shown, with D_{IN} being 0, the output node (N) is driven to '0', while C_{UP} (=αC_W) is pre-charged to V_{DD}. The output voltage at this stage is denoted as $V_{N,0}^{(n)}$, representing the V_N when D_{IN} = 0. Then, when D_{IN} transitions from 0 to 1, C_{UP} discharges its stored charge to N, resulting in a boosted '1' at N, while C_{DN} (=αC_W) is pre-charged to V_{DD}. The charge sharing between C_{UP} and C_W leads to a new output voltage, $V_{N,1}^{(n)}$, representing the V_N when D_{IN} = 1. This voltage is given by $V_{N,1}^{(n)} = [V_{N,0}^{(n)}+2\alpha V_{DD}]/(1+\alpha)$. Similarly, when D_{IN} switches from 1 back to 0, the charge sharing between

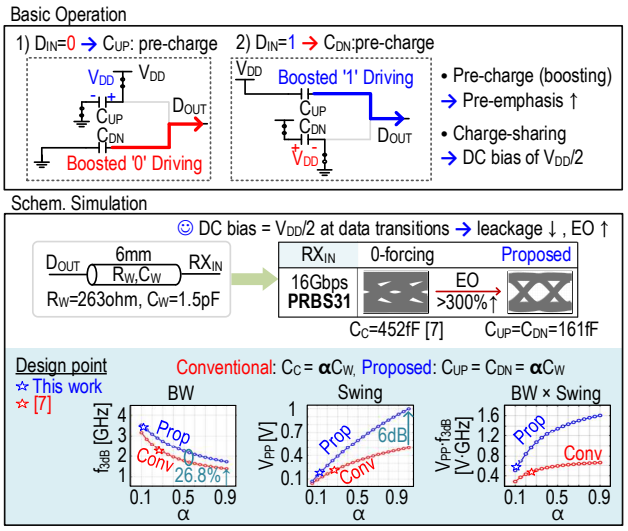


Fig. 2. Basic operation and key advantages of the SC driver.

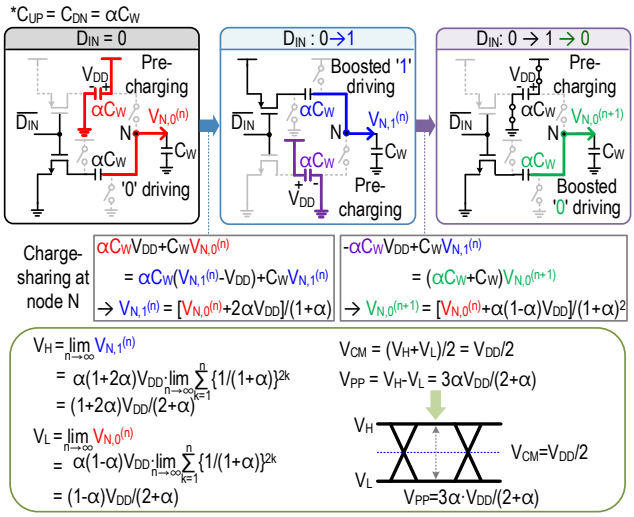


Fig. 3. Pre-charging and charge-sharing mechanisms.

C_{DN} and C_W leads to a new output voltage, $V_{N,0}^{(n+1)}$, given by $V_{N,0}^{(n+1)} = [V_{N,0}^{(n)}+\alpha(1-\alpha)V_{DD}]/(1+\alpha)2$.

With these repeated transitions, the output voltage levels, V_H and V_L, converge to $V_H = (1+2\alpha)V_{DD}/(2+\alpha)$ and $V_L = (1-\alpha)V_{DD}/(2+\alpha)$. These establish a constant DC bias $V_{CM} = (V_H+V_L)/2 = V_{DD}/2$, and a peak-to-peak voltage swing $V_{PP} = V_H-V_L = 3\alpha V_{DD}/(2+\alpha)$.

B. Overall Architecture

The overall architecture of the S-CDI is shown in Fig. 4. The transmitter (TX) includes a PRBS generator, a 64:4 MUX, a re-timer and two 4:1 serializers (SER) followed by a pre-driver. One generates D_{IN} signals for the main SC driver (SC driver$_{MAIN}$) and the other enables FFE via SC driver$_{POST}$ with $C_{UP/DN,POST} = \beta \times C_{UP/DN,MAIN}$ for 1st post-cursor compensation ($\beta = 0.3$). The SC driver then transmits the data through a 6-mm on-chip channel.

The receiver (RX) features dynamic comparators with NMOS input pairs, a 7-bit RDAC for generating the reference voltage (V_{REF}), a re-timer, a 4:64 DEMUX, and a PRBS checker.

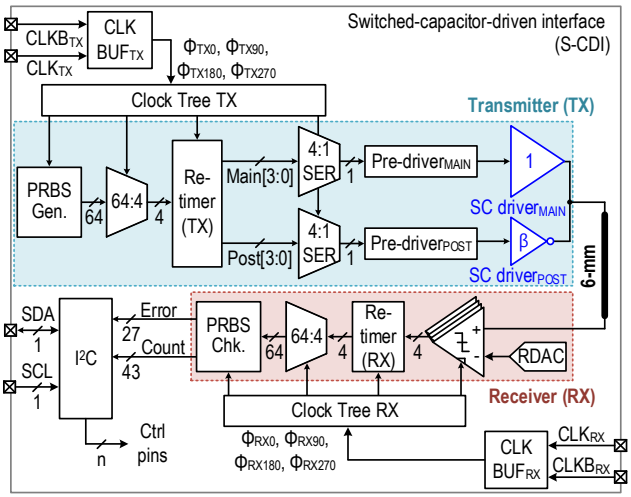


Fig. 4. Overall architecture of the S-CDI.

The clock path includes a CLKBUF$_{TX/RX}$ (CML buffer, a CML-to-CMOS converter, and a quadrature-phase clock generator) and a clock tree for driving the data path.

The PRBS generator, checker, and I²C are implemented in the logic area. The I²C controls internal blocks and reads error and count values from the PRBS checker for BER computation.

Fig. 5 shows the schematics of the re-timer and 4:1 SER. The NAND-based SER eliminates the need for a 1UI pulse generator by using a delayed clocking mechanism through NAND gates. This design enables low-power multiplexing, but it can be susceptible to glitches with narrow data-to-clock margins. To prevent this, the re-timer aligns the data streams with their corresponding clock phases, ensuring a 1UI margin before the SER combines these streams into a single output (SER_{OUT}), as illustrated in the timing diagram.

The series capacitor's pre-emphasis effect helps mitigate ISI and optimize the horizontal eye margin. The SC driver is designed to control this effect by adjusting the pre-charge current with the SW_{PC} size control (Fig. 6). A SW_{PC} utilizes a 5-bit binary-weighted control scheme to adjust the number of active sub-switches (n_{SW}), set by default at $n_{SW} = 11$. Based on the on-chip channel characteristics and the measurement setup (Fig. 7), the results (Fig. 6; top right) show that the horizontal eye margin varies with n_{SW} for different data rates (PRBS7), indicating that optimizing n_{SW} enhances signal integrity. Higher data rates require a greater n_{SW} for optimal performance.

III. Measurement Results

Fig. 7 shows the on-chip channel characteristics and measurement setup. The test chip employs a 6-mm on-chip channel with cross-sectional area (A_C) of 1.73 μm², R_W of 264 Ω, C_W of 1.41 pF, and $C_{UP} = C_{DN}$ of 161 fF ($\alpha = 0.114$). At the Nyquist frequency corresponding to 15.2 Gb/s ($f_{Nyquist}$ = 7.6 GHz), the insertion loss reaches -19.9 dB, indicating a highly lossy channel environment. Given that signal bandwidth degrades with increased channel length (L) and decreased A_C, normalized speed (f_N = data rate × L^2/A_C) is used for channel-aware performance comparison [5], [7]. An MP1800A PPG provides differential TX/RX clocks. The on-chip PRBS generator produces test patterns (PRBS7/15/31),

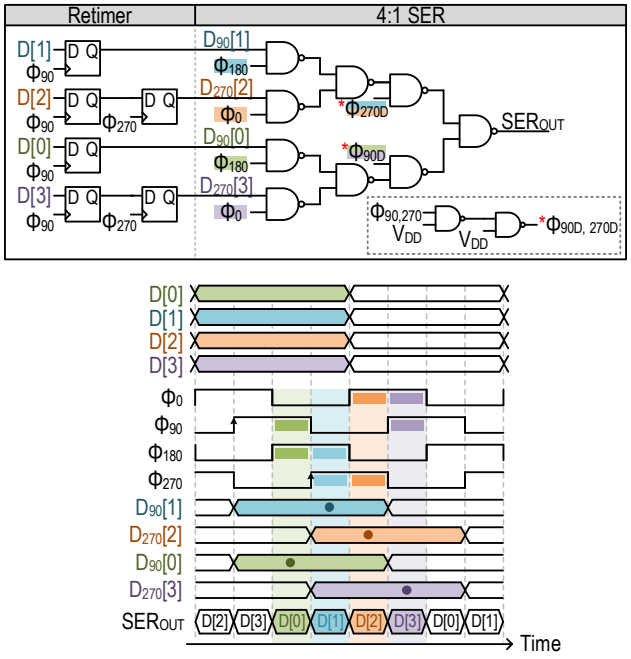


Fig. 5. Schematics and timing diagrams for the re-timer and 4:1 serializer.

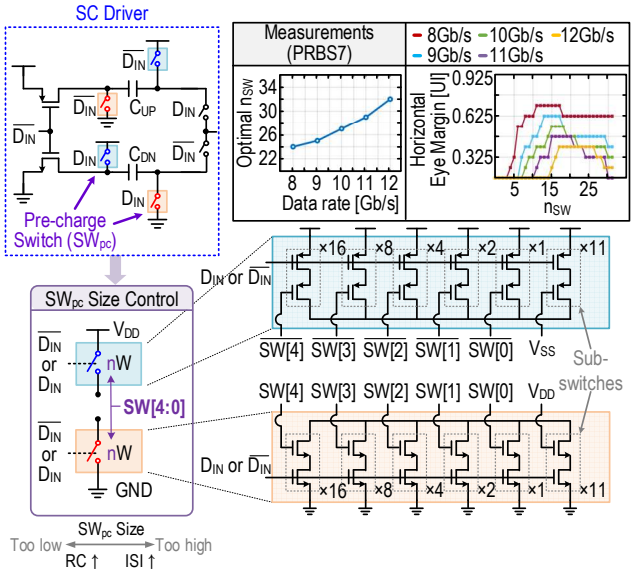


Fig. 6. Schematics of the SC driver's pre-charge switch (SW_{PC}) and its size control impacts on the eye margin.

and the PRBS checker outputs a 43-bit received-bit count and a 27-bit error count for BER measurement.

Fig. 8 shows the measured 2D Shmoo plots, which present BER distributions over a V_{REF} range of 425 mV to 575 mV and a 1UI sampling window, with step sizes of 5 mV and 0.04 UI, respectively. The results consistently demonstrate a stable DC bias at $V_{DD}/2$ across all tested patterns. The S-CDI achieves data rates over 12 Gb/s even without FFE.

The timing margin is further analyzed through the measured bathtub curves shown in Fig. 9. For each PRBS pattern, both with and without FFE, the curves reveal the impact of equalization on timing margin and signal integrity. At 15.2 Gb/s (PRBS7), the interface shows a margin of 0.16 UI; at 14 Gb/s (PRBS15), the margin is 0.08 UI; and at 13.8 Gb/s (PRBS31), it is 0.04 UI. All measurements are taken

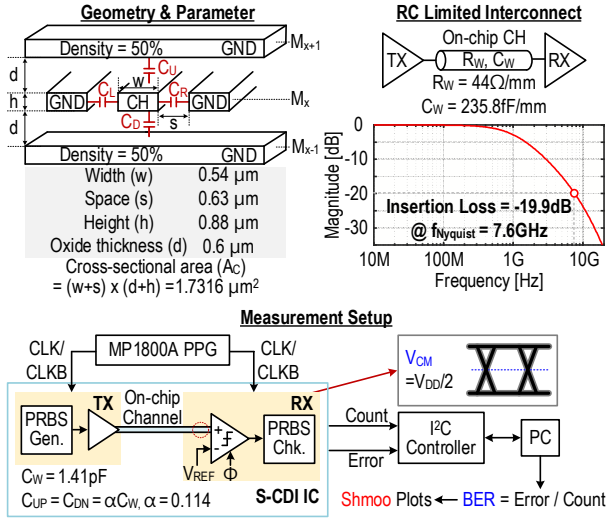


Fig. 7. On-chip channel characteristics and measurement setup.

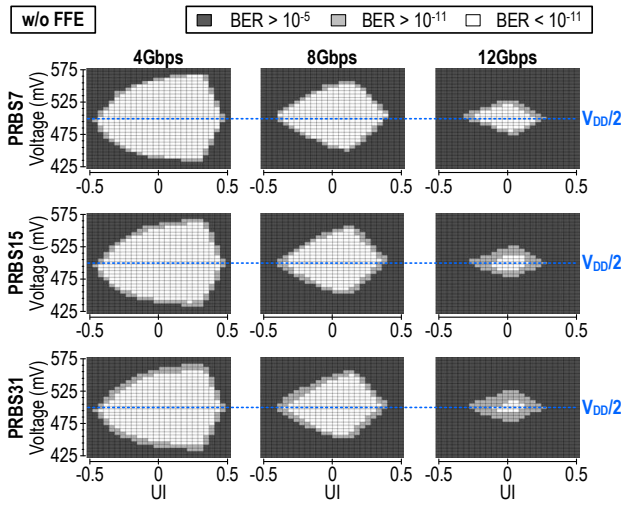


Fig. 8. Measured eye-opening shmoo plots without FFE.

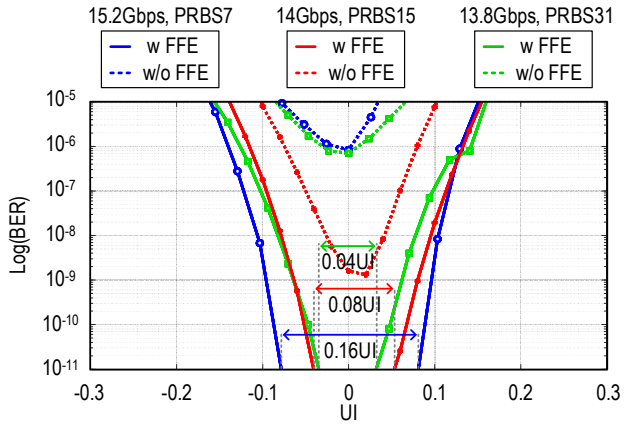


Fig. 9. Measured bathtub curves at maximum data rates for each pattern.

with V_{REF} fixed at $V_{DD}/2$ = 0.5 V, ensuring consistent bias conditions across test scenarios.

Table I and Fig. 10 show the performance summary and comparison. Two FoMs from prior literature [3-8] are compared: FoM_L = energy per bit (E_B)/L × pin number (1 and 2 for single-ended and differential signaling), and FoM_{dB} = E_B/insertion loss (dB). The proposed S-CDI achieves the fastest f_N of 316 Gb/s·mm²/µm² and 286.9 Gb/s·mm²/µm² for PRBS7 and PRBS31 patterns and the best FoM_{dB}, even

TABLE. I
COMPARISON WITH STATE-OF-THE-ART CDI

	ISSCC'22 [7]	VLSI'23	JSSC'24 [8]	This work		
Technology	65-nm CMOS	5-nm FinFET	28-nm CMOS	28-nm CMOS		
Signaling	Single-ended NRZ	Single-ended NRZ	Single-ended PAM-4	Single-ended NRZ		
Supply Voltage [V]	1.0/1.2 (TX/RX)	0.75	1.0	1.0		
Channel (CH) Length **L** [mm]	5.6	1.2	4.0	**6.0**		
CH Cross-section Area **Ac** [μm²]	1.63	N/A	3.18**	1.73		
Insertion Loss **IL** [dB]	< 10	4.5	4.3	**19.94**	**18.89**	**18.7**
Data Pattern	PRBS7	PRBS31	PRBS7/15/31	**PRBS7**	**PRBS15**	**PRBS31**
Data-rate f_D [Gb/s/pin]	12.0	25.2	24.0	15.2	14	13.8
Energy efficiency E_B [fJ/b]	441	190*	458	468	463.6	462.3
Normalized Speed f_N[1] [Gb/s·mm²/μm²]	231.21	N/A	120.75	**316.01**	**291**	**286.9**
FoM_L[2] [fJ/b/mm]	78.8	158.3*	114.5	**78**	**77.3**	**77.1**
FoM_{dB}[3] [fJ/b/dB]	> 44.1	42.2*	106.5	**23.5**	**24.5**	**24.7**

1. Normalized Speed $f_N = f_D \times L^2/A_C$ [5, 7].
2. $FoM_L = E_B/L$ [5, 6, 7, 8].
3. $FoM_{dB} = E_B/IL$.
(*): Including PLL power.
(**): Calculated using typical technology parameters.

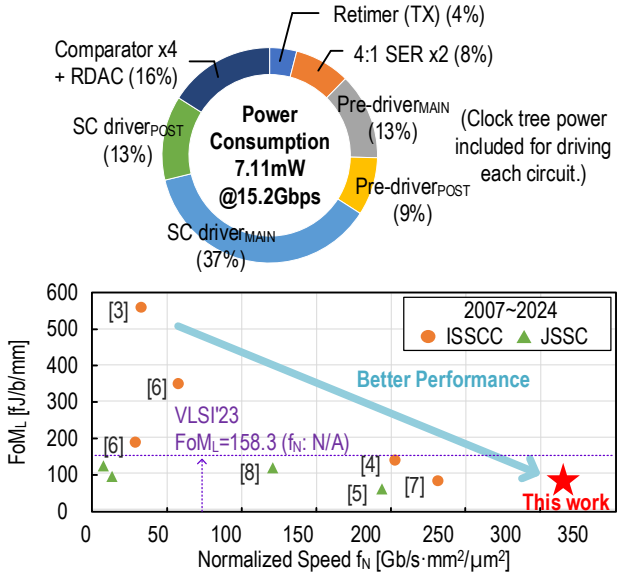


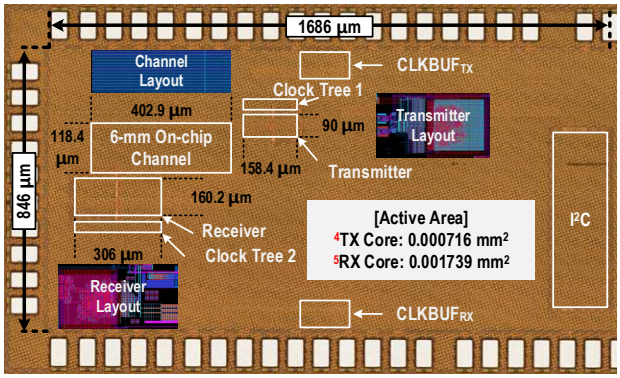
Fig. 10. Power breakdown and comparison (FoM_L vs. normalized speed f_N) of prior CDIs.

across the channel with >10dB higher insertion loss compared to prior CDIs. The prototype consumes 7.11 mW at 15.2 Gb/s, operating at V_{DD} = 1V.

Fig. 11 shows a die photo of the chip, fabricated in a 28 nm CMOS process, with a detailed layout. The active areas of the TX and RX cores are 0.000716 mm² and 0.001739 mm², respectively.

IV. CONCLUSION

This paper presents a switched-capacitor-driven on-chip interface (S-CDI) that eliminates the need for dedicated biasing circuitry. The alternating pre-charge and charge-sharing mechanism maintains a stable DC bias at $V_{DD}/2$ and enables signal boosting with reduced capacitor size. Implemented in a 28 nm CMOS process, the S-CDI operates at 15.2 Gb/s (PRBS7) and 13.8 Gb/s (PRBS31) over a 6-mm on-chip interconnect, achieving normalized speeds of 316 and 286.9 Gb/s·mm²/μm², respectively. The design achieves



4TX Core = 4:1 SER + Pre-driver + SC driver.
5RX Core = Comparator + RDAC.

Fig. 11. Chip micrograph and detailed layout.

468 fJ/b energy efficiency and a FoM_{dB} of 23.5 fJ/b/dB, demonstrating competitive performance among prior capacitor-driven interfaces.

ACKNOWLEDGMENT

This work was partly supported by the Institute of Information & communications Technology Planning & Evaluation (IITP) grants (RS-2022-II221171, RS-2022-II220991, RS-2023-00256472) and the National Research Foundation of Korea (NRF) grant (BK21), funded by the Korea government (MSIT). This chip fabrication and EDA Tool were supported by the IC Design Education Center (IDEC).

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