ART-PoL: An Auto-Reconfigurable Tri-Mode PoL for 48V-to-1V 200A Power Delivery with Enhanced Load Response and V_{IN}-Ramp-Synchronous Startup

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***Abstract*—A GaN-based 20-level series-capacitor (SC) 48V-to-1V buck is presented for point-of-load (PoL) applications, capable of delivering 200A load current (I_O). To address the inherent shortcoming of limited I_O step-up transient response in multi-level SC buck, an LDO mode is incorporated, reducing the output dip by 48% and recovery time by 45% for 100A/500ns load transient. To break through the bottleneck in reliable startup, an active-input-division (AID) mode is devised to achieve sequential balancing of the 19 flying capacitors with a maximum input (V_{IN}) rising rate of 10V/ms. These two modes share the power devices with normal switching mode, realizing an auto-reconfigurable tri-mode (ART) scheme for compact design. Fabricated in a 180nm BCD process, the 1MHz ART-PoL demonstrates a peak efficiency of 87.4%, while retaining above 80% efficiency over 85% of the full load range.**

***Keywords*—Direct 48V-to-1V conversion, large load current, enhanced transient response, V_{IN}-ramp-synchronous startup.**

I. Introduction

As the power demands of data center processors for AI and HPC keep rising, 48V power delivery architecture for servers is being widely accepted by the industry to suppress the distribution power loss [1]. However, the traditional multi-phase buck converter [2] struggles to balance the trade-off between high efficiency and high step-down ratio when converting 48V to sub-1V core voltage. To overcome this, multi-level series-capacitor buck (MLSCB) [3-9] emerges to efficiently accomplish a direct 48V-to-1V conversion, while delivering beyond 100A load current (I_O). As shown in Fig. 1(a), a typical MLSCB consists of a switched-capacitor stage to pre-regulate the high input (V_{IN}) to a lower intermediate voltage as V_{IN}/K, with K as the level number. Then, it employs a multi-phase inductive stage to achieve large current delivery. It has been analyzed that increasing K can scale down the normalized passive component volume (Q_P) and switch stress (Q_S), suggesting improved power density and conversion efficiency [1]. However, increasing K makes it quite challenging to balance the dynamic performance in terms of load and line transient responses, which must be resolved for practical applications.

Specifically, when K increases and V_{IN}/K decreases, the inductance (L) can be reduced proportionally to remain the same inductor current (I_L) ripple. However, the energizing voltage across L becomes ($V_{IN}/K-V_O$), which drops sharper than L with K increment. As a result, the I_L rising rate is reduced, degrading the I_O step-up response. For even worse, as shown in Fig. 1(b), MLSCB suffers from limited maximum duty cycle (D) [4]. This fails concurrent energizing of all inductors, exacerbating the sluggish load response as I_O changes from light load to heavy load. Consequently, the significant output (V_O) dip can induce

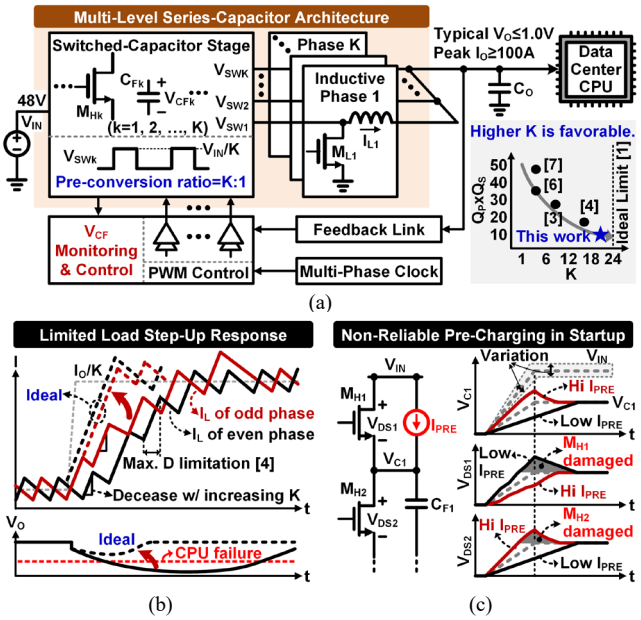

Fig. 1. Design challenges of multi-level series-capacitor buck: (a) system architecture, (b) limited load step-up response, and (c) non-reliable startup.

potential processor black-out. To avoid this, a dual phase-charging scheme was reported for simultaneous energizing of the 2 inductors in 2-level SCB [9]. However, it generally requires 2*(K−1) additional power devices to short all the switching nodes during transient, degrading system power density significantly. Additionally, due to incorporating flying capacitors (C_{Fk}), MLSCB encounters line transient response issue during startup for robust hybrid switching. The existing startup methods [5, 9] pre-charge C_{Fk} when V_{IN} has stabilized at the final level, incommensurate to various power-on sequences. Besides, they need high-voltage power devices to withstand the full V_{IN} stress, partly counteracting the benefit of hybrid topology. Thus, it is highly desirable to achieve a V_{IN}-ramp-synchronous startup to fully take the advantages of MLSCB. However, this is not straightforward. As shown in Fig. 1(c), a pre-charging circuit with a low I_{PRE} can incur excessive drain-source voltage (V_{DS1}) over the safe operating area (SOA) of the power device M_{H1}, while a high I_{PRE} would induce V_{DS2} overshoot to damage the transistor M_{H2}. To circumvent this, the startup process in [8] employs the normal switching of the power stage for level-by-level balance. However, it is merely feasible for limited V_{IN} slope.

To navigate the above challenges, this work designs a 20-level GaN PoL converter based on SCB structure, featuring auto-reconfigurable tri-mode (ART) control. Without adding any additional power devices, it can concurrently energize all 20 inductors to enhance I_O step-up response and achieves V_{IN}-ramp-synchronous startup independent of V_{IN} slew rate.

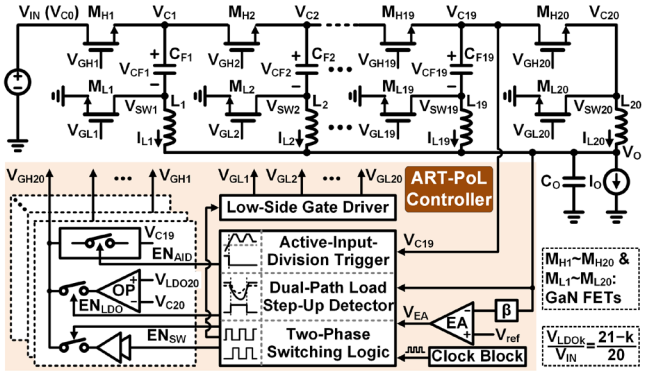

Fig. 2. Proposed GaN-based auto-reconfigurable tri-mode (ART) point-of-load (PoL) series-capacitor buck.

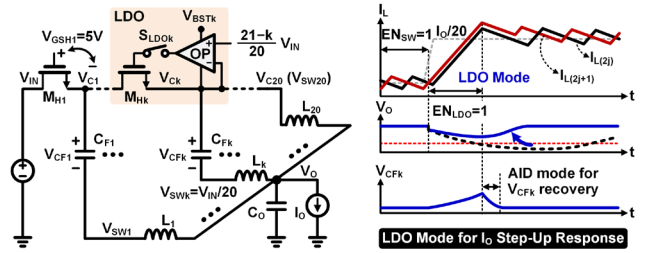

Fig. 3. Basic principle and operating waveforms of the proposed LDO mode to enhance the I_O step-up response.

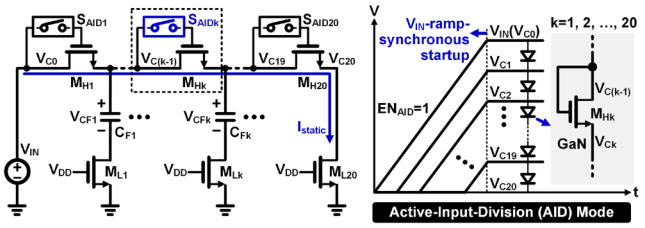

Fig. 4. Proposed active-input-division (AID) mode to achieve V_{IN}-ramp-synchronous startup regardless of V_{IN}-ramp rate.

II. Proposed GaN-Based ART-PoL Converter

Fig. 2 shows the system architecture of the designed ART-PoL converter. In specific, 20 SC branches are stacked using high-side GaN devices M_{H1}~M_{H20} and flying capacitors C_{F1}~C_{F19}, reducing switch stress to $V_{IN}/20$ for low power loss. They are subsequently connected to 20 inductive phases consisting of low-side GaN switches M_{L1}~M_{L20} and inductors L_1~L_{20} for large I_O. Under normal operating, the even and odd power branches are grouped respectively for interleaved switching to regulate V_O. As Io rises, a dual-path load step-up detector captures this event instantly to trigger LDO mode. Thus, as shown in Fig. 3, assisted by an adaptive-biasing op-amp (OP), the k^{th} high-side device M_{Hk} is reconfigured as an LDO, regulating all V_{Ck} to V_{IN}*(21−k)/20. Thus, all inductors, L_1~L_{20}, are energized in parallel, enhancing the I_O step-up response. To break through the startup bottleneck, an active-input-division (AID) mode, as shown in Fig. 4, is devised to connect each M_{Hk} as an active diode when V_{IN} ramps up, distributing V_{IN} to the nodes V_{C1}~V_{C19} evenly. By clamping the nodes V_{SW1}~V_{SW20} at ground with M_{L1}~M_{L20}, each voltage V_{CFk} on C_{Fk} is biased at V_{IN}*(1−k/20), accomplishing reliable startup without any overstressing risks, regardless of V_{IN}-ramp rate. As V_{C19} is established, the AID mode automatically ends to initialize the normal switching. Note that AID mode is also applied after LDO mode to swiftly balance V_{C1}~V_{C19}.

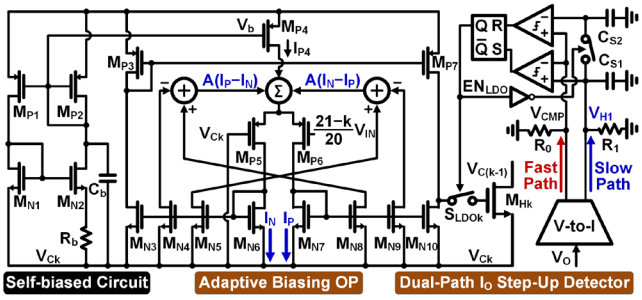

Fig. 5. Implementation of the proposed LDO mode by reusing the high-side power devices.

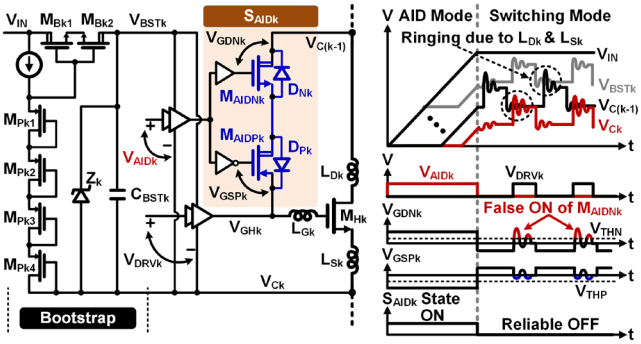

Fig. 6. Circuit design of the proposed active-input-division (AID) mode with immunity to parasitic inductances.

III. Circuit Implementations

Fig. 5 details the LDO mode design, engaging in two efforts to enhance I_O step-up response. Firstly, the adaptive biasing OP [10] is adopted to configure each M_{Hk} as a high-bandwidth LDO, regulating V_{Ck} to bias L_k positively. By such, it achieves concurrent energizing of all the inductors. The OP for M_{H1} is omitted by driving it as a switch to clamp V_{C1} at V_{IN}. In circuit design, the adaptive-biasing OP employs positive feedback for fast dynamic response. For this, it senses the absolute difference $|I_N-I_P|$ of the input currents and adds it up to the tail current I_{P4}. This enlarges $|I_N-I_P|$ in turn due to the improved transconductance of the input stage, enabling fast dynamic response with low static current. Secondly, a dual-path I_O step-up detector is designed to monitor load transient occasion, helping suppress V_O droop. Rather than using a fixed reference, it generates fast (V_{CMP}) and slow (V_{H1}) copies of V_O for dynamic comparison. As V_O abruptly drops down due to I_O step-up, V_{CMP} follows up to cross V_{H1}, activating LDO mode instantly for prompt response. Meanwhile, V_{H1} is sampled by C_{S2} as V_{H2}, marking the target level of V_{CMP} to end LDO mode for minimizing V_O overshoot. A self-biased module is designed to generate biasing currents in the floating voltage domain.

Fig. 6 depicts the implementation of the AID mode for reliable startup. During this mode, the k^{th} high-side power device M_{Hk} is diode-connected by the switch S_{AIDk}. As a result, the gate-source voltage (V_{GSk}) of M_{Hk} is biased at $V_{IN}/20$, close to the GaN transistor's threshold. Thus, the resultant static current I_{static} is sufficiently low for practical application. With a clear principle, the design of S_{AIDk} is not straightforward due to the parasitic inductances L_{Dk} and L_{Sk} of M_{Hk}. Ideally, S_{AIDk} could be realized by a single NMOS M_{AIDNk}, which is turned on in the AID mode by the high-effective drive signal V_{AIDk}. While in switching mode, V_{AIDk} keeps low to turn off M_{AIDNk}. However, L_{Dk} and L_{Sk} cause ringing, incurring temporarily higher V_{Ck} than $V_{C(k-1)}$, which

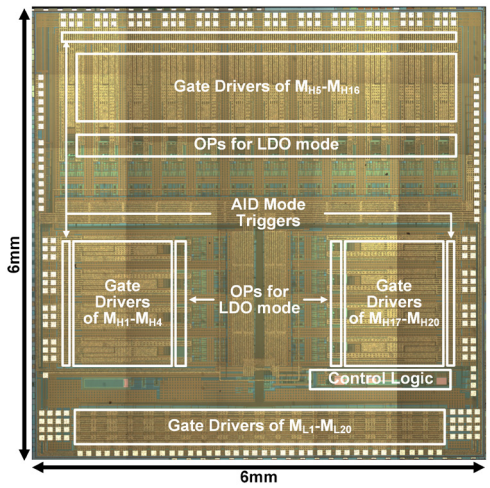

Fig. 7. Die photo.

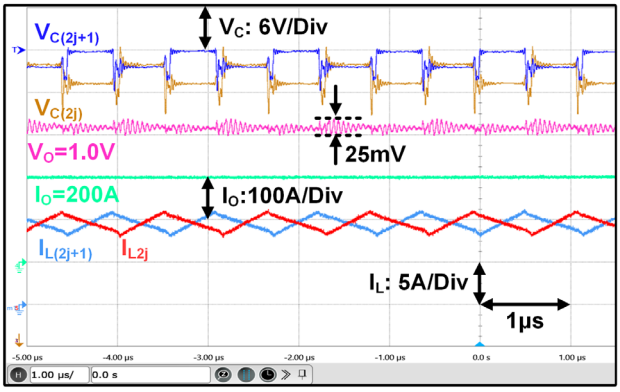

Fig. 8. Measured switching waveforms at steady state with 200A load.

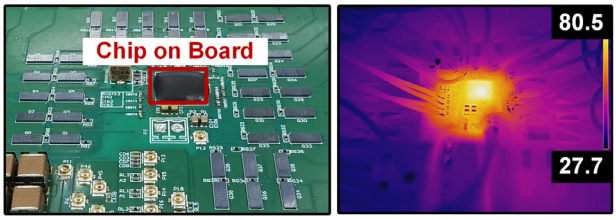

Fig. 9. PCB photo with 40 GaN transistors and thermal image in normal switching mode.

would falsely turn on M_{AIDNk}. To combat this, an additional PMOS M_{AIDPk} is drain-to-source connected with M_{AIDNk} to reliably turn off S_{AIDk}, which also prevents the body diodes D_{Pk} and D_{Nk} from conducting. To generate the drive power supply V_{BSTk}, a bootstrap circuit is integrated by drawing refreshing current from V_{IN}.

IV. Experimental Results

A prototype chip of ART-PoL controller was fabricated in a 180nm BCD process, driving 40 GaN power devices. Fig. 7 shows the die photo with a chip area of 6mm×6mm including the I/O pads. The measurements in Fig. 8 show that the converter achieves 48V-to-1V 200A power delivery. Under such operating condition, as demonstrated by the measured thermal image of Fig.9, the converter works at a maximum temperature of 80.5°C without thermal issue. As measured in Fig. 10, when I_O rises from 10A to 110A within 500ns, the proposed LDO mode suppresses V_O droop by 48% from 210mV to 110mV and reduces recovery time by 45% from 55µs to 20µs, compared to the classical control.

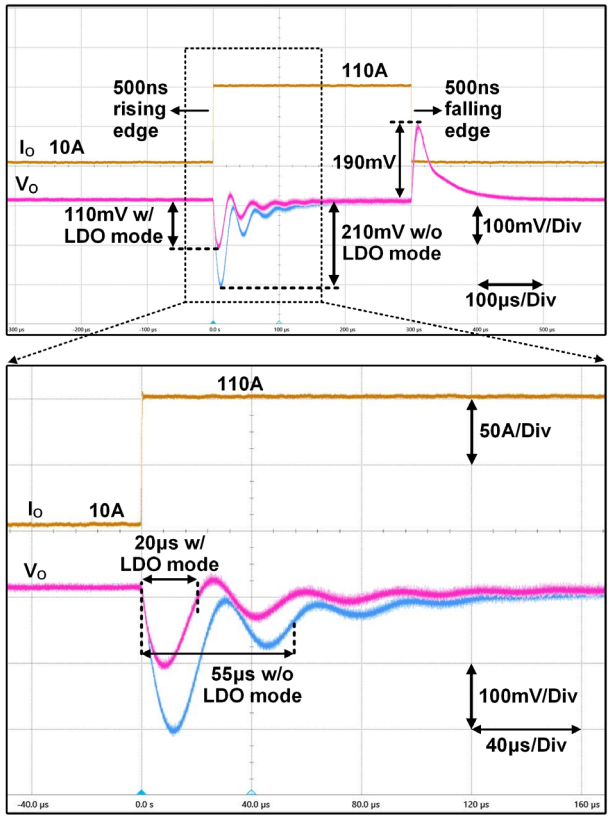

Fig. 10. Measured load transient responses with C_{load}=2.35mF for 10A-to-110A current step-up within 500ns and 110A-to-10A current step-down within 500ns.

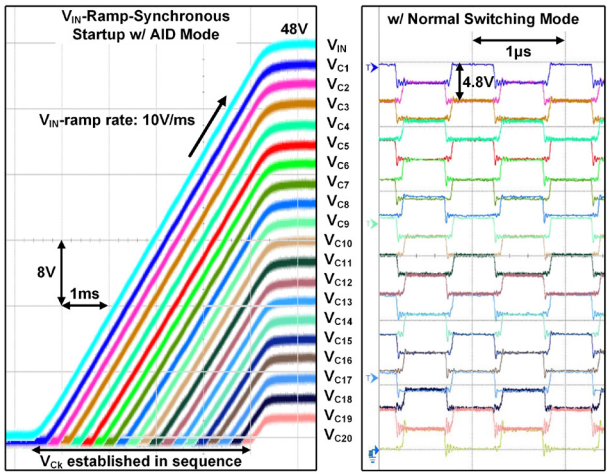

Fig. 11. Measured waveforms of the flying capacitors' top plates (V_{Ck}) under active-input-division (AID) mode and normal switching mode.

When V_{IN} ramps up at a rate of 10V/ms, the waveforms of V_{C1}~V_{C20} are measured in Fig. 11, indicating a sequential establishment of every V_{CFk} for reliable startup. Then, V_{C1}~V_{C19} switch at 1MHz with 2.4V swing range during normal switching mode. Based on the measurements of Fig. 12, the efficiencies of converting 48V to 1V at 1MHz peak at 87.4%, with ⩾80% efficiency over 85% of the full load range. As summarized in Table I, compared to the other chip-level solutions [2, 5-8], this work delivers the highest I_O. Compared to the PCB solutions [3, 4], it achieves the highest operating frequency. Overall, this work acquires the lowest Q_P and Q_S [1]. In comparison with [2], the proposed LDO mode shortens the recovery time by 2.5 times. Considering that the I_O step-up time is half that in [7], the

TABLE I. PERFORMANCE SUMMARY WITH PREVIOUS WORKS

Design		JSSC 2021 [2]	APEC 2023 [3]	TPEL 2024 [4]	JSSC 2021 [5]	VLSI 2022 [6]	VLSI 2024 [7]	JSSC 2024 [8]	This Work
Process		0.6μm BiCMOS	PCB solution	PCB solution	0.18μm BCD	0.18μm BCD	0.18μm BCD	0.18μm BCD	**0.18μm BCD**
Topology		6-phase buck	MSC-PoL	SBC	12-level SC	QSD	IP-TLVR	10-level SC	**ART-PoL**
Maximum V_{DS}		12V	30V	27V	8V	24V	6V	4.8V	**4.8V**
Input Voltage		12V	48V	48V	48V	48V	12V	24V	**48V**
Output Voltage		1V	1V	1V	1V	1V	1V	1V	**1V**
Maximum I_O		180A	220A	500A	8A	10A	100A	5A	**200A**
Switching Frequency		400kHz	704kHz	150kHz	2.5MHz	1MHz	1MHz	250kHz	**1MHz**
Inductor		6x250nH	8x140nH	16x606nH	-	4x1μH	2x150nH	2x10μH	**20x200nH**
Flying Capacitor		-	7x22μF	30x10μF 10x220μF	-	3x2.2μF	3x47μF	9x4.7μF	**19x22μF**
Output Capacitor		6000μF	-	108x47μF	4x47μF	20μF	2000μF	66μF	**2350μF**
V_{IN}-Ramp Sync. Startup		No	No	No	No	No	No	Yes(0.2V/ms)	**Yes(10V/ms)**
Q_PxQ_S*		-	28.1	15.3	-	34.3	43.3	21.4	**8.4**
Power Density		-	677W/in^3	464W/in^3	998W/in^{3}**	-	-	-	**626W/in^{3}****
Peak Efficiency		92.5%	91.2%	94.7%	90.2%	84.7%	93.6%	93.9%	**87.4%**
≥80% Efficiency Load Range		-	91%	98%	70%	60%	90%	99%	**85%**
I_O Step-Up Response	$\Delta I_O/\Delta t$	100A/-	-	-	5A/-	6.3A/50ns	90A/1μs	0.95A/0.5μs	**100A/0.5μs**
	V_O Undershoot	50mV	-	-	114.5mV	80mV	48mV***	120mV	**110mV**
	Recovery Time	50μs	-	-	-	1μs	15μs***	89μs	**20μs**

*The product of the normalized passive component volume (Q_P) and switch stress (Q_S) with β=500 [1]
**Considering the power stage volume ***Using trans-inductor

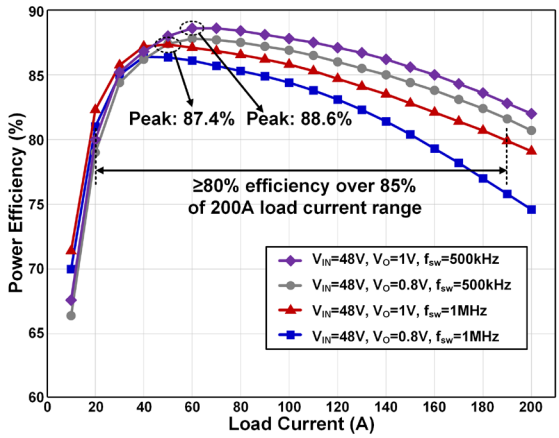

Fig. 12. Measured power efficiency plots.

ART-PoL, even without using trans-inductor, achieves a comparable if not better load response, while accomplishing a 4 times larger conversion ratio. Compared to [8], this design accomplishes a reliable V_{IN}-ramp-synchronous startup with 50 times faster V_{IN}-ramp rate.

V. CONCLUSION

This paper presents a 20-level GaN-based PoL converter, completing a direct 48V-to-1V conversion with 200A load current. With auto-reconfigurable tri-mode (ART) control, the proposed design can simultaneously energize all the inductors without adding any additional power devices, overcoming the limited I_O step-up response issue in MLSCB. Moreover, it features V_{IN}-ramp-synchronous startup with a maximum V_{IN} slope of 10V/ms for reliable hybrid switching.

ACKNOWLEDGMENT

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