A 20.8 nW, 41 fJ·K² Resolution-FoM SAR-based Temperature Sensor with Temperature Coefficient Amplifier

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***Abstract*—This paper presents a circuit technique that enables a selective amplification of the temperature coefficient of the sensing source, thereby mitigating the need for power-intensive readout schemes and simplifying the overall sensor architecture. Temperature coefficient amplifier introduces a negative proportional-to-absolute-temperature (PTAT) voltage, enabling an amplified gradient for both PTAT and complementary-to-absolute-temperature (CTAT) voltages within the usable temperature range, resulting in a reduced burden and precise temperature measurements with a low-complexity readout circuit. With a SAR-based conversion, implemented temperature sensor in 180nm CMOS achieves a figure-of-merit of 41fJ·K² with a 22.2mK resolution across −20°C to 100°C while consuming 20.8nW. It shows a 3σ inaccuracy of ±1.44°C after a single-point trimming procedure.**

***Keywords*—temperature sensor, temperature coefficient amplifier, ultra-low power, subthreshold, bandgap-Vth reference voltage**

I. Introduction

There has been extensive research on temperature sensors using CMOS process as it allows reliable sensing sources as well as high-precision integrated circuits for readout processing. The general approach for the temperature sensing is extracting a temperature-dependent variable with a linear characteristic of proportional-to-absolute-temperature (PTAT) voltage or current and complimentary-to-absolute-temperature (CTAT) voltage or current, and converts it to a digital value based on a temperature-independent reference obtained by the combination of the two. Reported PTAT and CTAT circuits with CMOS and parasitic BJTs show a good linearity [1,2]. However, the PTAT and the CTAT voltages hold small temperature coefficients (TC) of ±1~2mV/°C with their extrapolated voltages at 0K starting from 0V and 1.2V (bandgap), respectively [3]. Therefore, in a temperature range of interest (e.g. 250K ~ 370K), this small gradient consumes a large amount of voltage headroom at given supply voltage. Since this inevitable offset reaching a few hundreds of mV cannot be separated from the temperature dependence, it has not been possible to amplify the gradient only.

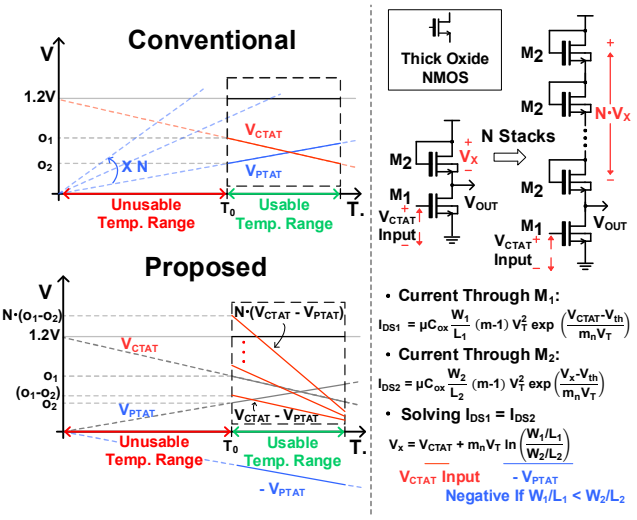

Fig. 1. Main Idea; Difficulty in multiplication of temperature coefficient (top left); Proposed multiplication of temperature coefficient (bottom left); Core circuit for temperature coefficient amplifier (right).

Therefore, to achieve a fine resolution of ~10mK from the small temperature coefficient, the readout circuits have been accompanied by costly techniques such as oversampling analog-to-digital converter (ADC) [1] with delta-sigma modulation (DSM) [2,4], dynamic element matching (DEM) [2,4], and low-noise design [1,2,4].

This work proposes a circuit technique that enables a selective amplification of the temperature coefficient of the sensing source while suppressing the offset, thereby achieving a fine-resolution conversion with a low-complexity readout circuit. It is achieved by introducing a negative PTAT voltage which enables an amplified temperature gradient for both PTAT and CTAT voltages within the temperature range of interest.

II. Proposed Temperature Sensor

A. Tempearture Coefficient Amplifier

The proposed idea is illustrated in Fig. 1. The V_{CTAT} and the V_{PTAT} for $T > T_0$ can be described as follows:

$$V_{CTAT}(T) = -\alpha\cdot(T-T_0) + o_1 \quad (1)$$

$$V_{PTAT}(T) = +\beta\cdot(T-T_0) + o_2 \quad (2)$$

where T_0 represents the lowest temperature in the temperature range of interest. The offsets, o_1 and o_2 will be few hundreds of mV in the temperature range of interest. Taking $V_{CTAT} - V_{PTAT}$ leads to

$$(V_{CTAT} - V_{PTAT})(T) = -(\alpha+\beta)\cdot(T-T_0) + (o_1-o_2). \quad (3)$$

The result reveals a suppressed offset of (o_1-o_2) with an increased temperature gradient of $-(\alpha+\beta)$. By simply stacking it N times in a branch, an amplified gradient of $-N\cdot(\alpha+\beta)$ can be achieved with an reduced offset of $N\cdot(o_1-o_2)$ that can be safely handled within the given supply rails (Fig. 1, bottom). The circuit for $V_{CTAT} - V_{PTAT}$ is formed with two transistors, where a NMOS diode load is stacked on a NMOS common-source amplifier, both operating in the subthreshold region. Applying a V_{CTAT} from the bandgap reference to the gate of the common-source amplifier leads to a sum of V_{CTAT} and V_{PTAT} at the voltage across the load. The gradient of V_{PTAT} becomes negative when W_2/L_2 exceeds W_1/L_1. Thus, desired amplification of the gradient can be achieved by simply stacking multiple diode stages. The threshold voltage term can be safely canceled out by using the same type transistors (thick gate oxide in this work) and body bias condition with different W/L ratios, resulting in enhanced immunity to process variations.

B. Proposed Architecture

Fig. 2 shows the overall circuit diagram of the proposed temperature sensor. The sensor consists of a 13-bit asynchronous split-CDAC SAR ADC, a bandgap reference [5], a temperature coefficient amplifier, and two low-dropout (LDO) regulators for the temperature coefficient amplifier and the ADC. The temperature coefficient amplifier receives the small gradient CTAT voltage from the bandgap reference and generates complimentary outputs with NMOS and PMOS amplification stages to provide a fully differential input to the ADC. The PMOS amplifier takes a node voltage from the NMOS amplifier for the CTAT input. The output voltage of the NMOS amplifier appears to be increasing as the amplified $(V_{CTAT} - V_{PTAT})$ is referenced to VDD. Conversely, the output of the PMOS amplifier generates a decreasing output because it is referenced to the ground. The LDO uses the CTAT voltage from the bandgap reference for the op-amp current bias, and the feedback voltage divider is formed by stacking diode-connected PMOS transistors to reduce the quiescent current. Each LDO generates VDD_{AMP} and $VREF_{ADC}$, the internal supplies for the temperature coefficient amplifier and the ADC making the circuits immune to supply variations. The $VREF_{ADC}$ is connected to an internal capacitor of 70pF in series with a 40Ω resistor to suppress ripples and inductive ringing.

The fully differential output of the temperature coefficient amplifier is then sampled by two split-capacitor DACs with each consisting of a 7-bit DAC and a 6-bit DAC for MSBs and LSBs, respectively. The unit capacitance of the CDAC is 20.28fF which is the minimum metal-insulator-metal (MIM) capacitance in the given 180nm technology. All transistors in the ADC are designed with thick gate oxide to minimize leakage current.

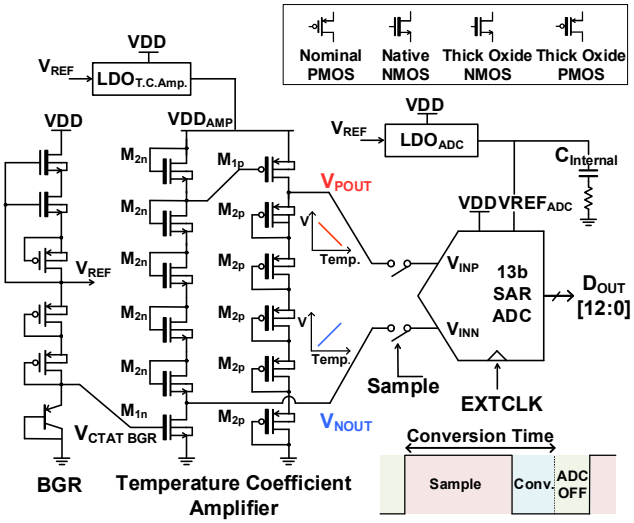

Fig. 2. Circuit diagram of the proposed temperature sensor.

III. Measurement Results

With all the required circuits included on chip, the temperature sensor was fabricated using a 180-nm CMOS process. Fig. 3 shows measured untrimmed raw output voltages of the temperature coefficient amplifier and CTAT voltages of BGR and raw ADC output codes measured over the temperature range of -20°C to 100°C from 24 samples, showing good immunity to chip-to-chip variation. While the average gradient of the BGR CTAT voltage is -0.79mV/°C, the average gradients of the V_{NOUT} and V_{POUT} are amplified to 10.3mV/°C and -9.4mV/°C, respectively.

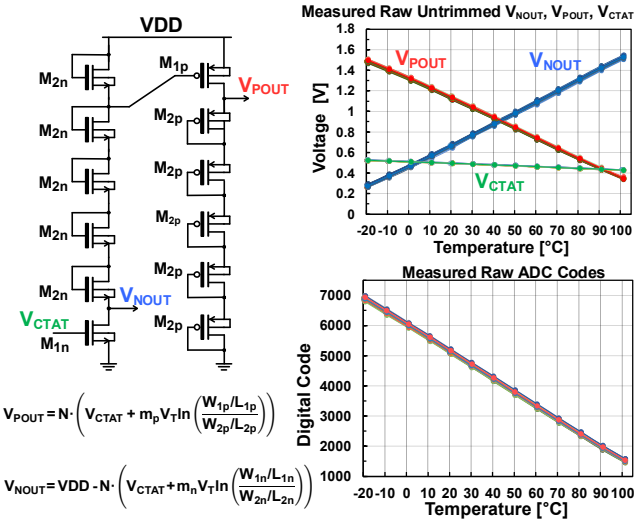

Fig. 3. Tested circuit of TC amplifier (left); Raw untrimmed output voltages measured from 24 chips (top right); Measured raw ADC output codes (bottom right).

This amplification of temperature gradient corresponds to a more than ten times increase, which is a significant improvement over conventional BJT-based CTAT voltages. Therefore, the single output covers a range of 0.25V-to-1.55V

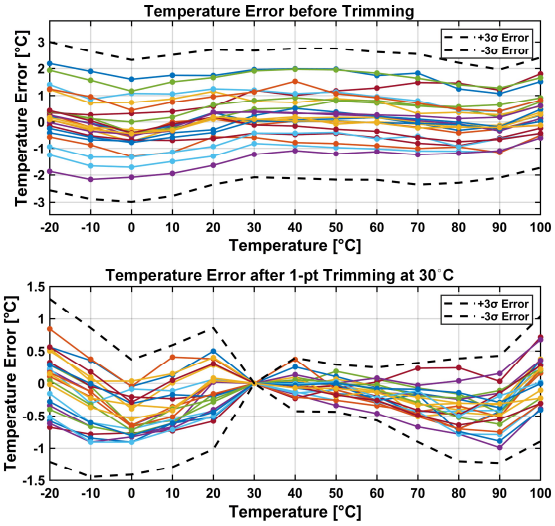

Fig. 4. Temperature error measured from 24 chips before trimming (top); Temperature error after one-point trimming at 30 °C (bottom).

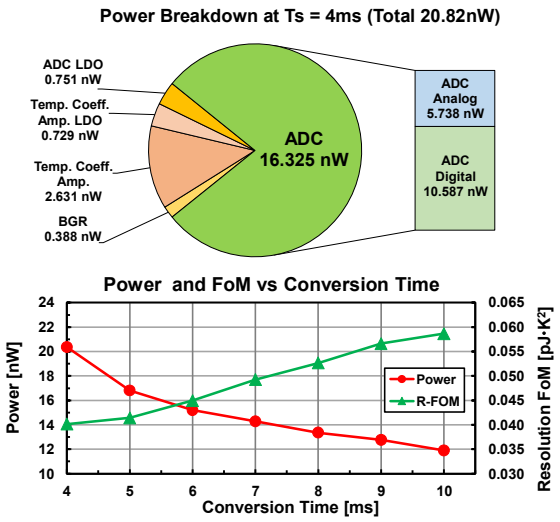

Fig. 5. Power breakdown at 4ms conversion time (top); Power and figure-of-merit as the conversion time varies (bottom).

when the temperature varies from -20°C to 100°C. It corresponds to about 70% of the full-scale ADC conversion window, making it easier to obtain a fine resolution using an energy-efficient low-cost SAR ADC.

Fig. 4 shows the measured temperature errors with 24 samples. A Pt-100 was used for the reference temperature during the measurements. Untrimmed codes obtained from 24 samples show a 3σ inaccuracy of about ±3°C. A 1 point offset trimming at 30°C without any off-chip processing or backend *n*th order polynomial fitting results in a 3σ inaccuracy of <±1.44°C over the measured temperature range. Fig. 5 (top) shows the power breakdown of the chip with a total of 20.8nW at room temperature, where ADC consumes 16.3nW at a sampling period of 4ms. Fig. 5 (bottom) shows average power consumption and resolution FoM as conversion time varies from

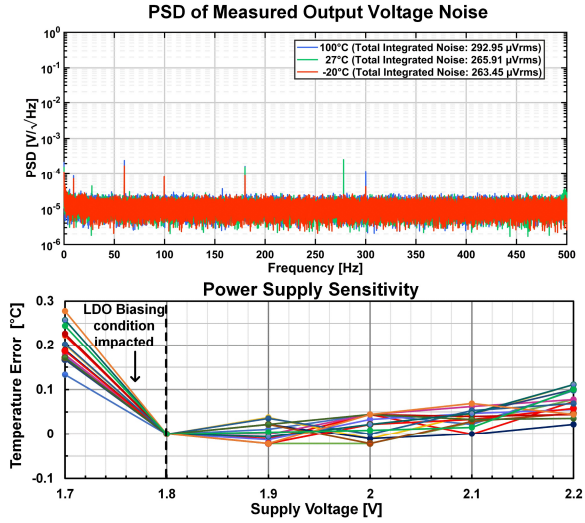

Fig. 6. PSD of output voltage noise obtained from 2^{16} ADC outputs at different temperatures (top); Supply sensitivity of 16 samples (bottom).

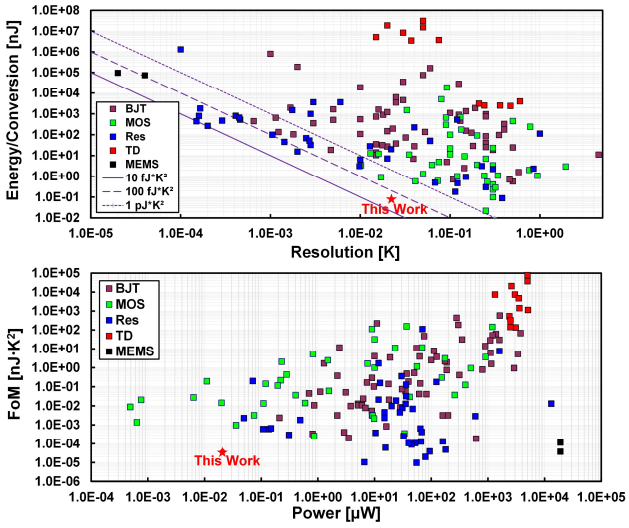

Fig. 7. Energy/conversion vs. resolution (top); FoM vs. power consumption (bottom).

4ms to 10ms. Fig. 6 (top) shows power spectral density (PSD) plot of the noise voltage, which was obtained by calculation from measured ADC codes with a sampling period of 4ms at -20°C, 27°C and 100°C. Total integrated noise shows 263.45μV_{rms}, 265.91μV_{rms} and 292.95μV_{rms} at -20°C, 27°C and 100°C respectively. The average supply sensitivity from 1.8V to 2.2V measured with 16 samples was 0.27°C/V (Fig. 6, bottom).

Fig. 7 visualizes the position of this work in a plot of energy per conversion versus resolution, for published temperature sensors, categorized by type, from 1989 to 2024 [6]. With 83pJ/conversion and 22.2mK resolution, the sensor achieves the best number of 41fJ·K² in the resolution FoM among MOS-based sensors. Fig. 7 (bottom) shows the FoM versus power consumption, highlighting that achieving the same level of FoM is even more difficult as the power consumption goes down to sub-μW range, where DC power consumption by leakage and bias current becomes more significant.

Table I. Performance Summary with comparison to previous works

	This Work	JSSC'24 [1]	ISSCC'24 [2]	ISSCC'23 [7]	VLSI'22 [8]	VLSI'22 [4]	ESSCIRC'22 [9]	ISSCC'18 [10]
Sensor Type	Hybrid +TC Amp.	NPN	NPN	WhB	Hybrid	NPN	WhB	Hybrid
Architecture	SAR	NS-SAR	CT ΣΔ	SAR	SAR	DT ΣΔ	SAR	SAR
Technology [nm]	180	180	180	65	4	180	65	22
Area [mm^2]	0.34	0.057**	0.07**	0.0023	0.0061	0.058**	0.0018	0.0043
Supply voltage [V]	1.8 to 2.2	1.8	1.4 to 2.2	1/0.6	1	1.2 to 1.8	1/0.6	1
Supply sensitivity [°C/V]	0.27	N/A	0.04	N/A	N/A	0.07	N/A	1.76
Temperature range [°C]	-20 to 100	-50 to 110	-55 to 125	-20 to 120	-10 to 100	-15 to 85	-20 to 120	-30 to 120
Inaccuracy [K] (Trimming Points)	±1.44 (1[a])	±1.57 (1[a])	±0.1 (1[a])	0.7/-0.6 (2[b])	±1.79 (2[a])	±0.15 (1[a])	-0.3/0.4 (2[b])	±1.07 (1[a])
Resolution [mK]	22.2	92	1.22	470	460	15	470	580
Power [µW]	0.0208	61.2	3.5	0.149	64	0.21	0.137	50
Conversion time [s]	4m	0.08m	38.4m	0.02m	0.011m	50m	0.02m	0.032m
FoM* [pJ·K²]	0.041	41.4**	0.200**	0.66	150	2.36**	0.60	540
# of samples	24	25	40	15	30	20	20	38

*** FoM = (Energy/Conversion) × (Resolution)^2 a: 3σ Inaccuracy b: Maximum worst case inaccuracy**

**** Excluding the off-chip decimation filter or digital back-end such as nonlinearity correction circuits.**

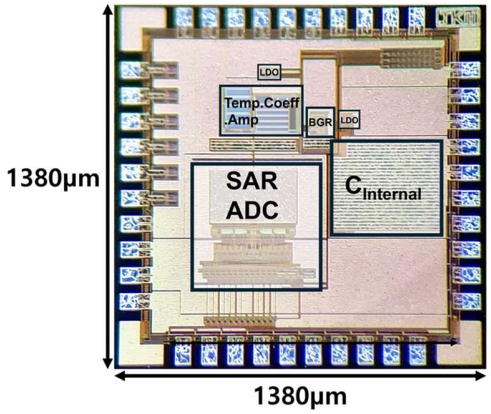

Fig. 8. Die photo.

Table I compares the performance with the state-of-the-art temperature sensors. Fig. 8 shows a die photo.

IV. Conclusion

This work presents an ultra-low power temperature sensor with a novel temperature coefficient amplification scheme. The temperature coefficient amplifier, employing sub-threshold current operation to generate a negative PTAT voltage, selectively amplifies both PTAT and CTAT gradients within the usable temperature range while suppressing the offset. The resulting SAR-based temperature sensor achieves a FoM of 41fJ·K² with a 22.2mK resolution over −20°C to 100°C, a 3σ inaccuracy of ±1.44°C after single-point trimming, and a power consumption of only 20.8nW. This performance represents the best FoM among MOS-type temperature sensors.

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