A 144 mW 76 Gb/s DAC-Based Discrete Multitone Wireline Transmitter in 5nm FinFET

Seoyoung Jang[1*], Jaewon Lee[2*], Marcel Kossel[2], Matthias Brändli[2], Thomas Morf[2], Pier-Andrea Francese[2], Gain Kim[1]
[1]Department of Electrical Engineering and Computer Science, DGIST, Daegu, South Korea
[2]Hybrid Cloud Research, IBM Research Europe, Rüschlikon, Switzerland
Email : jang119jsy@dgist.ac.kr, jaewon.lee3@ibm.com, gain.kim@dgist.ac.kr
*Equally Credited Authors (ECAs)

***Abstract*—This paper presents a 76 Gb/s digital-to-analog converter (DAC)-based discrete multitone (DMT) wireline transmitter (TX) fabricated in 5nm FinFET. Bit and power loading with 32/64/128-QAM across 31 orthogonal subchannels is demonstrated over a channel with 9.7 dB insertion loss (IL), achieving a bit error rate (BER) of 2.1 E-4. The prototype consumes 144 mW from 0.675 V digital and 0.725 V analog supplies, resulting in an energy efficiency of 1.89 pJ/b. An on-chip DSP performs subchannel-wise bit/power allocation and spectral shaping using a 64-tap inverse fast Fourier transform (IFFT) and cyclic prefix (CP) insertion. Compared to conventional PAM-based TXs, the proposed architecture provides improved bandwidth efficiency and signal-to-noise ratio (SNR) through frequency-domain modulation and equalization. This work is the first demonstration of a DAC-based DMT TX at 76 Gb/s data rate fabricated in advanced CMOS technology.**

***Index Terms*—Serial link, DAC-based transmitter, discrete multitone, DMT, bit and power loading, IFFT**

I. Introduction

Digital-to-analog converter (DAC)-based wireline transmitters (TXs) incorporating a digital signal processor (DSP) [1-9] have demonstrated strong pre-equalization capability. Such a DAC-based TX architecture can provide high flexibility to support various modulation schemes both in the time and frequency domains, such as 4-level pulse amplitude modulation (PAM-4) and discrete multitone (DMT) modulation.

Conventional PAM-based TX DSP employs feed-forward equalization (FFE) to partially compensate for the intersymbol interference (ISI) while the driver's output swing is restricted from peak-power constraints. In DMT communication, a cyclic prefix (CP), which is a replica of the end of the DMT symbol, is inserted at the beginning of the symbol to mitigate inter-symbol interference (ISI) [10]. This technique preserves the orthogonality of subchannels and improves the effective signal-to-noise ratio (SNR). Moreover, both the number of bits and the symbol power can be independently assigned to each frequency-domain subchannel, enabling signal spectrum shaping that adapts to the channel profile [11], [12].

Such a loading technique allows the system to reach near Shannon capacity for a given channel. Recently, [5] demonstrated the effectiveness of DMT over PAM; however, the DMT frame in [5] is generated by the software and stored in on-chip SRAM to be transmitted by DAC repeatedly. A

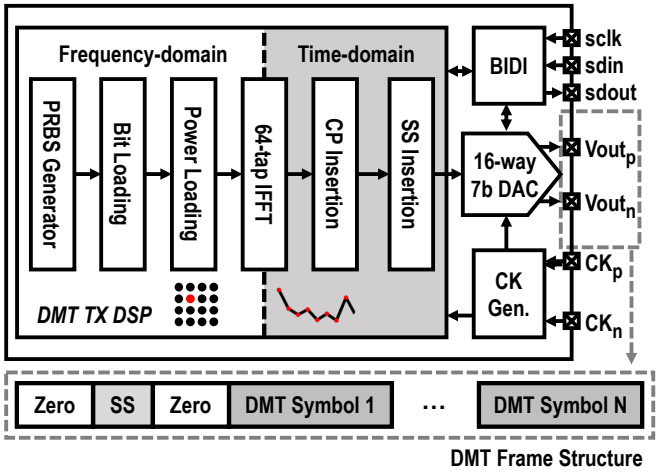

Fig. 1: Overall block diagram of the implemented DMT TX prototype and DMT frame structure.

56 Gb/s and 112 Gb/s DMT receiver (RX) prototype were demonstrated in [13] and [14] respectively; however, a complete DMT TX, including an integrated datapath DSP, is not yet shown in literature and is to be demonstrated for high-speed serial links. This paper presents a 76 Gb/s DAC-based DMT wireline TX fabricated in 5nm FinFET technology. An on-chip DSP performs bit and power loading across 31 orthogonal subchannels operating at 1.75 GHz to compensate for channel impairments. The prototype demonstrates 32/64/128-quadrature amplitude modulation (QAM) transmission with a bit error rate (BER) of 2.1E-4 over a channel exhibiting 9.9 dB insertion loss (IL) at 14 GHz. The TX prototype chip consumes 144 mW from 0.675 V digital and 0.725 V analog supplies, achieving an overall energy efficiency of 1.89 pJ/b, comprising 1.4 pJ/b for the DSP and 0.5 pJ/b for the DAC.

II. DMT TX Datapath

Fig. 1 shows the overall block diagram of the implemented DMT TX prototype. The test chip receives a differential half-rate clock (CK_{p}, CK_{n}) from where a 1/16-rate clock (C16) for DSP is generated. The bidirectional serial interface (BIDI) configures and reads back the DSP and DAC parameters.

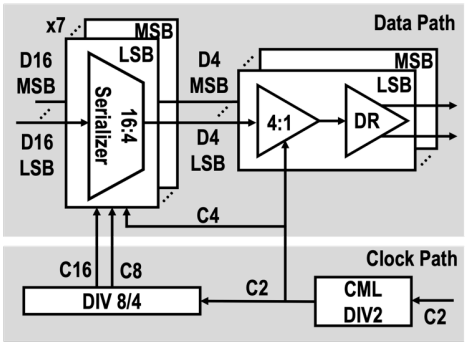

Fig. 2: Block diagram of implemented 28 GBaud 7-bit DAC.

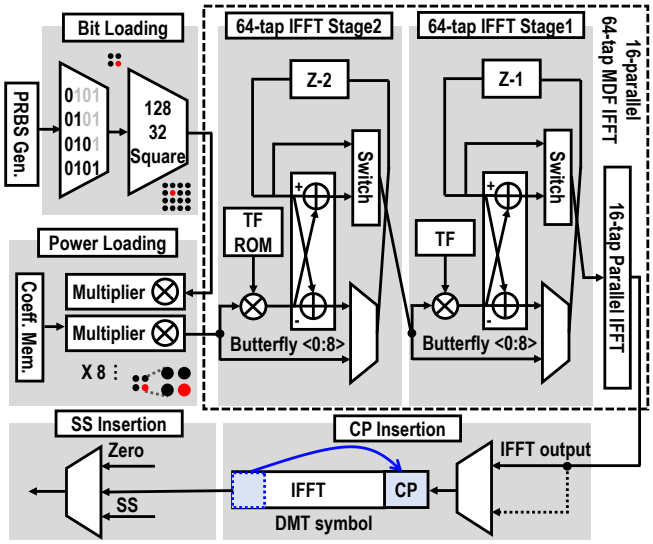

Fig. 3: DSP subblocks for bit/power loading, 16-parallel 64-tap MDF IFFT, and CP/SS insertion.

The bit loader maps the binary sequence from pseudo-random binary sequence (PRBS) generators into the QAM symbols. The power loader scales each subchannel power to meet the channel profile as

$$b_i = \log_2(1 + \frac{P_i \cdot SNR_i}{\Gamma_i}) \quad (1)$$

, where b_i is the average bit, P_i is the power loading, and Γ_i is the SNR gap for the i-th subchannel. The 64-tap inverse fast Fourier transform (IFFT) converts frequency-domain QAM symbols into time-domain waveforms. An 8-tap CP and a 64-tap synchronization sequence (SS) are inserted prior to data transmission through a 7-bit DAC, which employs 16:1 serialization and source-series terminated (SST) output stages integrated into the DAC weight network, as shown in Fig. 2. The resulting DMT frame consists of multiple DMT symbols, zeros, and SS [15].

Fig. 3 illustrates the DSP subblocks in the DMT TX datapath. The bit loader supports QAM constellations from QAM-4 to QAM-256 by forcing selected MSBs of the parallel PRBS output to zero for lower-order QAM and utilizing more bits for higher-order QAM. Cross QAM formats such as QAM-32 and QAM-128 are implemented with dedicated logic. Two-dimensional Gray coding is applied to minimize the BER for a given symbol error rate (SER). The power loader consists of eight parallel real multipliers that adjust the amplitude of each subchannel's constellation according to its assigned power level. Unlike the RX-side frequency-domain equalization (FDE), constellation rotation is omitted in the TX since it does not improve the SNR. Bit and power loading configurations are computed off-chip based on the measured channel SNR for each subchannel.

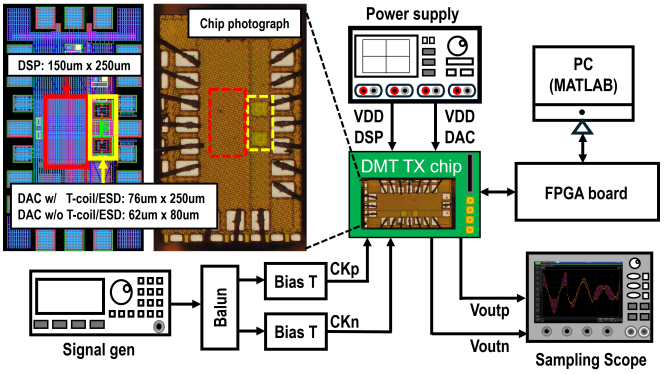

Fig. 4: Measurement setup of the implemented 76 Gb/s 7-bit DAC-based DMT TX prototype.

The two-stage 16-parallel 64-tap multi-path delay-feedback (MDF) IFFT processor is implemented to reduce multiplier count while increasing the number of subchannels [16], [17]. A 64-tap IFFT is computed by reusing a 16-tap parallel IFFT core four times. Twiddle factors (TFs) are stored in read-only memory (ROM); non-trivial complex multiplications are performed in the second pipeline stage, while the remaining TF multiplications use constant coefficients to minimize area and power consumption. Each complex multiplier is implemented using four real adders and three real multipliers. The IFFT engine adopts a real-valued decimation-in-time (DIT) architecture and exploits the complex conjugate symmetry, requiring only half of the butterfly structure compared to a complex-valued IFFT. After frequency-domain QAM symbols are converted to the time domain, an 8-tap CP is inserted. The CP length is chosen to balance the effective data rate and residual ISI performance at the receiver. A finite-state machine (FSM) controls the DSP output, selecting between zeros, SS, and CP-appended DMT symbols. The number of zeros and DMT symbols per frame is programmable. Clipping is applied at the end of DSP chain to prevent undesirable artifacts, such as overflow.

III. MEASUREMENT RESULTS

The DMT TX prototype is fabricated in 5nm FinFET CMOS and wire-bonded on a PCB for characterization. The DSP and TX core occupy $150\times250\,\mu m^2$ and $76\times250\,\mu m^2$, respectively, including the T-coil and ESD protection. The synthesized DSP has a cell density of 53.8%. The measurement setup is illustrated in Fig. 4. A 14 GHz clock is generated using

TABLE I: Comparison to the Prior art

	This work	[1]	[2]	[5]	[6]
Technology	5nm	7nm	7nm	4nm	22nm
Modulation	DMT	NRZ / PAM-4	PAM-4	PAM-4/8/DMT	Multicarrier
Supply voltage	0.735 / 0.725	0.9/0.96	1.8	0.95	0.85 / 1.5
Digital equalization	Bit / Power loading	8 -tap FFE	Pre - Emph.	SRAM	8 - tap FIR
Driver topology	SST / 7b DAC	SST / 8b DAC	CML / 8b DAC	SST / 8b DAC	CML / 7b DAC
Baud rate (GBd)	28	56	66	72	5*
Output swing (Vppd)	0.725	0.96	1.1	0.92	1.2
Active area (mm^2)	0.0565	0.032	0.5875**	0.047	0.133
IL (dB)	9.9	6	13	8.8	21.5
Data rate (Gb/s) (after CP removal)	60.3 - 84.4	112 (PAM-4)	132	212 (DMT)	50
BW efficiency (b/Hz)	5.4 @76.2Gb/s	4	4	5.9 (DMT)	4*
BER	2.1E-4 @76.2Gb/s	N/A	N/A	4.2E-4	$<$ 1E-4
Energy efficiency	1.89 @76.2Gb/s (DSP incl.)	1.4 (DSP incl.)	1.94***(N/A)	1.36 (DSP excl.)	1.68 (DSP incl.)

*Use three DACs for multicarrier transmission, **Single lane + amortized PLL, *** Estimated from DAC FoM, SNDR, and 3dB BW not including PLL power.

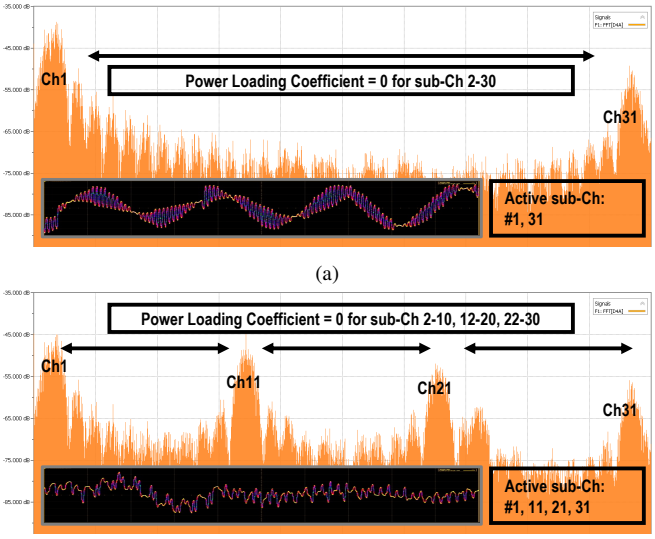

Fig. 5: Exemplary output spectrum of DMT TX and the corresponding time-domain waveform when subchannels 1 and 31 are enabled (a), and subchannels 1, 11, 21, and 31 are enabled (b).

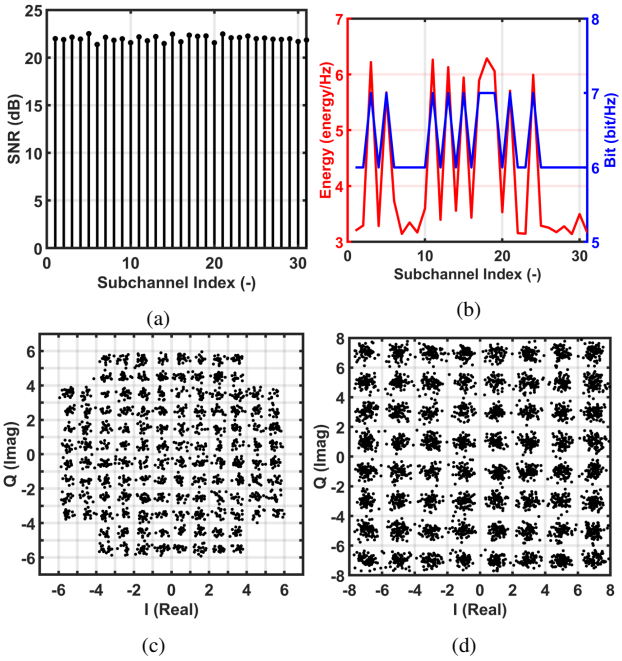

Fig. 6: Channel SNR (a), bit and power loading profile (b), reconstructed constellations with QAM-128 (c), and QAM-64 (d) at 76 Gb/s data rate.

an E8257D signal generator and converted to a differential signal with a 0.6 V common-mode voltage using a balun and bias-T pair. The on-chip clock path includes a quadrature error correction (QEC) circuit to ensure a 50% duty cycle and reduce nonlinearity. Configuration of the DSP and DAC is managed by an FPGA board. The time-domain DMT waveform is transmitted through a 1-meter RF cable and oversampled 32 times using a Keysight N1000A sampling oscilloscope. Post-processing, including channel SNR extraction and constellation reconstruction, is performed offline on a PC.

Fig. 5 shows the exemplary output spectrum of DMT TX and the corresponding time-domain DMT waveform for visualization purposes. To emphasize the impact of subchannel allocation on time-domain signal shape, zero power loading coefficients are applied to unused subchannels. In Fig. 5(a), data is transmitted on the 1^{st} and 31^{st} subchannels, while in Fig. 5(b), the 1^{st}, 11^{th}, 21^{st}, and 31^{st} subchannels are enabled. The captured waveforms are post-processed off-chip to reconstruct constellation diagrams and compute the BER. Each unit interval (UI) contains 32 samples, which are downsampled by a factor of 32 using a brick-wall decimation filter to suppress aliasing near the Nyquist frequency. The optimal sampling phase is determined by sweeping the downsampling start index and selecting the one yielding the highest SNR. The CP location is identified by detecting the peak of the cross-correlation between the received waveform and the Zadoff–Chu sequence [15]. SNR is calculated from the error vector magnitude (EVM) of the equalized QAM-4 pilots, with an average of 22.0 dB as shown in Fig. 6. Based on the measured SNR per subchannel, a margin-adaptive Levin–Campello (LC) algorithm [18] determines the bit and power loading profile, targeting an SER of 5E-4 per dimension. The TX achieves a peak-to-average power ratio (PAPR) of

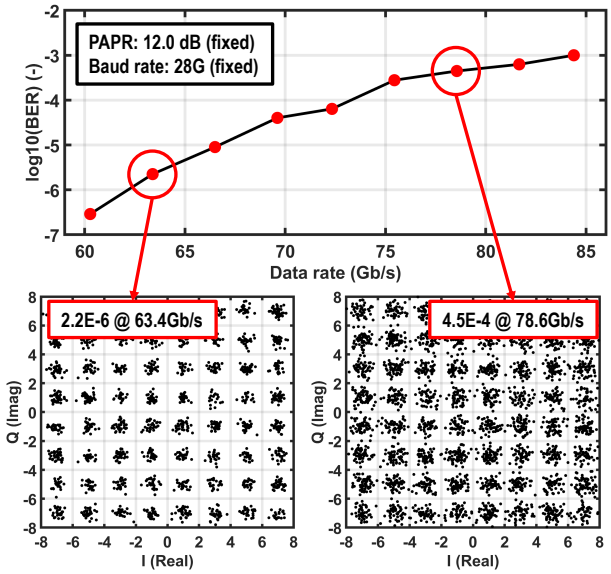

Fig. 7: Data rate versus BER curve at 28 Gbaud with 12.0 dB PAPR (top), and reconstructed QAM-64 constellations at low BER with low data rate (bottom-left), and high BER with high data rate (bottom-right).

12.0 dB and a bandwidth efficiency of 5.4 b/Hz, corresponding to an effective data rate of 76.2 Gb/s at 28 Gbaud including the 8-tap CP overhead. The measured BER is 2.1E-4, and the reconstructed constellation diagrams show EVMs of -25.4 dB and -23.3 dB for QAM-128 and QAM-64, respectively.

Fig. 7 shows the measured BER versus data rate curve at a 28 Gbaud DAC rate, along with the reconstructed QAM-64 constellations. A rate-adaptive LC algorithm allocates more power to lower-order QAM subchannels to minimize BER, trading off data rate while maintaining a constant PAPR of 12.0 dB. Unlike PAM, the data rate in DMT systems can be dynamically adjusted by reconfiguring the bit/power loading profile without changing the Baud rate under a given SNR condition. A data rate of $>$84 Gb/s is achieved at BER of 1E-3, while a BER could get as low as 2.9E-7 at a data rate of 60.3 Gb/s. At 0.735 V digital and 0.725 V analog supply, the DSP and DAC consume 105.8 mW and 37.7 mW, respectively, resulting in a total energy efficiency of 1.89 pJ/b.

Table I summarizes the key features and performance metrics of the proposed DMT TX test chip and compares them with prior state-of-the-art designs. To the best of authors' knowledge, this is the first reported DAC-based DMT TX implemented in 5nm FinFET technology. Compared to PAM-4 TX, the prototype achieves 1.4$\times$ higher bandwidth efficiency by assigning high-order QAM (64/128) to each subchannel. While [5] demonstrates the feasibility of high-speed DMT transmission using software-generated frames, this work implements a complete DMT TX chip integrating an on-chip DSP and DAC.

IV. CONCLUSION

This paper presents a 76 Gb/s DAC-based DMT wireline TX implemented in 5nm FinFET CMOS, featuring an on-chip DSP that performs bit and power loading across 31 orthogonal subchannels. The prototype integrates a 16-parallel 64-tap MDF IFFT engine, CP and SS insertion, and a 7-bit DAC with SST output drivers. The complete DSP-DAC datapath demonstrates energy-efficiency of 1.89 pJ/b and achieves 5.4 b/Hz bandwidth efficiency over a channel with 9.9 dB IL. This is the first reported DMT TX implementation with fully integrated DSP and DAC in advanced FinFET CMOS technology, demonstrating the feasibility of DMT modulation for high-speed wireline links.

ACKNOWLEDGMENT

This work was supported in part by MOTIE (RS-2024-00410244), the National Research Foundation of Korea (NRF) funded by MSIT (RS-2024-00352784, RS-2024-00409692), the DGIST R&D Program of the Ministry of Science and ICT under Grant (24-KUJoint-09), and the Samsung Future Technology Incubating Program (SRFC-IT2301-01).

REFERENCES

[1] M. Kossel *et al.*, "An 8b DAC-based SST TX using metal gate resistors with 1.4pJ/b efficiency at 112Gb/s PAM-4 and 8-tap FFE in 7nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 130-132, 2021.
[2] R. L. Nguyen *et al.*, "A highly reconfigurable 40-97GS/s DAC and ADC with 40GHz AFE bandwidth and sub-35fJ/conv-step for 400Gb/s coherent optical applications in 7nm FinFET," *ISSCC Dig. Tech. Papers*, pp. 136–138, 2021.
[3] J. Kim *et al.*, "A 224-Gb/s DAC-based PAM-4 quarter-rate transmitter with 8-tap FFE in 10-nm FinFET," *IEEE JSSC*, vol. 57, no. 1, pp. 6–20, Jan. 2022.
[4] H. Park *et al.*, "A 4.63 pJ/b 112Gb/s DSP-based PAM-4 transceiver for a large-scale switch in 5nm FinFET," *ISSCC Dig. Tech. Papers*, pp. 5–7, 2023.
[5] T. O. Dickson *et al.*, "A 72-GS/s, 8-bit DAC-based wireline transmitter in 4-nm FinFET CMOS for 200+ Gb/s serial links," *IEEE JSSC*, vol. 58, no. 4, pp. 1074–1086, April 2023.
[6] I. -M. Yi *et al.*, "A 50-Gb/s multicarrier transmitter using DAC-based polar drivers in 22-nm FinFET," *IEEE JSSC*, vol. 59, no. 9, pp. 2948–2959, Sept. 2024.
[7] M. Cusmai *et al.*, "A 224Gb/s sub pJ/b PAM-4 and PAM-6 DAC-based transmitter in 3nm FinFET," *ISSCC Dig. Tech. Papers*, pp. 126–128, 2024.
[8] D. Pfaff *et al.*, "A 224Gb/s 3pJ/b 40dB insertion loss transceiver in 3nm FinFET CMOS," *ISSCC Dig. Tech. Papers*, pp. 128–130, 2024.
[9] S. Jang *et al.*, "Recent advances in ultrahigh-speed wireline receivers with ADC-DSP-based equalizers," *IEEE OJSSCS*, vol. 4, pp. 290–304, Nov. 2024.
[10] J. Armstrong, "OFDM for optical communications," *IEEE JLT*, vol. 27, no. 3, pp. 189–204, Feb. 2009.
[11] B. Vatankhahghadim *et al.*, "A study of discrete multitone modulation for wireline links beyond 100 Gb/s," *IEEE OJCAS*, vol. 2, pp. 78–90, 2021.
[12] Z. Jiang *et al.*, "High speed DMT for 224 Gb/s and faster wireline transmission," *IEEE TCAS-I*, vol. 70, no. 4, pp. 1758–1771, April 2023.
[13] G. Kim *et al.*, "A 161-mW 56-Gb/s ADC-based discrete multitone wireline receiver data-path in 14-nm FinFET," *IEEE JSSC*, vol. 55, no. 1, pp. 38–48, Jan. 2020.
[14] J. Lee *et al.*, "A 353mW 112Gb/s discrete multitone wireline receiver datapath with time-based ADC in 5nm FinFET," *ISSCC Dig. Tech. Papers*, pp. 144–146, 2025.
[15] D. Chu, "Polyphase codes with good periodic correlation properties," *IEEE TIT*, vol. 18, no. 4, pp. 531–532, July 1972.
[16] G. Kim, "Design space exploration of single-lane OFDM-based serial links for high-speed wireline communications," *IEEE OJCAS*, vol. 3, pp. 134–146, 2022.
[17] J. Lee *et al.*, "A 2-lane discrete multitone wireline receiver datapath with far-end crosstalk cancellation on RFSoC platform," *IEEE TCAS-II*, vol. 71, no. 11, pp. 4738–4742, Nov. 2024.
[18] J. Campello, "Optimal discrete bit loading for multicarrier modulation systems," *IEEE ISIT*, pp. 193–193, 1998.