A 7b 30GS/s 0.032mm^2 CI-SAR TIADC in 28-nm CMOS with Fractional-delay FIR Filter based Full-Digital Background Timing Skew Calibration

Jongho Kim
Advanced DRAM Technology Team
Hwaseong-si, Gyeonggi-do, Korea
Samsung Electronics
jason.w.kim@samsung.com

Gyuchan Cho
Advanced DRAM Technology Team
Hwaseong-si, Gyeonggi-do, Korea
Samsung Electronics
gchani.cho@samsung.com

Hwankyu Song
Controller Development Team
Hwaseong-si, Gyeonggi-do, Korea
Samsung Electronics
hkyu.song@samsung.com

Hyeonsik Kim
Controller Development Team
Hwaseong-si, Gyeonggi-do, Korea
Samsung Electronics
gray.kim@samsung.com

Jintae Kim
Electrical and Electronics Eng. Dept.
Seoul, Korea
Konkuk University
jintkim@konkuk.ac.kr

***Abstract*— This paper presents a 30GS/s 7-bit 32x time-interleaved (TI) SAR ADC achieving the record-breaking area efficiency. The ADC utilizes segmented charge-injection cells and occupies only 294µm^2 per slice. A fractional-delay FIR filter based full-digital timing skew calibration scheme overcomes the drawbacks of correlation-based timing-skew calibration. Fabricated in 28nm CMOS, the prototype 30GS/s ADC achieves a peak SNDR of 31.43dB for 14.9GHz input with FoM$_W$ = 86.5fJ/conv.-step and performs reliably at 28GS/s over the temperature range from -30°C to 80°C.**

Keywords*— *Time-Interleaved ADC, Background Timing-Skew Calibration

I. INTRODUCTION

With the increasing adoption of multi-level wireline links, a compact and low-power time-interleaved analog-to-digital-converter (TIADC) is becoming a necessity in modern high-speed interfaces [1], [2]. This work focuses on tackling several challenges in such TIADC designs. First, area reduction is a key issue for highly interleaved TIADCs. While designing TIADCs in a scaled CMOS process is a straightforward path to improving area efficiency [2], a new slice ADC structure for the highest possible sampling speed per area is still needed. Also, background timing-skew calibration is mandatory for these TIADCs. The two-channel correlation-based timing-skew calibration [3], [4] is widely used, but this technique is not easily scalable to a higher number of interleaved channels, often requiring extra analog hardware to support many channels [5], [6], [7] or input signal that is not harmonically related to the sampling frequency.

In this paper, we report a 30GS/s 7-bit TIADC that utilizes segmented charge-injection cells (CICs) to minimize the slice ADC area, leading to an extremely compact 30GS/s 7-bit ADC. The full-scale and linearity of the slice ADC are maintained by embedded mixed-signal background feedback loops that are shared across all ADCs for maximum area efficiency. A new digital background timing skew calibration based on a fractional-delay FIR filter is presented to overcome the limitations of the existing correlation-based skew calibration. Our method, without requiring extra analog hardware, allows the timing skew calibration for any number of TI channels and a subharmonic input frequency tone.

II. CHARGE INJECTION SAR BASED TIADC

A. TIADC Architecture

Shown in Fig. 1, the 32x interleaved ADC uses a two-rank topology where the 1st rank comprises four non-bootstrapped NMOS sampling switches. The 1st rank sampling capacitors (=17fF) are followed by four source-follower (SF) based buffers, each driving eight slice ADCs. The SF buffer output common-mode is regulated by a separate common-mode feedback loop to accurately define the signal common-mode in 2nd rank sampler, which is a PMOS sampling switch, because the common-mode critically impacts the signal bandwidth and ADC operating speed. A 7.5GHz on-chip delay-locked-loop (DLL) generates quadrature phase clocks that are distributed to four local clock generators that are dedicated to each eight-ADCs quad, respectively. A 6-bit digital-to-time converter (DTC) with a time resolution of ~100 fs is used per each 1st rank sampler to provide a tuning knob for the timing skew calibration.

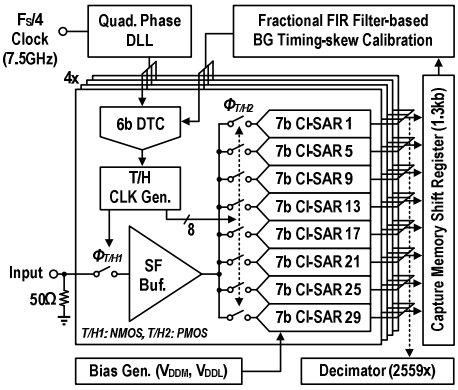

Fig. 1. Block diagram of the 32-way CI-SAR TIADC.

B. Slice ADC Architecture

Recent studies in charge-injection (CI) SAR ADC have significantly reduced the form factor by downscaling the input sampling capacitance with a customized layout [8] or hybridizing the capacitive DAC (CDAC) and CI-DAC [9]. However, the exponential tradeoff between the number of unit CI cells (CICs) and the resolution [8] or excessively large input swing (1.4V$_{ppd}$) as well as the full-scale

matching issue between the two heterogeneous DAC topologies (CDAC and CI-DAC) [9] limits its practical usage as a slice ADC of the TIADC for a wireline receiver where the input range tends to be upper-bounded by around 400~500mV$_{ppd}$ [1]. Table I compares the slice ADC of this work with recent studies on CI-SAR ADCs.

TABLE I. COMPARISON OF THE CHARGE INJECTION SAR ADCS

	This Work	*[8]*	*[9]*
Process (nm)	28	28	28
Resolution (b)	7	6	8
Slice F_S (GS/s)	0.937	1.1	1
Input Range (mV$_{ppd}$)	500	400	**1400**
# of Unit CICs	8	**16**	4
# of Unit Metal Cap.	2	2	22
Temp. Robust?	Yes	Yes	No

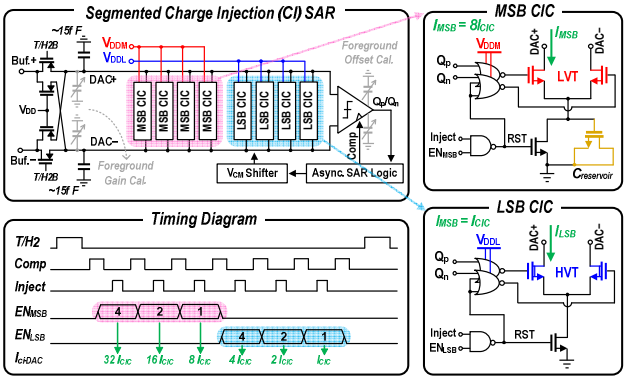

Fig. 2. Proposed segmented CI-SAR slice ADC.

Fig. 2 illustrates the proposed CI SAR ADC as well as the timing diagram and CI cell structures. To minimize the number of CICs, the CI-DAC uses two types of CICs (MSB and LSB CIC), each nominally drawing $I_{MSB}=8I_{CIC}$ and I_{CIC}, respectively, to realize 6-bit CI-DAC. The MSB CIC has a ~2 fF MOS capacitor ($C_{reservoir}$) on the source of the transfer device to realize substantially large current difference compared to the LSB CIC. To minimize area, the physical size of the MSB CIC is almost the same as LSB CIC by using separate CI gate bias voltages and device types, i.e., V_{DDM} for MSB CIC using LVT and V_{DDL} for LSB CIC using HVT, respectively.

Note that the $I_{MSB}=8I_{CIC}$ should hold over global voltage and temperature variation for robust operation. Shown in Fig. 3, two mixed-signal feedback loops consisting of replica MSB and LSB CICs constantly update the CI cell bias voltages, V_{DDM} and V_{DDL}, such that that the $I_{MSB}=8I_{CIC}$ is maintained over environmental variations. Specifically, in the V_{DDM} generation feedback loop, fixed reference DC input corresponding to ADC output of 8 LSB is applied and the converged V_{DDM} through the feedback minimizes the ADC input full-scale fluctuation over environmental variation [8]. The V_{DDL} generation loop compares the charge pulled by one MSB CIC and eight LSB CICs. In this V_{DDL} loop, the MSB CIC is biased by the V_{DDM} forwarded from the V_{DDM} generation loop. The digital controller accumulates the comparison outputs and adjusts the resistor-DAC (RDAC) that generates the V_{DDL} in such a way that the $I_{MSB}=8I_{CIC}$ holds. Note that unlike [8] where an entire ADC is used as a replica to generate the CI-cell bias voltage, only the replica pulse generator is employed to reproduce the injection pulse for the replica MSB and LSB CICs, significantly reducing area overhead. Moreover, the power and area overhead of this feedback loop are amortized since 32 slice ADCs share the same bias voltages. Overall, the presented CI-SAR uses only 8 CICs and 2 metal capacitors while achieving 7b-0.94GS/s in 294μm^2 per ADC slice.

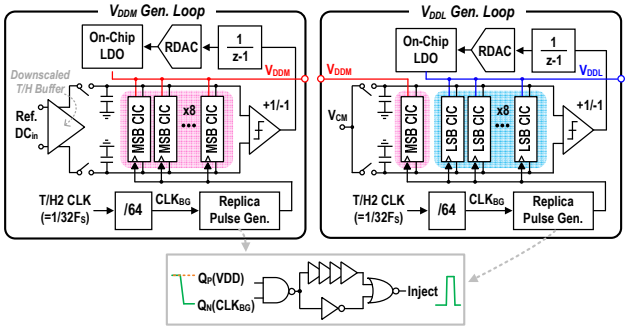

Fig. 3. Feedback-loop-based bias generator.

III. FRACTIONAL-FIR BASED TIMING SKEW CALIBRATION

A. Singularity in Correlation-based Skew Calibration

The conventional correlation-based skew detection method fails to work when the input signal frequency (F_{in}) is harmonically related to the ADC sampling frequency (F_s), i.e., $F_{in}=F_s/N$ with N being an integer. Let us imagine a 4-channel TIADC in which x_1, x_2, x_3 and x_4 are the sequential ADC outputs from each channel, respectively, and the two-step calibration process is illustrated in Fig. 4. In step 1, the average difference between $(x_3-x_1)^2$ and $(x_3-x_{1*})^2$ is proportional to the timing mismatch (ΔT) when aligning channel 3 using channel 1 as a reference [3]. In step 2, however, when aligning channel 2 (or 4) against channel 3, the average powers from channel 1 and channel 3, σ_1^2 and σ_3^2, do not cancel out when $f_{in}= f_{sam}/N$. This is because the same set of outputs are sampled repeatedly in each channel when input is harmonically related to sampling clock frequency.

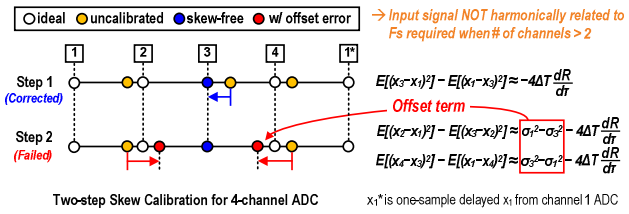

Fig. 4. Illustration of the singularity case in the conventional correlation -based background timing mismatch calibration technique.

To numerically verify our claim, a behavioral TIADC model in MATLAB has been set up where 4 ADCs are time-interleaved. Fig. 5 shows the simulated D(ΔT) of channel 2 vs. timing skew error assuming that channel 3 is skew-free, where the D(ΔT) is the difference between the average distance between channels. The left of Fig. 5(a) indicates that the D(ΔT) is proportional to the ΔT when nonharmonic input is applied, which is a normal behavior. On the other hand, shown at the right of Fig. 5(a), the D(ΔT) fails to detect ΔT when subharmonic inputs (F_{in}/F_s=1/2, 1/4, 1/8 and 1/16) are applied, in which case

D(ΔT) exhibits zero error or error with a large DC offset. Fig. 5(b) shows simulated D(ΔT) over F_{in}/F_s in which we want to detect the channel 2 timing skew when actual timing mismatch is +1%. The result reveals that the D(ΔT) is zero or with large DC offset at F_{in}/F_s=1/N, illustrating the case when the correlation-based timing calibration fails.

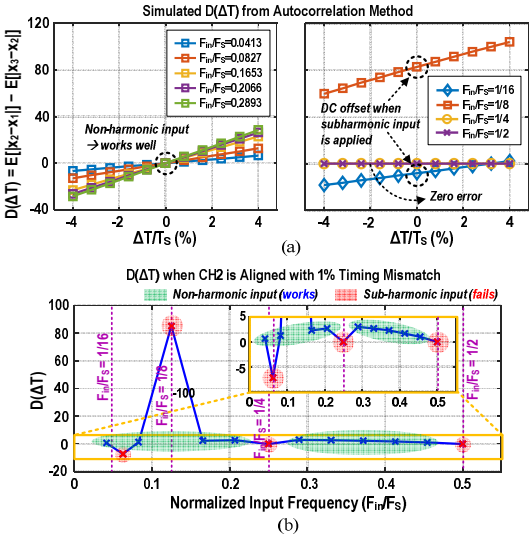

Fig. 5. Simulated D(ΔT) from autocorrelation based method.

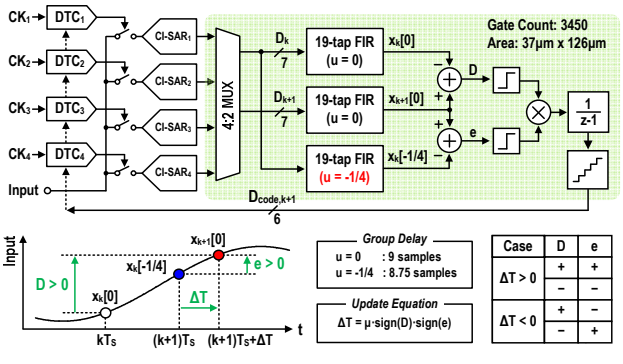

Fig. 6. Proposed timing skew calibration using fractional-delay FIR filter.

B. Proposed Timing Skew Calibration

Fig. 6 displays our full-digital background timing skew calibration system, in which the calibration logic takes digitized ADC outputs from two adjacent channels (D_k and D_{k+1}) and generates three outputs ($x_k[0]$, $x_{k+1}[0]$, and $x_k[-1/4]$) using three digital filters. The digital filters that produce $x_k[0]$ and $x_{k+1}[0]$ are all-pass 19-tap FIR filters with group delay of 9 samples. The number of taps was chosen considering the tradeoff between the calibration accuracy and area. The filter that produces $x_k[-1/4]$ is a fractional-delay FIR filter having a group delay of 8.75 samples, where 0.25 sample delay corresponds to the ideal time difference between adjacent channels given that four 1st rank samplers are used in our TIADC. Since $x_k[-1/4]$ is a digital reproduction of $D_{out,k+1}$, without any timing skew, $x_{k+1}[0]-x_k[-1/4]=0$ should hold. Therefore, by calculating $D=x_{k+1}[0]-x_k[0]$ and $e=x_{k+1}[0]-x_k[-1/4]$, one can identify the direction of the timing skew. The table at the bottom-right in Fig. 6 summarizes how the polarity of the timing skew is detected based upon D and e. In implementation, the settings for the DTCs in the 1st-rank sampler are updated using the sign-sign LMS algorithm based on D and e.

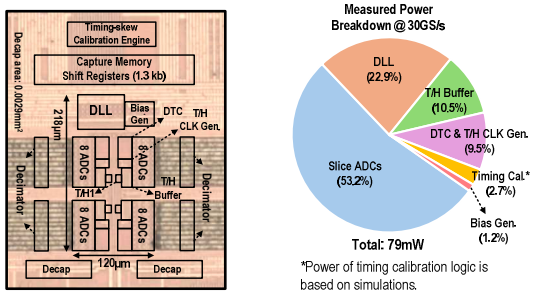

Fig. 7. Die micrograph (left) and power breakdown (right).

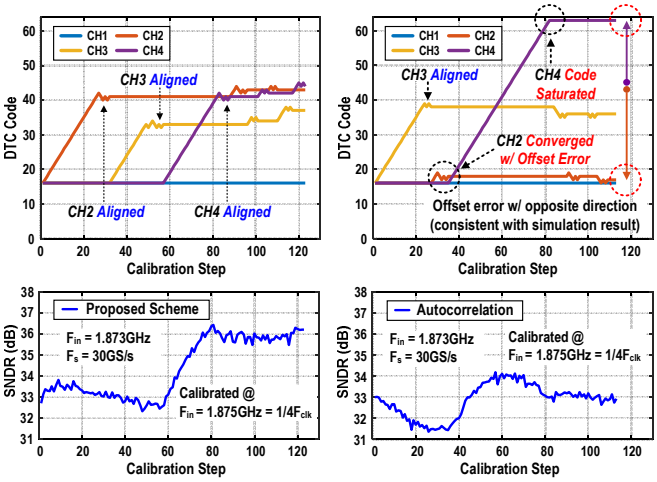

Fig. 8. Measured convergence (1536 samples/step) of the proposed scheme (left) and the autocorrelation (right) when subharmonic input is applied.

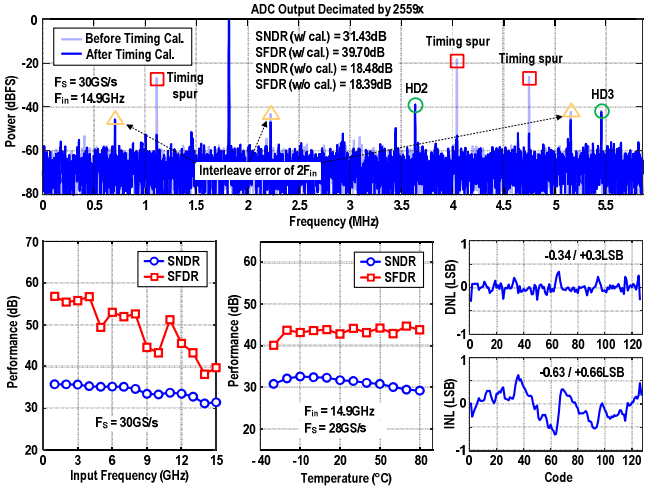

Fig. 9. Measured spectrum of the decimated (2559x) ADC output (top), SNDR, SFDR vs. input frequency, temperature robustness, and DNL/INL (bottom).

Conceptually, the proposed algorithm in Fig. 6 is similar to the derivative-based algorithm in [6], [7] but our method has an advantage of not needing any extra analog hardware and works entirely in the digital domain. In contrast, extra slice ADCs are required in [6] and [7], which considerably increases the design complexity. Note that due to the sampled nature of the fully-digital implementation, our algorithm works only up to the Nyquist input frequency of the 1st rank sampler, which is $F_{in,max} = F_{clk}/2$ where F_{clk} is the 1st rank sampling frequency.

IV. Experimental Results

Shown in Fig. 7, the ADC fabricated in 28nm CMOS occupies only 0.032mm^2, which is one of the smallest among all published ADCs with >30GS/s. The total consumed power including the quadrature clock generator, entire TIADC core, and the digital calibration logic is 79mW, leading to an FoM$_w$ of 86.5fJ/conv-step. The digital calibration is implemented on-chip to estimate the area of the digital calibration logic, which is only 14.5% of the analog TIADC core. In measurements, foreground calibration is applied to correct gain and offset mismatches, while the timing skew is background calibrated when F_{in}<2GHz and is frozen in the higher input frequency. This is because the group delay and magnitude response of the 19-tap fractional-delay all pass FIR filter stays flat up to $0.35\times F_{clk} \approx 2.6$GHz. Also, the bandwidth mismatch beyond F_{in}>3GHz was foreground calibrated. A 0.9V/1.1V supply and input full scale of 0.5V$_{ppd}$ are used in measurements.

TABLE II. Comparison with State-of-the-Art

	This Work	ISSCC'24 Martens	ISSCC'24 Whitcombe	VLSI'24 Nani	JSSC'23 Zhu	VLSI'22 Yonar	ISSCC'21 Nguyen	ISSCC'23 Agrawal
Slice ADC Architecture	CI-SAR	Slope	TDC-assist SAR	SAR	pipe-SAR	SAR	SAR	TDC+SAR
Process (nm)	28	16	22	5	22	4	7	22
Sampling Rate (GS/s)	30	42	40	60	38	56	97	40
Interleaving Factor	32	768	48	64	32	64	128	48
Resolution (b)	7	7	7	7	7	8	8	7
SNDR (dB) @ LF (GHz)	35.74	32.5	37.3	35.5	39.26	41.0	41	35.4
SNDR (dB) @ HF (GHz)	31.43	28.9	32.3	34.3	35.6	32.8	32	30.7
Power (mW)	79	96	76.4	109.3	119.7	240	305	104
ADC Area (mm^2)	0.032	0.056*	0.080*	0.068	0.107	0.078	N/A	0.138*
Slice ADC Area (μm^2)	294	35	644*	N/A	648	925*	N/A	N/A
Supply Voltage (V)	0.9/1.1	0.8	0.85	0.9	0.85/0.9	0.8	0.9/1.2	1.0
FoM$_w$ (fJ/c-s) @ LF	52.6	66.6	31.7	37.3	43.7**	47	34	54.1
FoM$_w$ (fJ/c-s) @ HF	86.5	101	56.7	42.88	64.05**	117	96	92.8
Timing Cal. Background?	Yes	No	No	No	No	No	N/A	No

	This Work	JSSC'13 Stepanovic	VLSI'22 Chang	VLSI'24 Park	VLSI'22 Moon	JSSC'14 Wei
Timing-skew Calibration Technique	Fractional-delay FIR Filter based SS-LMS	Dummy Channel based SS-LMS	Relative-prime Rotation based Autocorrelation	Absolute Error-based Autocorrelation	Autocorrelation	Conventional Autocorrelation
Require Extra Analog Hardware?	No	2 ADCs	1 ADC	No	No	No
Support Subharmonic Input? ($F_{IN} = F_S/N$)	Yes	Yes	Not Reported	No	No	No

* Estimated from the die photograph ** Multi-phase clock generator NOT included

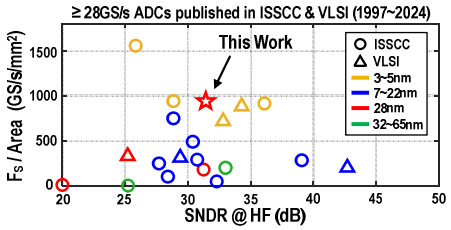

Fig. 10. Comparison of the ADC area efficiency.

To test timing calibration, non-decimated full-speed ADC outputs are stored in an on-chip 1.3kb memory and taken offline for easier testing. The left of Fig. 8 shows a successful convergence of the timing skew calibration algorithm for subharmonic input with $F_{in}=F_{clk}/4$ where F_{clk}=7.5GHz. The convergence is reached after 135k samples, corresponding to a convergence time of 135μs when the digital calibration logic runs at 500MHz. Also, the right of Fig. 8 verifies that the correlation-based method fails for the same input signal.

Shown in Fig. 9, the decimated ADC output spectrum shows the SNDR and SFDR of 31.43 dB and 39.70 dB when Nyquist input is applied. The measured ENOB at 30 GS/s is 5.6b when F_{in}=1GHz and 4.9b when F_{in}=14.9 GHz, respectively. The ADC performs reliably at 28GS/s over the temperature range from -30°C to 80°C. Table II and Fig. 10 summarize the comparison of this work with state-of-the-art, highlighting the unparalleled area efficiency of our TIADC and the versatility and simplicity of the presented timing-skew calibration method.

V. Conclusions

This paper introduces a CI-SAR based TI-ADC with a very small form factor, boasting an area efficiency comparable to those fabricated in 3~5nm process nodes. The proposed 32-way TI-ADC samples the output at 30GS/s, with an area of only 0.032mm^2. Simple mixed-mode feedback loops maintain the linearity of the CI-SAR ADC in the background. A factional-delay FIR filter based full digital background timing skew calibration effectively fills the blind spots of the conventional correlation-based scheme with minimal extra hardware overhead. Therefore, our algorithm is applicable even when the ADC F_{in} and F_{clk} are harmonically related, which can happen in wireline links with a common PLL reference clock for both the transmitter and receiver.

Acknowledgment

The authors thank IDEC and KAIST for CAD support and chip fabrication. This work is supported by Samsung Research Funding Center under SRFC-IT2302-03.

References

[1] H. Park et al., "A 4.63pJ/b 112Gb/s DSP-Based PAM-4 Transceiver for a Large-Scale Switch in 5nm FinFET," *IEEE ISSCC*, 2023.

[2] A. S. Yonar et al., "An 8-bit 56GS/s 64x Time-Interleaved ADC with Bootstrapped Sampler and Class-AB Buffer in 4nm CMOS," *IEEE VLSI*, 2022.

[3] H. Wei, P. Zhang, B. D. Sahoo and B. Razavi, "An 8 Bit 4 GS/s 120 mW CMOS ADC," in *IEEE JSSC*, vol. 49, no. 8, pp. 1751-1761, Aug. 2014.

[4] K. -J. Moon et al., "A 12-bit 10GS/s 16-Channel Time-Interleaved ADC with a Digital Processing Timing-Skew Background Calibration in 5nm FinFET," *IEEE VLSI*, 2022.

[5] D. -J. Chang and S. -T. Ryu, "A Relative-Prime Rotation Based Fully On-Chip Background Skew Calibration for Time-Interleaved ADCs," *IEEE VLSI*, 2022.

[6] D. Stepanovic and B. Nikolic, "A 2.8 GS/s 44.6 mW Time-Interleaved ADC Achieving 50.9 dB SNDR and 3 dB Effective Resolution Bandwidth of 1.5 GHz in 65 nm CMOS," in *IEEE JSSC*, vol. 48, no. 4, pp. 971-982, April 2013.

[7] H. -W. Kang, H. -K. Hong, S. Park, K. -J. Kim, K. -H. Ahn and S. -T. Ryu, "A Sign-Equality-Based Background Timing-Mismatch Calibration Algorithm for Time-Interleaved ADCs," in *IEEE TCAS-II*, vol. 63, no. 6, pp. 518-522, June 2016.

[8] J. Kim, G. Cho and J. Kim, "A 7 GHz ERBW 1.1 GS/s 6-bit PVT Tolerant Asynchronous Charge-Injection SAR With Only 8.5 fF Input Capacitance in 28 nm CMOS," in *IEEE JSSC*, vol. 59, no. 3, pp. 765-773, March 2024.

[9] C. -H. Kye and K. Choo, "A 0.000261 mm2 Single-Channel 1 GS/s 8-Bit 3-Stage Capacitor Array-Assisted Charge-Injection DAC-Based SAR ADC in 28 nm CMOS," *IEEE A-SSCC,* 2023.