Cryogenic 22nm FD-SOI Circuit Measurements and Compact Modeling L-UTSOI: From Transistor-Level Effects to System Performance

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***Abstract*—This paper presents the first complete benchmark of the standard L-UTSOI compact model from the transistor behaviour to system performance at cryogenic temperatures. The proposed model effectively captures the complete behaviour of 22 nm FD-SOI devices at 4 K, across operating regions from linear to saturation. Furthermore, the study of both measurement and simulation results on a complete ring oscillator circuit, with its integrated test architecture, confirms the relevance of the model for cryogenic applications. Specifically, the model accurately predicts measured frequency and consumption for various back-gate voltages at cryogenic condition, achieving an average error of less than 2 % , under nominal biasing conditions. Finally, given its compatibility with standard design and SPICE simulation environments, this work establishes proposed model as a valuable tool for predicting, Optimising, and anticipating specific cryogenic effects in cryo-CMOS circuit performance.**

***Index Terms*—cryo-CMOS, compact modeling, FD-SOI, quantum computing, cryogenic temperature, ring oscillator.**

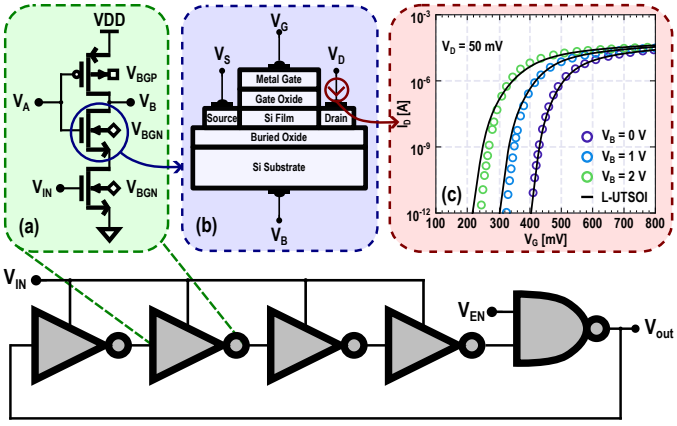

Fig. 1. Ring oscillator architecture selected for the validation of the L-UTSOI model. (a) Voltage-controlled delay inverter, (b) simplified device structure, and (c) example of L-UTSOI modeling in large signal for an n-MOS transistor with $W/L = 1\,\mu m/1\,\mu m$ at 4 K (markers represent the measurement data).

I. Introduction

Cryogenic electronics based on MOS transistors (cryo-CMOS) gaining significant interest in two main cases of applications. The first includes strategic use cases where cryo-CMOS offers substantial performance gains over room temperature operation, as demonstrated in [1], [2]. For example, this has led to research initiatives exploring cryo-computing as a means to enhance performance and energy efficiency [3]. However, the primary driver of cryo-CMOS development lies in applications that intrinsically require cryogenic operation. The most prominent example is quantum computing [4], where cryo-CMOS presents a unique solution for the biasing, manipulation, and readout of qubits [5]–[7], enabling scalable architecture as required by quantum error correction [8].

The development of cryo-CMOS circuits presents significant challenges. On one hand, achieving high performance and low power consumption requires deeply optimized designs, as needed by the limited cooling capacity of cryostats. On the other hand, the absence of dedicated cryogenic process design kits (PDKs) has hindered precise circuit optimization at cryogenic temperatures. Consequently, most designs rely on room-temperature optimizations using standard PDKs, lacking of precise adjustments for cryogenic effects. While FD-SOI technology offers advantages in mitigating threshold voltage challenge without affecting leakage current [9], it remains insufficient and, like CMOS, it requires accurate compact models to anticipate and account for cryogenic behaviour, as proposed in works [10], [11].

This paper extends the cryogenic L-UTSOI library initially proposed for p-MOS [11] to n-MOS devices in 22 nm FD-SOI technology. Beyond this extension, it provides the first complete benchmark of the L-UTSOI model from the transistor level to circuit implementation at cryogenic temperatures. This validation is conducted through SPICE simulations and cryogenics measurements of an integrated circuit, designed in FD-SOI technology, as illustrated in Fig. 1. The test study is a five stage voltage-controlled ring oscillator, enabling a rigorous assessment of the model accuracy. To achieve this, we first present the proposed model, along with key insights into cryogenic effects on available devices. Next, we detail the validation methodology, addressing the challenges and design choices that ensure a meaningful comparison between measurement and modeling. Finally, we apply this methodology to the full circuit, presenting key results and observations before concluding on the model relevance for cryo-CMOS design.

II. Assessment of L-UTSOI Cryogenic Model

Validation of the proposed cryogenic model and assessment of the effect of temperature on circuit performance requires a evaluation of n-MOS and p-MOS low threshold voltage (V_T) flip-well devices. The L-UTSOI version 102.7 compact model is utilized for both device types. Calibration of n-MOS devices begins with the extraction of process-related parameters, such as gate oxide thickness (tox), from the gate-to-channel capacitance (C_{GC}) versus gate voltage (V_G) curves. Then, electrostatic and mobility parameters are then derived from the drain current (I_D) versus V_G curves for a long and wide transistor, as shown in Fig. 1(c). To take into account short channels effects and the channel length modulation, I_D-V_G curves are fitted with L at 20, 40, 100, 500, and 1000 nm for a W of 1 µm. Edge effects are incorporated by fitting W at 80, 120, 170, 300 and 1000 nm with an L of 1 µm. To capture the extreme geometry, an additional point of W 80 nm and L 20 nm was used. This calibration procedure mirrors the p-MOS calibration detailed in [11] and enables the generation of a global cryogenic model map capable of processing simulations for different geometries. In order to minimize the impact of variability, we extract data on transitors located on the same die. Finally, during calibration, the effect of the cryogenic environment on device performance is evaluated for n-MOS.

The independent parameters governing drain current, such as inversion charge and mobility, must be analyzed to fully capture the impact of device physics. C_{GC}-V_G curves for 300 K and ∼4 K are presented in Fig. 2 (left). The 300 K, used as a comparison, represents the standard BSIM model for the 22 nm FD-SOI (calibrated for a typical case), while the 4 K curves are fitted using L-UTSOI model. At cryogenic temperatures, capacitor inverts more abruptly and at higher V_G values (∼450 mV compared to ∼280 mV at 300 K). Apart from the steepest transition to inversion, the maximum inversion charge remains relatively constant at both room and cryogenic temperatures, suggesting that current carriers in strong inversion are primarily governed by technological parameters. Given the model's accuracy in fitting charge and current curves, the effective mobility (μ_e) is simulated as function of V_G for V_B 0 V using the split capacitance voltage method [12], as shown in Fig. 2 (right). A substantial increase in maximum mobility (∼350 cm^2/(V·s)) is observed at cryogenic temperatures, consistent with FD-SOI technologies [13].

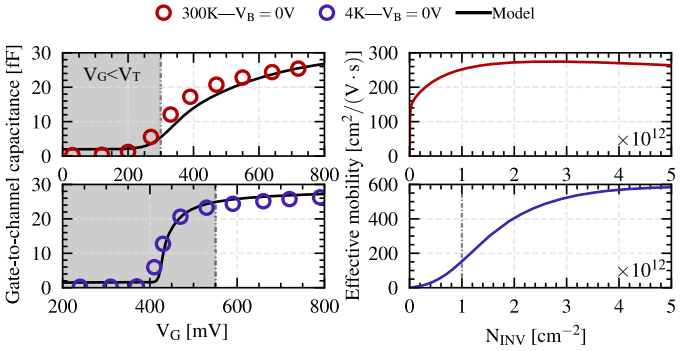

Fig. 2. Measurement and modelling results of C_{GC} and μ_e for n-MOS $W/L = 1\,\mu m/1\,\mu m$ versus V_G. Markers are the measurement data, and for model, the upper curve corresponds to 300 K and the lower to 4 K.

Subsequently, the ON current (I_{ON} = I_D at V_D = V_G = V_{DD}), V_T, and Drain-Induced-Barrier-Lowering ($DIBL$) are assessed. The models are benchmarked against experimental result, with figures of merit for various channel lengths at 300 K and 4 K as shown in Fig. 3. Both models exhibit a good fit to the experimental data. The 300 K model is calibrated using a typical centered die, whereas measurements are taken from an arbitrary die on the wafer, resulting in a small deviation from the expected values. 4 K model is calibrated directly using the capacitance and I_D curves for each geometry as mentioned in [11]. Although the devices overall behavior is well captured, discrepancies from experimental values are observed. These discrepancies are attributed to cryogenic effects not yet incorporated into the L-UTSOI model, such as localized states in the silicon channel [14] or intersubband scattering [15]. Additionally, variations arise from the random die selected on the wafer and the limited number of extraction points, which can significantly deviate from the average (e.g., W 300 nm at 4 K). However, most of these inaccuracies affect $DIBL$ in long-channel devices, where the impact on circuits is negligible. This allows a compromise in the library to accurately fit I_{ON}, which is more critical for these channel lengths, despite of variability. Devices I_{ON} exhibits an approximately 8% maximum increase for n-MOS devices, despite a substantial mobility increase at lower temperatures. This increase is likely attributed to additional factors, such as device self-heating [16], which becomes more significant at higher drain voltages. Notably, the back-gate voltage (V_B) enhances I_{ON} due to reduced V_T and increased μ_e resulting from back-channel formation. This distinctive feature of SOI transistors is particularly advantageous for cryogenic applications, as it mitigates the increase in V_T at low temperatures. With key device properties established and the model calibrated, the performance of cryogenic circuits is then analyzed.

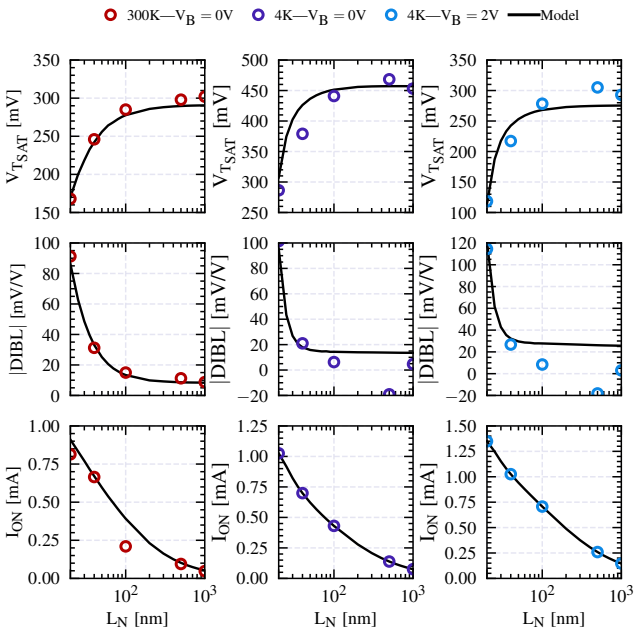

Fig. 3. Measurement and modelling results V_T, $DIBL$ and I_{ON} as a function of channel length for wide n-MOS (W = 1 µm).

III. Benchmark Methodology

Figure 4 illustrates the test architecture employed for the first phase of our validation methodology, at circuit level, of the extracted library using L-UTSOI. This setup enables the cryogenic characterization of the ring oscillator using a dipstick immersed in a liquid helium dewar at ∼4 K. Dipstick is wired with low-impedance copper cables for DC biasing and a 50 Ω transmission line for output signal, which connects to the daughter board, through the motherboard, where die are located in QFN48-package. In addition, the circuit integrates a 1 to 1024 frequency divider, implemented with 22nm FD-SOI standard cells, to mitigate the parasitic caused by this environment and bandwidth limitations on the transmission line. The circuit is controlled with selector signal from 300 K and also includes a ratiometric output buffer to drive the transmission line. The results presented in the section IV correspond to a 1024 division factor, though additional validation confirmed a negligible impact on frequency mesurement accuracy across temperature and division factors. Finally, to ensure precise and automated measurements, a high-end spectrum and signal analyzer is used for frequency analysis, while low-noise, high-resolution digital-to-analog converters provide circuit biasing.

The second phase involves a comprehensive SPICE simulation of the complete circuit using the cryogenic library. This is conducted within the Cadence Virtuoso design environment for 22nm FD-SOI technology, employing the Spectre simulator on a post-layout extraction of the full chip in a typical process corner. To ensure correlation with measurements, the simulation test bench incorporates an accurate modeling of the experimental setup, including resistive extraction of the dipstick copper wires and S-parameter characterization of the transmission line. Finally, a transient simulation initiated by enable signal (V_{EN}) is performed and compared with measurement results, as described in the following section.

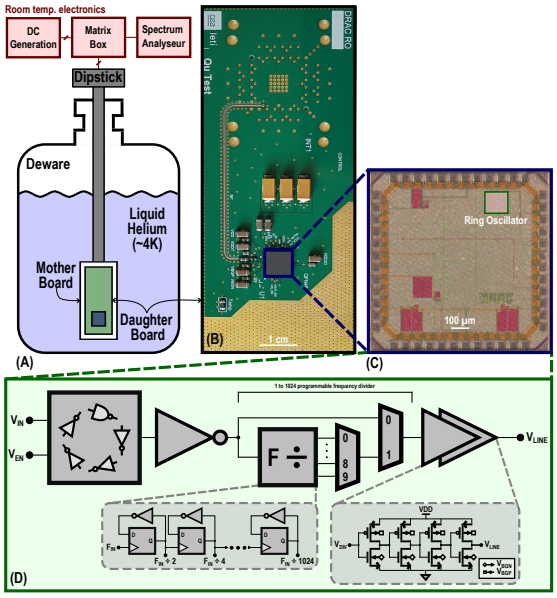

Fig. 4. (a) Simplified representation of the dewar with the test environment, (b) Daughter board used for cryogenic measurements, (c) Die micrograph, and (d) Integrated architecture for ring oscillator testing.

IV. Measurement and Modelisation Results

Frequency performance is proportional to the inverter delay, which can be approximated by $C_L \cdot V_{DD}/I_{inv}$, where C_L is the load capacitance at the output of each inverter which is mainly due to layout parasitics plus C_{GC}, and V_{DD} is the supply voltage of the circuit, to the target output amplitude. Regarding I_{inv}, the output current of inverter, it is controlled by the input voltage (V_{IN}) through M_{N2}, as seen in Fig. 1, in a range from V_T to V_{DD} and is proportional to μ_e. Accordingly, when the circuit is cooled, C_{GC} remains constant, V_T increases without forward body bias F_{BB} and μ_e increases, resulting in a small delay improvement in a reduced range of V_{IN}, based on previous simplified relationship. With the same hypothesis, the use of F_{BB} improves the range of control and performance.

Figure 5 presents the cryogenic test and modelling results of the complete circuit, obtained with Fig. 4 set-up, for different configurations. The experimental results confirm the simplified hypothesis, showing improved performance and enhanced control range with F_{BB}. The cryogenic library exhibits the same improvement trend with F_{BB}, demonstrating good agreement between measurements and simulations, though a slight degradation in accuracy is observed as V_{DD} decreases. Specifically, the average error between frequency measurement and modeling reaches 1.8, 1.9, and 6.9 % for 0.8, 0.6, and 0.5 V of V_{DD}, respectively, under nominal biasing. This discrepancy can be primarily attributed to device variability, as simulations are performed under the typical calibration of the L-UTSOI model, which itself exhibits intrinsic variability relative to the golden die of the technology, as does devices in the circuit. Additionally, the device W/L chosen for the ring oscillator were not explicitly covered in the 10 devices used for model extraction, leading to interpolation between different geometries in the model. Despite these factors, the model successfully captures the predicted performance improvements.

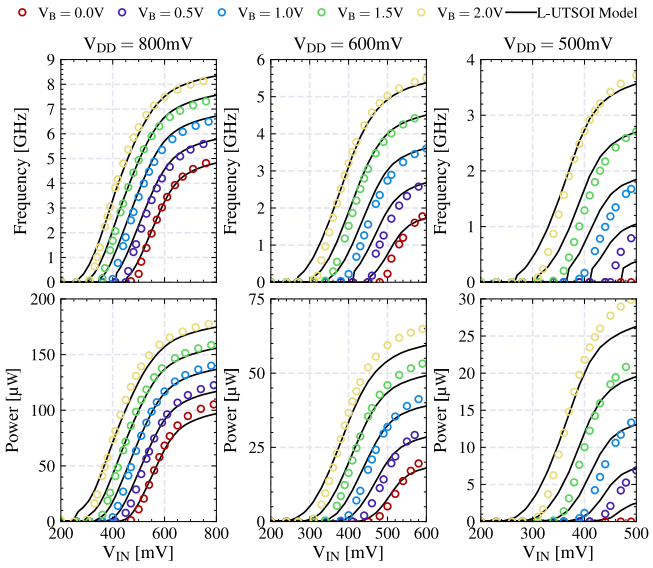

Fig. 5. Frequency and power results versus oscillator input voltage. Markers represent cryogenic measurement (4 K), while solid lines L-UTSOI simulations. V_B correspond to n-MOS back-gate voltage and p-MOS to its opposite ($V_{B_P} = -V_{B_N}$).

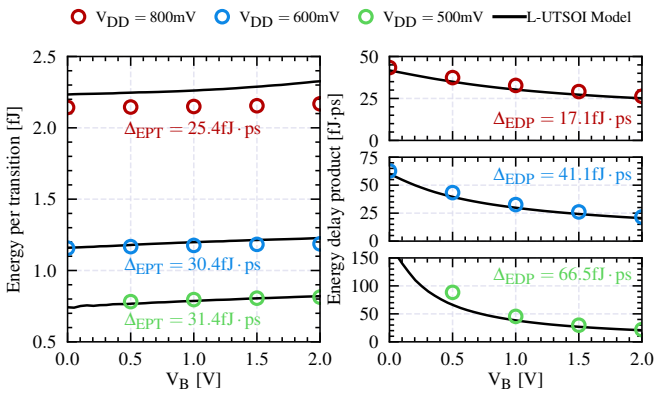

Fig. 6. Energy per transition and Energy-delay product cryogenic measurement and L-UTSOI simulation results versus F_{BB}, considering $V_{IN} = V_{DD}$.

Figure 6 presents two key figures of merit for the ring oscillator as a function of supply voltage. The first, energy per transition (EPT), relates power consumption to operating frequency through the inverter delay, defined as $EPT = P \cdot \tau_{inv}$. The second, energy delay product (EDP), is given by $EDP = P \cdot \tau_{inv}^2$, as proposed in [17], [18]. The L-UTSOI model nicely matches the experimental results and highlights the advantage of FD-SOI technology, which maintains an almost constant EPT across F_{BB}. This behavior can be attributed to the native support for F_{BB} and the reduced leakage at cryogenic temperatures, enabling full F_{BB} utilization to enhance mobility and lower V_T without compromising EPT. This is a key strength compared to conventional CMOS F_{BB} techniques, which induce large EPT variations at constant supply voltage, as depict in [17]. However, traditional CMOS approaches offer other advantages, including lower cost, and lower self-heating. Moreover, applying a high F_{BB} significantly improves EDP, particularly at low V_{DD}. Finally, Tab. I summarizes the measurement results at 300 K and 4 K, along with variations across F_{BB} for the nominal condition.

V. Conclusion

This paper demonstrated, through experimental results, that the L-UTSOI standard model can accurately predict the cryogenic circuits performance and effectively captures the physics of both n-MOS and p-MOS 22nm FD-SOI devices at low temperature. Furthermore, the study of both measurement and simulation results on a complete ring oscillator circuit, with its integrated test architecture, confirmed model relevance for cryogenic applications. Specifically, the model reproduced the measured performance improvement at cryogenic temperatures, achieving roughtly constant (2.3 %) in EPT and 51 % gains for EDP, under nominal conditions with forward body biasing. Finally, given its compatibility with standard design and SPICE simulation environments, this work establishes the L-UTSOI model as a valuable solution for predicting, optimizing, and anticipating specific cryogenic effects in Cryo-CMOS circuit performance. Future research should focus on incorporating additional cryogenic effects and studying variability to further enhance the accuracy of the library based on the L-UTSOI model and circuit analysis.

TABLE I
Comparison of key performance metrics across temperature under nominal biasing condition

Temperature	$[K]$	300	4			
V_B	$[V]$		0		2	
		Transistor (V_G = V_D= 0.8 V)				
μ_e	$[cm^2/V_s]$	259	586	↗126%	772	↗ 198%
C_{GC}	$[fF]$	26.8	27.2	↗ 2%	26.5	↘ 1%
$V_{T_{SAT}}$	$[mV]$	280.5	467.2	↗ 67%	275	↘ 2%
		Ring Oscilator (V_{IN} = V_{DD} = 0.8 V)				
Power	$[\mu W]$	91.9	105.8	↗ 15%	178.8	↗ 95%
Frequency	$[GHz]$	4.1	4.9	↗ 19%	8.3	↗ 99%
EPT	$[fJ]$	2.22	2.14	↘ 3.6%	2.17	↘ 2.3%
EDP	$[fJ \cdot ps]$	53.3	43.4	↘ 19%	26.3	↘ 51%

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