Low-Frequency Noise Characterization of sub-μm a-IGZO TFTs using both mobility fluctuation and UTSOI 2 models

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***Abstract*—We characterize the low-frequency noise (LFN) behavior of amorphous indium gallium zinc oxide (a-IGZO) thin-film transistors (TFTs) fabricated by Pragmatic Semiconductor. The LFN, often referred to as flicker noise, mainly follows the carrier mobility fluctuations (CMF) model, and the extracted Hooge's parameter (α_H) is around 2 × 10^{-3}, which is quite low compared to the results from literature. We also use the commercial simulation model (UTSOI 2) to model the low-frequency noise behavior which is compatible with the PDK provided by the foundry. The measurement results, the theoretical carrier mobility fluctuation model, and the tuned UTSOI 2 model match with each other, which enables simulating low-noise circuit designs using sub-μm a-IGZO TFTs.**

***Keywords*—LFN, flicker noise, thin-film transistor, a-IGZO, carrier mobility fluctuations model, Hooge's parameter, UTSOI 2**

I. Introduction

Thin-film transistors (TFTs) have been extensively employed in display applications due to their uniformity, low-cost large-area fabrication, and flexible characteristics. Among various TFT technologies, amorphous indium gallium zinc oxide (a-IGZO) TFTs have attracted significant attention owing to their relatively high electron mobility (~10 cm²/V·s) and superior electrical performance compared with conventional amorphous silicon (a-Si) TFTs [1]. This advantage facilitates the transition from purely digital circuits [2] toward analog circuit designs [3]. In recent years, numerous analog circuits based on a-IGZO TFTs have emerged, particularly targeting biomedical applications such as ultrasound patches [4], EMG [5], ECG [6], and ECoG [7] sensors, benefiting from their inherent flexibility and compatibility with conformal attachment to the human body.

Given that biomedical signals are typically very weak, understanding and minimizing the noise characteristics of a-IGZO TFTs become crucial when designing readout circuits. Without proper noise characterization, these weak biomedical signals risk being overwhelmed by intrinsic noise from the circuit itself. However, there is limited existing research on noise characterization for commercially fabricated a-IGZO TFTs, which significantly hinders the development and optimization of TFT-based circuits intended for biomedical or other low-noise applications.

In this work, we systematically characterize the low-frequency noise behavior of a-IGZO TFTs fabricated by Pragmatic Semiconductor [8], a leading semiconductor foundry specializing in high-density sub-μm a-IGZO technology. The carrier mobility fluctuation (CMF) theory is employed to elucidate the origin of the observed low-frequency noise, and the associated Hooge's parameter is extracted. Furthermore, we calibrate the LFN parameters within the UTSOI 2 simulation model. Combining these calibrated parameters with the accurate DC and AC characteristics provided by the PDK with the UTSOI 2 model enables effective design of low-noise circuits. Designers can thus accurately estimate the required transistor dimensions to meet specific input-referred noise performance criteria in analog front-end circuits.

II. Experiment and Result Discussion

A. Low-frequency noise measurement

Low-frequency noise (LFN) measurements were conducted using Keysight's advanced low-frequency noise analyzer (E4727B) at room temperature. The analyzer first performs a gate-to-source voltage (V_{GS}) sweep while measuring the drain current (I_{DS}) to obtain the I_{DS}–V_{GS} and g_m–V_{GS} characteristics as depicted in Fig.1. The threshold voltage (V_{th}) of each transistor is extracted at the point where I_{DS} is 1×10^{-7}A. LFN measurements were performed in the linear regime, using a constant drain-to-source voltage (V_{DS}) of 0.1 V and predefined overdrive voltages (V_{OV}) of 1, 2, and 3 V, corresponding to typical biasing levels in analog circuit applications. Data were collected from 32 dies. On each die, transistors with different channel widths but identical channel length of 0.8 μm were measured.

B. Measurement result discussion

The mean values and 95% confidence intervals of the normalized drain current noise power spectral density (S_{IDS} / I_{DS}^2) for a-IGZO TFTs with different channel widths and overdrive voltages are presented in Fig. 2. All measured devices exhibit a $1/f^{\gamma}$ noise spectrum, with $\gamma \approx 1$ over the frequency range of 10Hz to 5000 Hz, consistent across various biasing and device geometries.

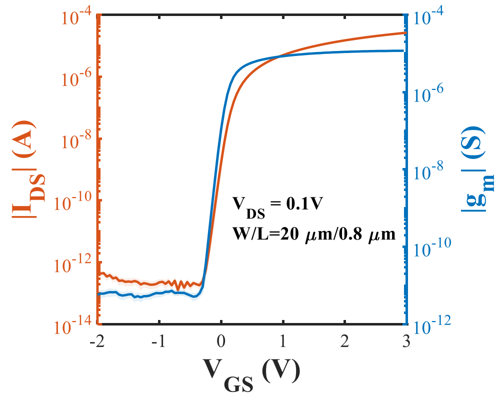


Fig. 1 I_{DS}-V_{GS} and g_m-V_{GS} curves, where the solid line represents mean value of the measurements from 32 dies, and the shaded region indicates the corresponding 95% confidence interval.

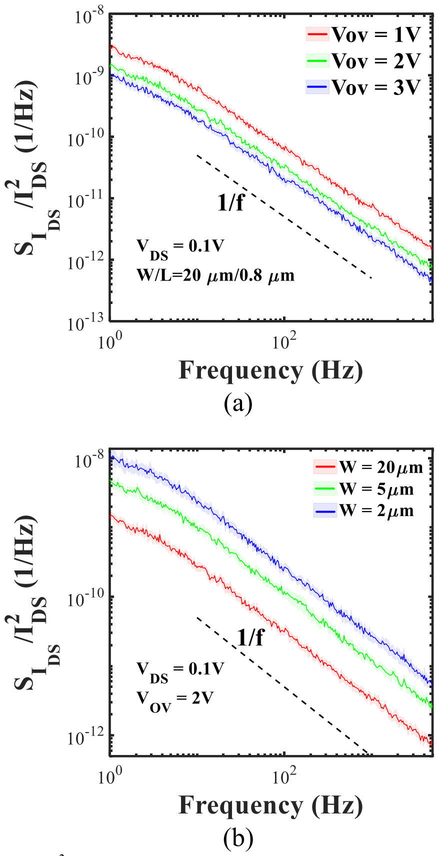


Fig. 2 S_{IDS} / I_{DS}^2 of a-IGZO TFTs as a function of (a) overdrive voltage (V_{OV}) and (b) channel width (W). The solid lines represent the mean values of the measurements, and the shade regions indicate the corresponding confidence intervals.

There are two primary theories that explain the origin of low-frequency noise (LFN) in semiconductor devices, each attributing the noise to different physical mechanisms. The first is the carrier number fluctuation (CNF) model, which explains LFN as a result of fluctuations in the number of free carriers available for conduction. These fluctuations arise from the trapping and de-trapping of carriers at defect states located either in the semiconductor or at the semiconductor–dielectric interface. This process causes temporal variations in carrier density, which manifest as noise in the drain current [9].

In the CNF model, the normalized drain current noise power spectral density is given by:

$$\frac{S_{IDS}}{I_{DS}^2} = \frac{q^2 kT n_{BT}}{\alpha W L C_{ox}^2 f} \frac{1}{(V_{GS}-V_{th})^2} \tag{1}$$

where q is the electron charge, k is the Boltzmann's constant, T is the temperature, n_{BT} is effective trap density in the dielectric, f is the frequency, C_{ox} is the gate insulator capacitance per unit area, W and L are respectively the width and length of the transistor, and α is the tunneling factor [10].

The second model is the carrier mobility fluctuation (CMF) theory, which attributes LFN to fluctuations in the carrier mobility. These fluctuations are caused by random scattering events, including interactions with phonons, impurities, or lattice defects [11], [12].

The CMF model is typically described by the empirical Hooge's relation [13], and its formula for transistors working at the linear region is [14]:

$$\frac{S_{IDS}}{I_{DS}^2} = \frac{\alpha_H}{Nf} = \frac{q}{C_{ox} W L f} \frac{\alpha_H}{(V_{GS}-V_{th})} \tag{2}$$

where α_H is the Hooge's parameter—a dimensionless empirical constant independent of bias [15], and N is the total number of carriers in the channel.

To distinguish between the two noise models, we examine the slope of the log-log plot of S_{IDS} / I_{DS}^2 at a fixed frequency versus V_{OV}. As shown in Fig. 3, the mean values and 95% confidence intervals of S_{IDS} / I_{DS}^2 at 90 Hz are plotted against different overdrive voltages for transistors with various channel widths. The slope is approximately −1, which is consistent with the CMF model. However, it should be noted that in practical devices, the 1/f noise is generally attributed to a combination of CMF and CNF. The observed behavior is therefore interpreted within the CMF framework as a dominant, but not exclusive, contribution. The Hooge's parameter can be extracted using the CMF formulation:

$$\alpha_H = \frac{S_{IDS}}{I_{DS}^2} \frac{C_{ox} W L f}{q} (V_{GS}-V_{th}) \tag{3}$$

The Hooge's parameter provides a convenient metric to compare noise performance among devices where the CMF model applies [16]. As shown in Fig. 4, the extracted α_H values versus V_{OV} are plotted for devices with different channel sizes. The values remain relatively constant around 2×10^{-3}, consistent with the dimensionless and bias-independent nature of Hooge's parameter. As illustrated in Fig. 5, the extracted α_H values are compared with prior studies on a-IGZO TFTs using different gate insulators. Our results are among the lowest

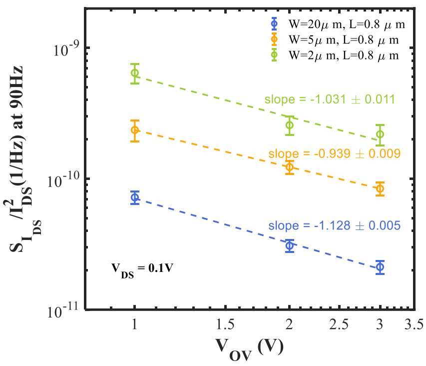


Fig. 3 S_{IDS} / I_{DS}^2 at 90Hz versus V_{OV} for a-IGZO TFTs biasing in the linear region. The hollow symbols are the mean values of measurements from 32 dies, and the error bars indicate the corresponding 95% confidence intervals. The slope extracted from the log-log plot is around -1.

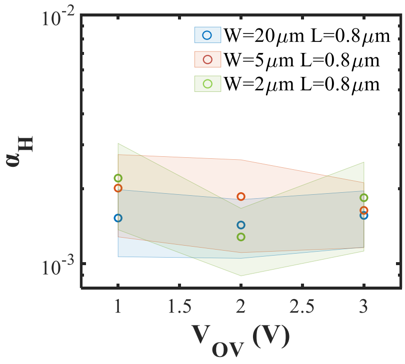


Fig. 4 Extracted Hooge's parameter in the linear region versus V_{OV}. The hollow circles and shaded regions are the mean and the corresponding confidence intervals.

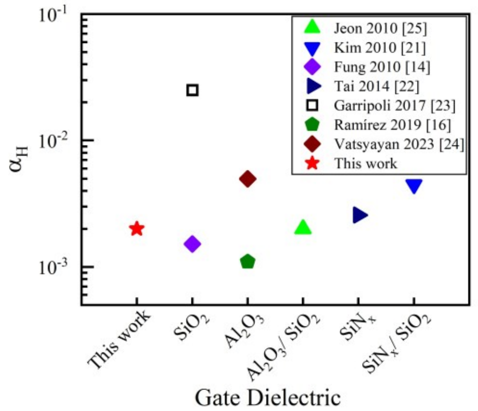


Fig. 5 Recently published Hooge's parameters for a-IGZO TFTs with various gate dielectric. Adapted from [16].

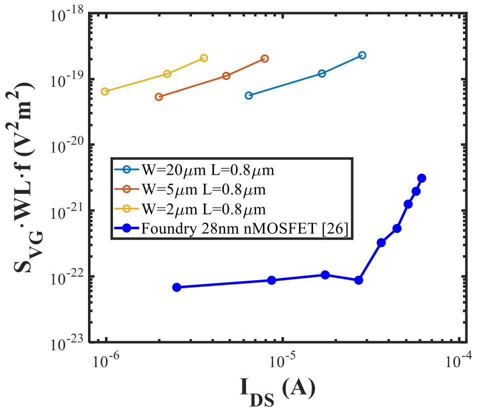


Fig. 7 $S_{VG}{\cdot}f{\cdot}WL$ at 20Hz versus I_{DS} from a-IGZO and 28nm Si nMOSFET (W = 1μm, L = 0.5μm)

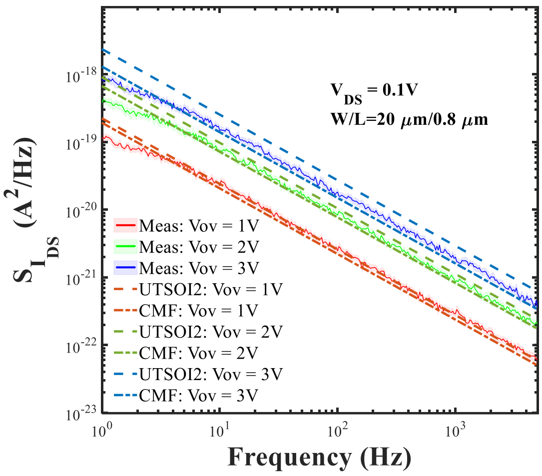
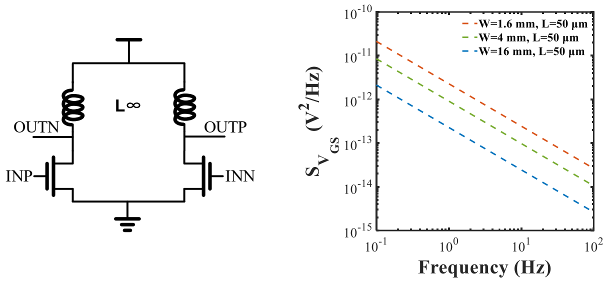


Fig. 6 S_{ID} comparisons of measurement results, theoratical CMF model, and calibrated UTSOI 2 model for the same transistor at different V_{OV}.



(a) (b)

Fig. 8 (a) The schematic of measuring the IRN only with the contribution from the input pair. (b) S_{VG} simulation result with different W but identical L.

reported in the literature, demonstrating that foundry's a-IGZO TFTs offer competitive noise performance.

The commercial UTSOI 2 model [17] can accurately simulate device characteristics. However, the LFN component in the provided PDK is initially uncalibrated. In the UTSOI 2 model, LFN is obtained by developing a surface-potential-based version of the CMF+CNF model [19], [20] and dependent on several fitting parameters, namely *NFA*, *NFB*, *NFC*, and *EF* [18], which account for different physical aspects of the noise behavior. After adjusting these parameters to $5{\times}10^{26}$, $5{\times}10^{-6}$, $2{\times}10^{-6}$, and 0.97 respectively, accurate noise simulations can be performed. As shown in Fig. 6, a high level of agreement is observed among measurements, simulations, and theoretical CMF prediction across devices with different sizes.

Direct comparison between devices with different noise mechanisms cannot rely on a single physical constant. In practice, analog circuit designers are concerned with both input-referred noise (IRN) and power consumption. To enable a meaningful comparison from a circuit design perspective, we plot $S_{VG}{\cdot}f{\cdot}WL$ at a fixed frequency, where S_{VG} is the voltage noise spectral density at the gate, as a function of I_{DS} as shown in Fig.7. In this plot, the x-axis (I_{DS}) can represent the power consumption of the circuit, and the y-axis ($S_{VG}{\cdot}f{\cdot}WL$) integrates both the noise level and the device's amplification capability, where the impact of device size is removed by normalizing S_{VG} with the transistor's area. The significant difference observed between the 28nm Si nMOSFET and a-IGZO TFTs predominantly attributable to the ~100× difference in carrier mobility, which is determined by the intrinsic properties of Si and a-IGZO transistors.

III. Design suggestions

After successfully characterizing the LNF behavior of the a-IGZO transistor, we can roughly estimate the size of the readout circuit's input pair in different IRN specifications. The S_{IDS} / I_{DS}^2 in saturation region is twice as large as the one in linear region [14]. Since the input pair always works in the saturation region, by taking g_m/I_{DS} = $2/V_{ov}$, S_{VG} can be formulated as:

$$S_{VG} = \frac{S_{IDS}}{g_m^2} = \frac{(V_{GS}-V_{th})q\alpha_H}{2C_{ox}WLf} \tag{4}$$

By integrating S_{VG} over the interested signal bandwidth and making it equal to the IRN specification, we can roughly estimate the required area of the input transistor assuming the LFN of the input transistor dominates the IRN by:

$$WL = 2*\int_{f_L}^{f_H} S_{VG}\ df = \int_{f_L}^{f_H} \frac{(V_{GS}-V_{th})q\alpha_H}{C_{ox}f\ (IRN\_spec_{rms})^2} df \tag{5}$$

where f_H and f_L defines as the high and low frequency of the interested bandwidth, and IRN_spec_{rms} is the specification for the IRN.

Table I demonstrates the calculated size for different applications based on their own specifications by assuming the V_{GS}-V_{th} equal to 1V, which is a rough estimation for amplifier design. For ExG applications, since the input signal is very weak, it has a strict requirement for the noise specification, leading to very large sizes for the input transistor.

TABLE I. SPECIFICATIONS AND CALCULATED SIZES FOR DIFFERENT APPLICATIONS

Application	IRN spec(μVrms)	BW(Hz)	Calculated size(μm^2)
ECG	2	0.05 - 150	**~240k**
EEG	1	0.1 - 100	**~820k**
μECoG	1	1 - 500	**~740k**
Ultrasound patch	100	1M-10M	**~27.3**

Circuit design techniques such as chopping, auto-zeroing and correlated double sampling (CDS) can be used to reduce LFN instead of sizing the input pair.

Simulations based on UTSOI 2 model are also carried out depicted in Fig.8. The schematic of simulation circuit is shown in Fig.8(a). The load is infinite inductance to eliminate any noise contribution instead of input pairs', the supply voltage is 5V, and the overdrive voltage of the input transistor is 1V. Using the EEG specification as an example, to achieve an IRN of 1 μV_{rms}, the calculated size of the input transistor is around 0.82 mm^2, as indicated by Table I. In the simulation, the length of the transistor is fixed as 50µm while the W varies. The S_{VG} is shown in Fig. 8(b), where S_{VG} decreases by increasing the area, consistent with the trend predicted by (5). By integrating S_{VG} of the transistor with dimensions W=16mm and L = 50µm (corresponding to an area of 0.8 mm²) from 0.1Hz to 100Hz, the simulated IRN is 1.3µVrms, which is in good agreement with the value predicted by the Hooge's model. The slight discrepancy, with the simulation result being higher than the target value, is attributed to the calibrated UTSOI 2 model slightly overestimating the noise spectral density compared to the measurement data.

IV. CONCLUSION

An LFN characterization of sub-µm a-IGZO thin-film transistors (TFTs) has been conducted for the first time. The measured devices exhibit noise behavior consistent with the carrier mobility fluctuation model, with an extracted Hooge's parameter of ~ 2×10^{-3}. After calibrating the LFN parameters in the UTSOI 2 model, accurate noise simulations can be performed. Based on both theoretical calculations and simulation results, it is suggested that very large input transistors are required for low-noise biomedical signal readout applications. This finding highlights the necessity of employing advanced circuit design techniques, such as chopping and correlated double sampling (CDS), to further suppress noise in these systems.

ACKNOWLEDGMENT

Authors would like to thank Pragmatic Semiconductor for the samples (www.pragmaticsemi.com).

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