Exploring 2D TMD pFET gate stack scalability towards 1nm electrical thickness

T.D. Ngo[1*], Z. Lin[1], C.J. Dorow[2], X. Wu[1], R.K. Grubbs[1], D. Cott[1], K. Banerjee[1], I. Hoflijk[1], T. Conard[1], O. Richard[1], H. Han[1], F. Xi[1], A. Kozhakhmetov[2], K. Maxey[2], A. Oni[3], M. Metz[2], K.P. O'Brien[2], U. Avci[2], C.J. Lockhart de la Rosa[1], G. Sankar Kar[1], B. Govoreanu[1*]

[1]imec, Remisebosweg 1, B-3001 Leuven, Belgium, [2]Intel Foundry Technology Research & [3]Quality and Reliability Intel Corporation, Hillsboro, OR 97214, USA

*Contact: tien.dat.ngo@imec.be, bogdan.govoreanu@imec.be

***Abstract*— We report p-type compatible WO_x/HfO_2 gate stacks for WSe_2-based 2D pFET devices. 2D pFET compatible gate stacks are challenging as typical 2D gate stack processes often result in unintentional n-type doping. In this work, we preserve the p-type attributes of the channel through ALD precursor optimization, while employing interfacial layers to maintain the channel integrity. Dual-gate devices are fabricated with channel length down to 50nm and gate stacks achieving about 1.4 nm CET. We also present the first reported 2D pFET CV characteristics, including AC conductance analysis, showing successful CET scaling when thinning from 10 nm down to 4 nm HfO_2 physical thickness.**

Keywords—2D pFET, gate-stack, oxygen plasma, high-k ALD, CET scaling

I. Introduction

2D TMD channel materials are expected to extend the scalability of future technology nodes beyond Si, thanks to their atomically thin channel, enabling good electrostatic control, while not severely degrading mobility. Realization of a performant pFET device is a cornerstone in further advancing the 2D-channel materials technology. However, recent studies indicate that forming a p-type compatible gate stack requires a tailored approach, as gate stacks used in nFETs often include interfacial layers (ILs) that induce n-type doping, compromising p-type performance. In this work, we explore p-type compatible gate stacks, underlining the importance of high-k deposition process in the overall device performance, and propose a WO_x/HfO_2 gate stack that shows promise to meet (sub-)1nm CET requirements.

II. Processes, Results and Discussion

A. Device fabrication

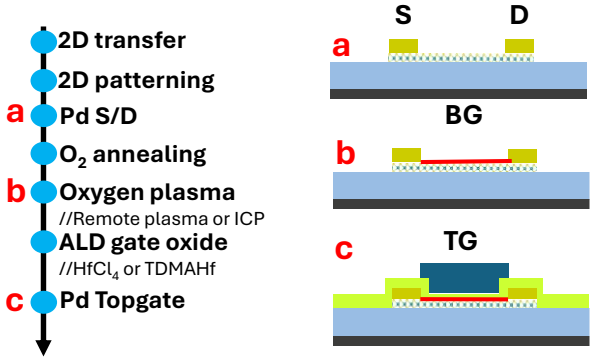

Fig. 1. Key process steps and schematic cross-sections for dual-gate 2D TMD pFET device fabrication. The labels a, b, c indicate intermediate and EOL testing points.

Fig.1 shows a schematics of a dual-gate (DG) device fabrication process flow. Unless otherwise specified, the channel material is multilayer (nML) WSe_2 directly grown on SiO_2 substrates using a 300 mm MOCVD process [1]. Prior to device fabrication, the 2D material was transferred onto a 12 nm ALD HfO_2 substrate deposited over a TiN back gate (BG). A 200 C O_2 anneal was performed after S/D contacts definition to reduce the contact resistance. An O_2 plasma was used to form a WO_x IL by sacrificial WSe_2 oxidation, followed by ALD HfO_2 deposition and top gate (TG) patterning.

B. Precursors impact

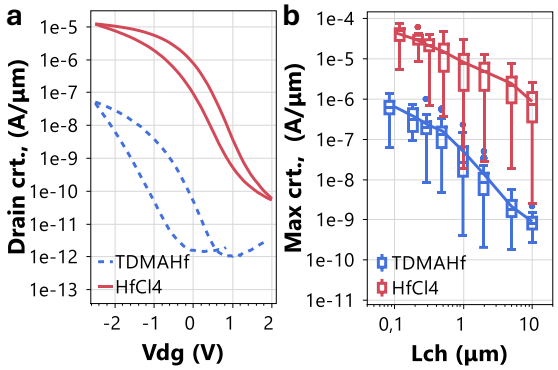

Fig. 2. (a) DG median IV characteristics for fully-processed DG devices (Fig. 1,c), with a plasma-formed WO_x IL and 10nm ALD HfO_2 deposited with 2 different processes, using TDMAHf and $HfCl_4$ precursors, respectively (L_{ch} = 1 µm). (b) Maximum current scaling with channel length (L_{ch}), evidencing a major impact of the ALD precursor. In DG operation mode, the BG and TG are connected together, $V_{bg} = V_{tg} = V_{dg}$.

Formation of WO_x IL by a plasma-based oxidation process on nML WSe_2 is essential to protect the WSe_2 channel, induce p-type doping, and promote ALD nucleation and growth [2]. Nevertheless, severe drive current reduction was observed, after high-k (HfO_2) deposition. To find the root cause, we used 2 different ALD processes to fabricate DG devices, with organic/inorganic precursors, i.e. TDMAHf and $HfCl_4$. IV characteristics (Fig.2) show a major difference, with around 2 orders of magnitude higher drive current and better hysteresis for $HfCl_4$-based HfO_2 and otherwise identical-process devices. This difference in current was maintained across the entire channel length range. We attribute this outcome to the chemistry of the ALD process, where the organic byproducts of the TDMAHf-based HfO_2 may interact with the WO_x IL, resulting in W with a lower oxidation state, and compromise the quality of the IL and/or the WO_x/HfO_2 inner interface.. This is suggested by the hard-XPS (HAXPES) W3d spectra, where a slightly larger shift of the W-O peak to lower binding energies was observed for the TDMAHf case compared to the $HfCl_4$ (Fig.3). Degradation of the WO_x IL is also seen in SS data, which have higher values for the TDMAHf case (not shown). Separate experiments, performed on monolayer (ML) WSe_2, where the WSe_2 material was exposed to the HfO_2 deposition

process directly (without any WO_x IL) (Fig.4) showed that while the $HfCl_4$ process degrades the channel, the TDMAHf process induced n-type doping, suppressing the p-type branch. This is consistent with chemical action on WSe_2 by HCl byproduct ($HfCl_4$ process), while dimethylamine ($HN(CH_3)_2$) byproduct adsorbs into and functionalizes WSe_2 (TDMAHf process), respectively. Hence, when present, the WO_x IL acts as a protective layer, which can only withstand the $HfCl_4$-based ALD process.

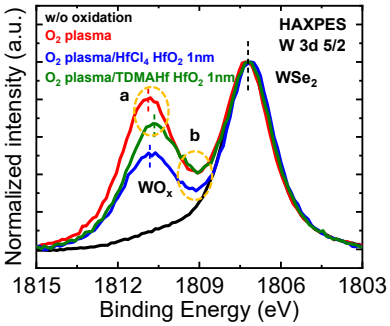

Fig. 3. W3d HAXPES spectra with plasma surface treatment and different ALD processes on multilayer (nML) WSe_2. The decrease of the $HfCl_4$-based W-O peak is attributed to a limited removal of WO_x during the ALD process, while features **a** and **b** suggest an increased fraction of W suboxides formation for the TDMAHf-based ALD process. A 1nm-only ALD HfO_2 has been employed to form the WO_x/HfO_2 interface on blanket samples to allow HAXPES probing resolution.

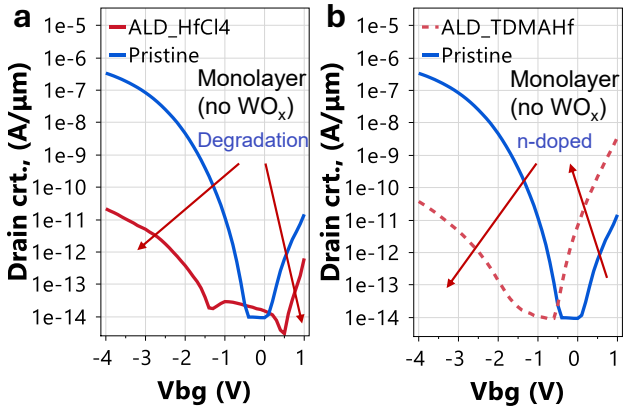

Fig. 4. I_dV_g curves of **monolayer** WSe_2 devices and **without** WO_x IL evidence the direct impact of the as-deposited HfO_2: the $HfCl_4$-precursor induces a degradation of the current level, while TDMAHf precursor induces an n-type doping, commonly observed with other dielectrics, e.g. AlO_x or Si-seed (SiO_x).

C. *Plasma impact*

O_2 plasma treatment forms the WOx IL by WSe_2 oxidation. A direct plasma leads to a stronger p-type doping, resulting in large current increase and V_t-shift, limiting the on/off ratio (I_{max}/I_{min}) of the device. A remote O_2 plasma process produces a soft doping, mainly resulting in V_t-shift (Fig.5, for test point "b" in Fig. 1). Forming the TG with ALD HfO_2 (test point "c", Fig.1) results in good TG control, able to counteract the channel doping and turn off the devices, while retaining the advantage of higher drive current achieved with direct O_2 plasma treatment (Fig.6). When operated in the DG mode (BG and TG tied together), I_{max}/I_{min} ratio for the samples that received a direct plasma WO_x IL exceeds 7 decades.

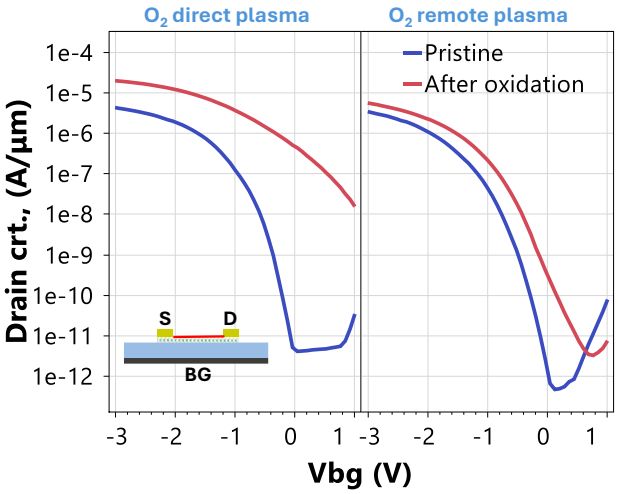

Fig. 5. WO_x ILs produced by O_2 plasma oxidation, induce p-type doping, in contrast with HfO_2 (Fig.4) or other ILs. A strong doping is achieved with an direct O_2 plasma, leading to a noticeable increase of the drive current and a V_t-shift. A soft doping is achieved with a remote O_2 plasma, resulting mainly in a V_t-shift. Data show median IV curves, for devices of L_{ch} = 2 μm.

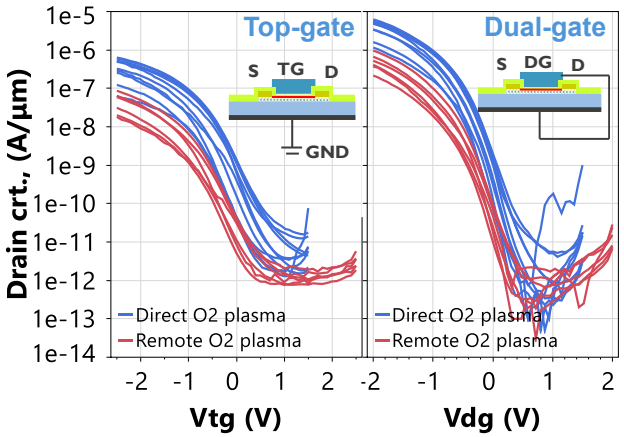

Fig. 6. (Top) gate stacks formed with $HfCl_4$-based HfO_2, for both plasma treatments, show very good TG control, which can turn off the direct plasma-treated devices, while retaining the advantage of a higher drive current (left plot). Operating the devices in DG mode (TG and BG shorted) further improves the channel modulation, increasing I_{max}/I_{min} ratio to over 7 orders of magnitude (right plot). (L_{ch} = 2 μm)

D. *Gate stack scaling*

We adopted an direct O_2 plasma treatment and a $HfCl_4$-based HfO_2 process to explore gate scalability. We fabricated devices with HfO_2 thickness down to 3 nm (Fig.7). HR-TEM cross-sections through 50 nm channel devices show well formed, uniform gate stacks for both 4nm and 3nm HfO_2, and nML WSe_2 channel. Line profiles of EDS maps on a 3 nm-HfO_2 device evidence presence of the WO_x IL, by shifts of W profile relative to Se, and that of O relative to Hf. Very good electrostatic control of both TG and BG is shown, down to 3 nm HfO_2 layer (Fig.8).

Gate dielectric thickness scaling shows improved modulation of the drain current (I_d), at similar bias, and for the same ΔV_{tg} swing.

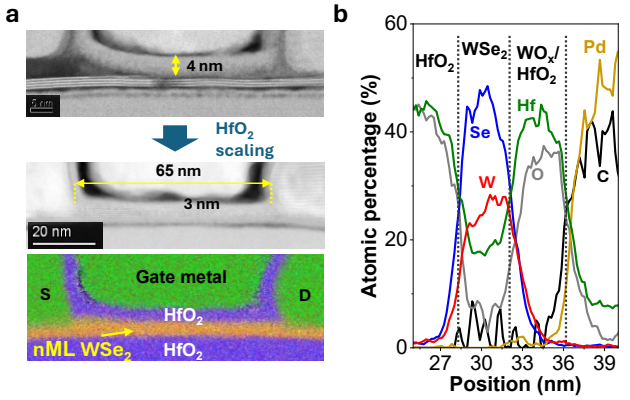

Fig. 7. (a) TEM cross-sections and elemental map of fabricated DG devices of L_{ch}=50nm, featuring a WO_x/HfO_2 gate stack with 4nm (top) and 3nm (bottom)_$HfCl_4$-based HfO_2. The WSe_2 channel consists of several (4-8) monolayers (nML). (b) Integrated line scans, evidencing existence of a thin WO_x IL between the channel and HfO_2 dielectric.

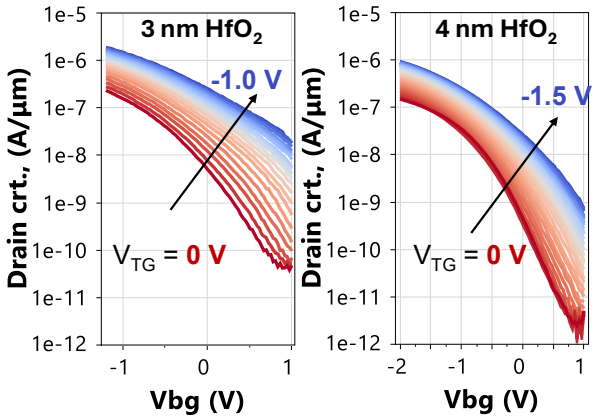

Fig. 8. IV transfer curves of back-gated devices with WO_x/HfO_2 gate stacks, at various TG biases. Very good control is achieved, even for the thinnest TG stack (3nm HfO_2). Devices have L_{ch} = 5 µm.

Dual-sweep IV plots show that the hysteresis is small (Fig.9), with an extracted $|\Delta V/V_{dg,max}| < 60$ mV/V. I_{max} exceeds 100 µA/µm, with the best performing devices showing a maximum current of up to ~170 µA/µm, for 4 nm HfO_2 thickness. I_{max}-L_{ch} plots (Fig.10) show that the contact resistance limits the actual device performance; contact optimization would project current levels well over 500 µA/µm at below 50 nm channel length, if contact resistance is reduced sufficiently.

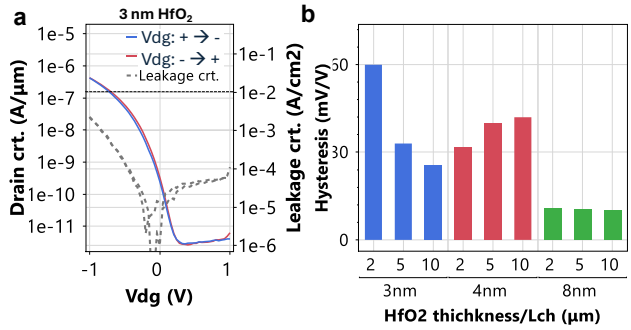

Fig. 9. (a) Double-sweep IV's for $HfCl_4$-based WO_x/3nm HfO_2 gate stacks, measured on large area DG devices, evidencing very small hysteresis and low leakage current, with margin for further HfO_2 thickness scaling (DG operation, L_{ch}=10µm, W_{ch}=5µm). (b) Median hysteresis $|\Delta V/V_{dg,max}|$ extracted at a current level I_d=10^{-9}A/µm for several $HfCl_4$-based WO_x/HfO_2 TG stacks show values below 60mV/V.

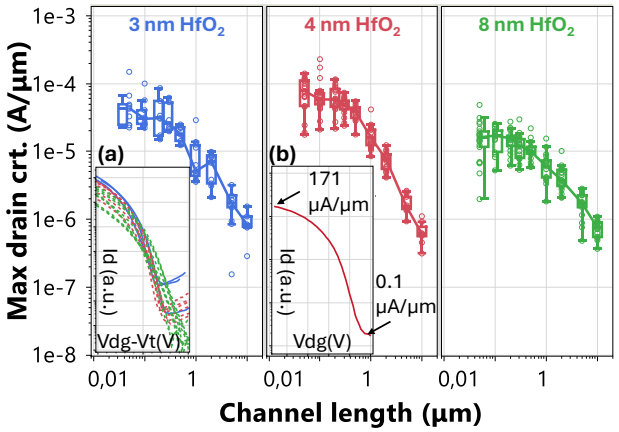

Fig. 10. Maximum current scaling with L_{ch}, indicating contact-limited conduction for devices below 1µm channel length. This hinders observation of higher currents for short channel devices. Contact optimization may enable currents of hundreds µA/µm, at below 50nm-channels, as inferred from an ideal I_{max}-L_{ch} scaling trend. The apparent drop of I_{max} at 3nm HfO_2 is mainly due to lower overdrive (V_{dg}-V_t) sweep range (corrected for in the inset a). The inset b shows an IV selected from best performing devices with 4nm HfO_2 thickness (L_{ch} = 100nm).

TABLE I. I_{dmax}, hysteresis and CET benchmarking of 2D pFET DG devices with grown-TG stack showing best-in-class I_{dmax}, hysteresis and electrical thickness. Our work is summarized in the first 3 table lines.

Gate stack	I_{dmax} (µA/µm)	Hysteresis (mV/V)	t_{HfO2} (nm)	EOT_{TG} (nm)
WO_x (Direct) + $HfCl_4$ HfO_2	171	30	4	1.7
WO_x (Remote) + $HfCl_4$ HfO_2	112	88	3	n/a
WO_x (Direct) + TDMAHf HfO_2	1.23	240	10	2.8
Ref. [3] – HfO_2	123	n/a	12	n/a
Ref. [4] – HfO_2	2	n/a	10	n/a
Ref. [5] – HfO_2	~10	n/a	~10	n/a
Ref. [6] – HfO_2	132	n/a	n/a	n/a

Multi-frequency CV data showed well-behaved capacitances, as measured for BG-only, as well as for DG configurations on large area devices (Fig.11). TG capacitance was extracted by subtracting BG capacitance from DG capacitance, correcting for parasitic (e.g. pads) components. A CV tool was then used to extract TG electrical thickness (CET), by fitting experimental CV curves in the accumulation region. Extracted values for 10 nm down to 4 nm HfO_2 gate stacks were used to extract the HfO_2 dielectric constant (16) and extrapolated to an WO_x IL CET of 0.7 nm (Fig. 12). Projected CET of 3 nm HfO_2 gate stack yielded a value of about 1.4 nm.

Frequency-scaled (G_p/ω) conductance plots on structures with 10 nm HfO_2 gate stacks were taken for devices processed with both HfO_2 precursors (Fig. 13) and showed an important contribution of the interface traps, of similar magnitude (expected, given the similar WO_x interface), but manifesting at different biases, consistent with the IV curves (Fig.2). We estimated a D_{it} density in the order of (5-6)·10^{12}/cm^2.eV, which leaves room for further improvement.

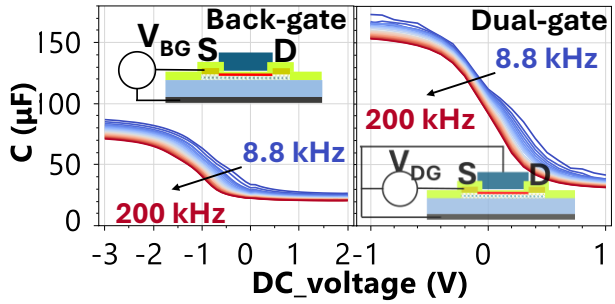

Fig. 11. Multi-frequency CV curves obtained on BG and DG large area ($5.76 \cdot 10^{-5} cm^2$) devices with $HfCl_4$-based WO_x/4nm HfO_2 TG stacks. Pad-free TG capacitance is extracted as explained in the text.

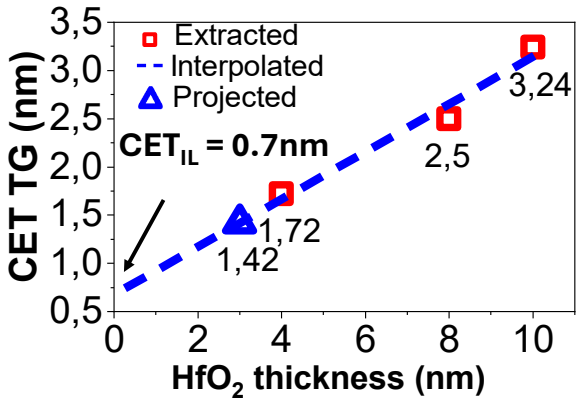

Fig. 12. CET plot, based on extracted CET values for 4nm, 8nm and 10nm $HfCl_4$-based HfO_2 gate stacks, extrapolates to an WO_x IL of ~0.7nm EOT. A CET of ~1.4nm for WO_x/3nm HfO_2 TG stacks is projected by the linear fitting curve (direct CET extraction is hindered by the leakage of the large area devices used).

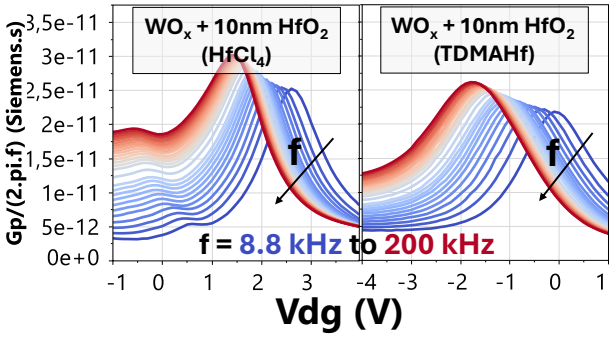

Fig. 13. Multi-frequency G_p/ω curves for $HfCl_4$ and TDMAHf-based gate stacks, evidencing interface traps most active at biases around their respective V_{FB}'s, consistent with the IVs in Fig.2. The peaks of the curves were used to extract the interface trap density (D_{it}).

III. Conclusion

We demonstrated p-type tailored WO_x/HfO_2 gate stacks by optimizing the formation of an WO_x IL and by utilizing a suitable ALD process chemistry to preserve good pFET device performance. While the WO_x IL can be optimized to improve the p-type benefits, it is also essential to protect the WSe_2 channel from secondary processes that can be induced during the ALD. Besides that, it provides an alternative method to produce an interface, which avoids using slow physisorption processes, commonly employed to enhance high-k nucleation/growth on 2D surfaces, but pose a manufacturability challenge.

Gate stack scalability was explored by IV & CV analysis, showing controllable gate stacks down to at least 3 nm HfO_2 thickness. Further scalability may be achieved by optimizing the IL formation, while performance can significantly benefit from S/D contact engineering, currently limiting short-channel device performance.

Acknowledgments

This work has been partly performed within imec's core CMOS industrial affiliation program (IIAP) on Exploratory Logic devices.

References

[1] C.J. Dorow, "Exploring manufacturability of novel 2D channel materials: 300 mm wafer-scale 2D NMOS & PMOS using MoS2, WS2, & WSe2," 2023 International Electron Devices Meeting (IEDM), 2023, pp. 1-4.

[2] T.D. Ngo, "The Critical Role of 2D TMD Interfacial Layers for pFET Performance," 2024 IEEE International Electron Devices Meeting (IEDM), 2024, pp. 1-4.

[3] X. Xiong, "Top-Gate CVD WSe2 pFETs with Record-High Id~594 µA/µm, Gm~244 µS/µm and WSe2/MoS2 CFET based Half-adder Circuit Using Monolithic 3D Integration," 2022 International Electron Devices Meeting (IEDM), 2022, pp. 20.6.1-20.6.4.

[4] C. Cheng, "First demonstration of 40-nm channel length top-gate WS2 pFET using channel area-selective CVD growth directly on SiOx/Si substrate," 2019 Symposium on VLSI Technology, 2019, pp. T244-T245.

[5] T.Y.T.Hung, "pMOSFET with CVD-grown 2D semiconductor channel enabled by ultra-thin and fab-compatible spacer doping," 2022 International Electron Devices Meeting (IEDM), 2022, pp. 7.3.1-7.3.4.

[6] W. Mortelmans "Gate Oxide Module Development for Scaled GAA 2D FETs Enabling SS<75mV/d and Record Idmax>900µA/µm at Lg<50nm," 2024 IEEE International Electron Devices Meeting (IEDM), 2024, pp. 1-4.