A 28nm 8-Bit 32-GS/s DAC Achieving > 55dBc/> 40dBc SFDR up to 5.2GHz/13.6GHz Using 4-Channel NRZ Time-Interleaving with Background Calibration for Direct Digital Signal Synthesis

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***Abstract*—This work presents an 8-bit 32-GS/s 4-channel non-return-to-zero (NRZ) time-interleaving (TI) digital-to-analog converter (DAC) fabricated in a 28nm CMOS process. This DAC is the first to achieve a sampling rate of over 16 GS/s using an NRZ TI structure. The proposed DAC employs background calibration to ensure the clock timing alignment of the four channels, which significantly improves the DAC dynamic performance. The measurement results demonstrate a 55dBc spurious-free dynamic range (SFDR) at 5.2GHz and a 40dBc SFDR at 13.6GHz. The total power consumption is 692mW when the DAC operates at 32-GS/s sampling rate (FS) under a mixed 1.8V/1.2V/1.0V supply. The proposed DAC provides superior bandwidth and precision for direct digital signal synthesis (DDS), especially at high frequencies.**

Keywords—Digital-to-analog converter (DAC), time-interleaving (TI), non-return-to-zero (NRZ), background calibration, direct digital signal synthesis (DDS).

I. Introduction

As an essential component of electronic devices, direct digital signal synthesis (DDS) has a strong demand for high-linearity digital-to-analog signal conversion at high frequencies. Fig. 1 shows three different existing digital-to-analog converter (DAC) structures to obtain gigahertz signals. The mixing DACs are widely utilized to generate analog signals in the second Nyquist zone [1]. However, mixing DACs require a clock with high frequency and a high-performance bandpass filter, which introduces extra design complexity and overall system cost.

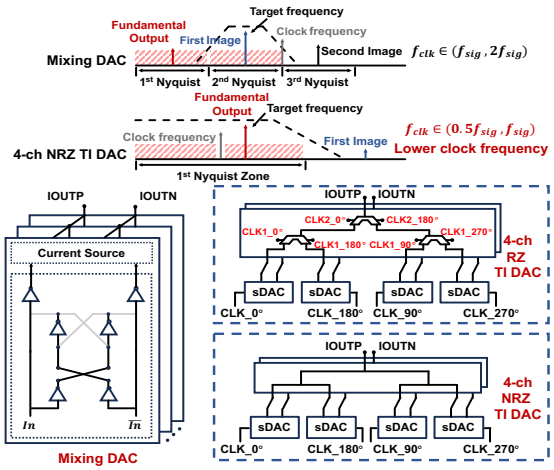


Fig. 1. Comparison of different DAC architectures for generating analog signals with GHz frequencies.

Compared with the mixing DACs, the time-interleaving (TI) DACs in Fig. 1 enable the parallel operation of multiple sub-DACs and combine their outputs, thus increasing the sampling rate by several times, equal to the number of channels. The TI structures prevent the use of ultra-high-frequency clocks and ultra-high-speed single-channel DACs. Furthermore, TI DACs push the first image far away, which reduces the system design complexity considering the filters. Therefore, TI DACs have significant advantages in generating analog signals with high frequencies, in particular, beyond the single-channel capability.

As a recent advance, the non-return-to-zero (NRZ) TI structure has been proposed as an efficient approach for an ultra-high sampling rate. The NRZ structure highlights the greatly simplified interleaving structure by summing the outputs of sub-DACs directly. A recent 28nm 8-bit 4-channel NRZ TI 16-GS/s DAC has achieved a spurious-free dynamic range (SFDR) above 61dBc up to 2.3GHz using four 4-GS/s sub-DACs [2]. Fig. 2 summarizes the state-of-the-art TI DACs [2]-[7], [10], [12]. The proposed DAC is the first reported NRZ 4-channel TI DAC that achieves a sampling frequency over 16GS/s, and also the first >20GS/s DAC chip with a silicon verified SFDR above 55dBc at 5.2GHz.

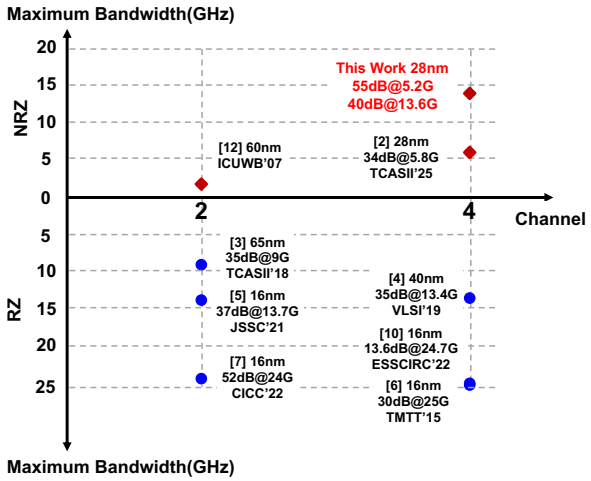


Fig. 2. Summary of the recent trend of the state-of-the-art TI DAC architectures.

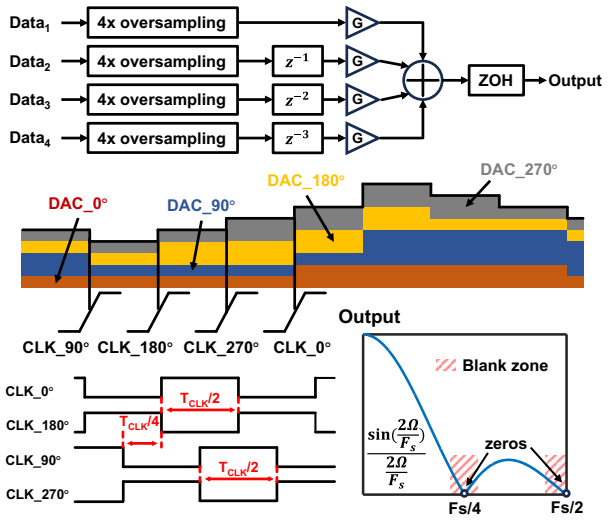


Fig. 3. Principle and implementation of 4-channel NRZ structure.

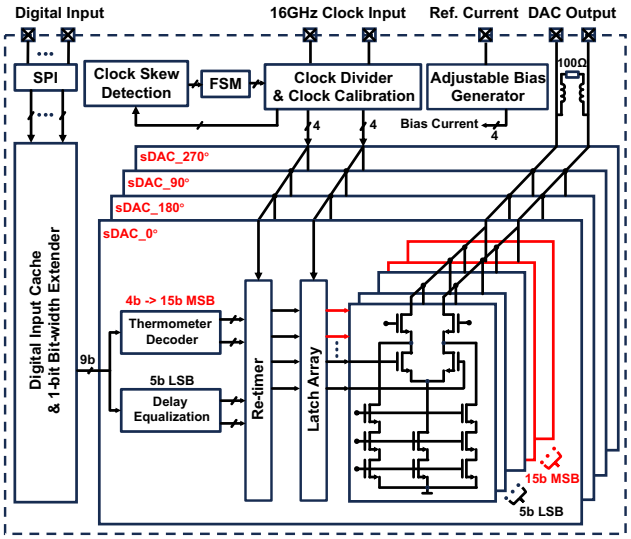


Fig. 4. Top architecture of the DAC core.

This paper presents a 32-GS/s 8-bit DAC in 28nm CMOS using a 4-channel NRZ TI structure. Different from [2], this work incorporates a custom background clock calibration and overcomes the timing misalignments between channels. Experimental results show an SFDR over 55dBc at 5.2GHz and 40dBc at 13.6GHz, providing superior bandwidth and dynamic performance for DDS.

II. Top Architecture

The proposed DAC employs an NRZ TI structure, which sums the outputs of four channels directly through a current tree to generate the final output. Fig. 1 presents the structure of the NRZ DAC. Compared with the conventional return-to-zero (RZ) TI structure [7], an NRZ structure avoids the use of output analog MUXs and additional controlling clocks. This greatly simplifies the design of the current source array and clock calibration circuit [4]. Fig. 3 illustrates the principle of the 4-channel NRZ structure. Controlled by a set of orthogonal clocks, the 4-channel sub-DACs operate in parallel and update the output on the corresponding clock's rising edge. The images near

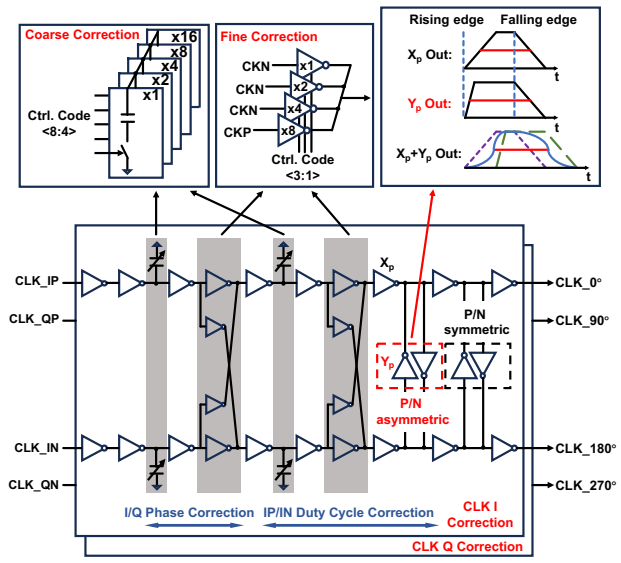


Fig. 5. Design of the proposed clock calibration circuit.

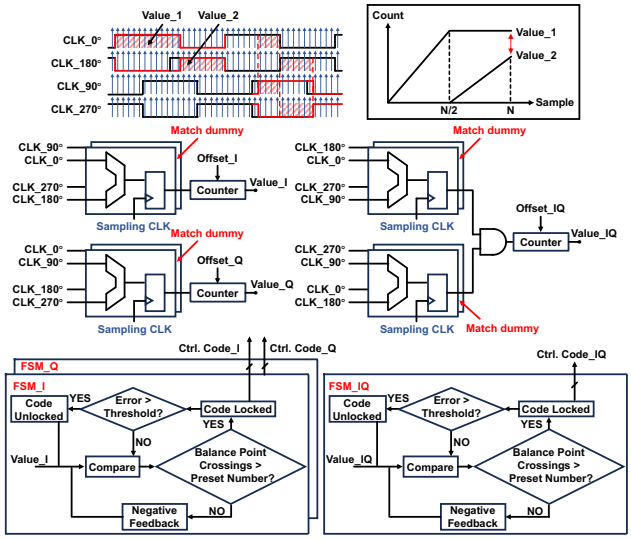
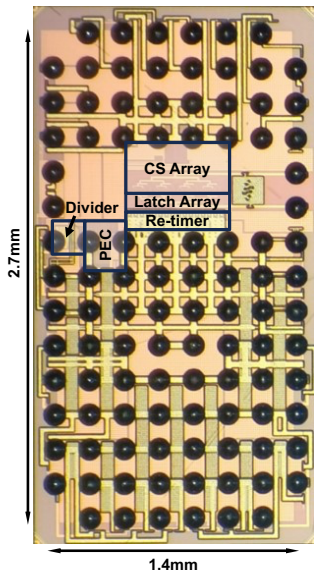
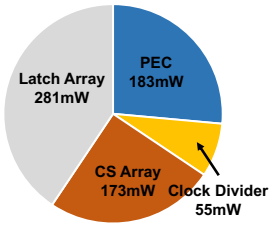


Fig. 6. Design of the phase misalignment detection circuit.

Fs/4, Fs/2 and 3Fs/4 are canceled out during the summation process, leading to a four times effective sampling rate [8]. Meanwhile, the cancellation of the images introduces zeros at the image frequencies, leaving blank zones in the frequencies around Fs/4 and Fs/2 in the first Nyquist zone. Fortunately, this issue can be solved by adjusting Fs based on the target frequency band.

Fig. 4 presents the top architecture of the proposed DAC. The proposed DAC contains four sub-DACs, each with an 8-GS/s sampling rate and a 9-bit resolution. The extra redundant bit employed in each channel enhances the swing range of sub-DACs, thereby reducing the impact of blank zones [2]. The segmentation of the sub-DAC current source array follows 4-bit MSBs and 5-bit LSBs. A background calibration circuit is employed to ensure the accuracy of the orthogonal clocks. A set of 16 GHz differential clocks, after division and calibration, are used to drive each sub-DAC. To precisely match the current weights, a regulation module integrated into the biasing circuit adjusts the bias current of each sub-DAC. The output is





Technology	28nm
Resolution	8 bits
Sample Rate	32GS/s
Supply	1.8V/1.2V/1V
Full Scale	400mV
Power	692mW
Core Area	0.15mm^2
SFDR@5.2GHz	55.69dBc
SFDR@13.6GHz	40.23dBc

Fig. 7. Chip micrograph and performance summary.

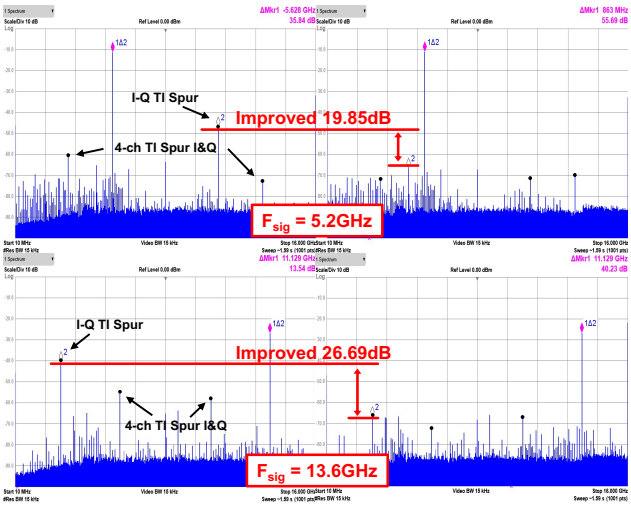


Fig. 8. SFDR measurements of signals with frequencies of 5.2/13.6GHz before and after calibration at a sampling frequency of 32GS/s.

connected to a coupled inductor to reduce signal amplitude attenuation at high frequencies. The differential full-scale output swing is 400mV.

III. Circuit Design

The proposed DAC employs background clock calibration to alleviate the misalignments between the controlling clocks of the sub-DACs, thereby improving dynamic performance. Fig. 5 illustrates the implementation of phase error correction (PEC) of the calibration circuit. The configurable capacitor array is utilized for coarse correction. A clock delay with an accuracy of approximately 90fs and a range of ±5ps can be achieved by adjusting the size of the capacitor array. Fine delay correction with a resolution of approximately 15 fs is achieved by changing the strength of the counteracting inverters.

The duty cycle of the I/Q differential clocks is not adjusted directly. Instead, a set of P/N asymmetric cross-coupled inverters is introduced into the clock distribution inverter chain

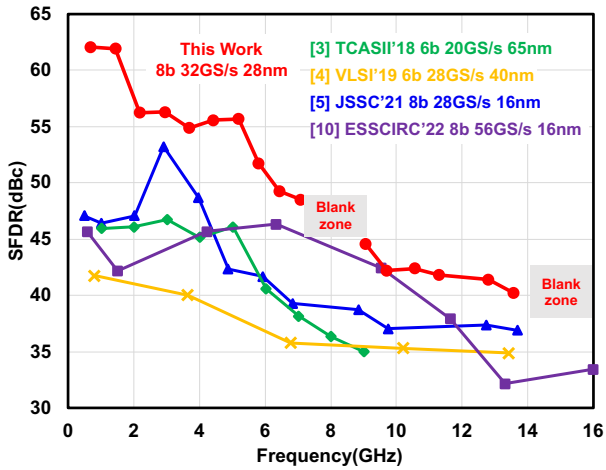


Fig. 9. Comparison of SFDR with state-of-the-art DACs.

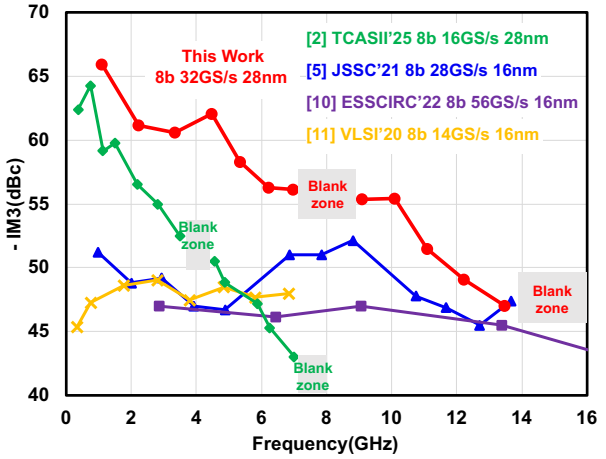


Fig. 10. Comparison of IM3 with state-of-the-art DACs.

to convert the delay between the I/Q differential clocks into duty cycle adjustment. As shown in Fig. 5, during the duty cycle calibration process, the adjustment of the delay between the differential clocks changes the duration of the asymmetric inverters' effect on the edges of the differential clocks, thereby altering the duty cycle of the differential clocks. The duty cycle adjustment range is from 46% to 54% when the proposed DAC operates at a 32-GS/s sampling rate.

An algorithm based on sampling is used for detecting clock phase misalignments, as shown in Fig. 6. A dedicated clock samples the orthogonal clocks. The count values of the high-level samples are then sent to a finite state machine (FSM), which applies preset offsets to compensate for distribution skew. The sampling clock is independent of the orthogonal clocks. Therefore, the samples can be considered approximately uniformly distributed given a sufficiently long period of time. The count value of level '1' samples represents the proportion of time the clock remains high during the cycle. Moreover, dummy elements are used in the sampling module to match the loads of orthogonal clocks. During the calibration process, the FSM compares the count values and applies negative feedback to correct timing misalignments. The control codes are locked temporarily by FSM when the comparison of the sample results

TABLE I. COMPARISON WITH STATE-OF-THE-ART DACS

	This work	VLSI'19 [4]	JSSC'21 [5]	CICC'22 [7]	ESSCIRC'22 [10]	JSSC'21 [13]
Architecture	**Current Steering 4-ch NRZ TI**	Current Steering 4-ch RZ TI	Current Steering 2-ch RZ TI	Current Steering 2-ch RZ TI	Current Steering 4-ch RZ TI	Capacitive
CMOS (nm)	**28**	40	16	16	16	16
Sampling Rate (GS/s)	**32**	28	28	50	56	16
Resolution (bit)	**8**	6	8	9	8	12
Supply Voltage (V)	**1.8/1.2/1**	1.1/1.6	0.8	1/0.8	0.85	1.2
Swing ($mV_{pp\text{-}diff}$)	**400**	200	320	400	270	873
Core Area (mm^2)	**0.15**	0.045	0.03	0.2	0.011	0.072
Power (mW)	**692**	103	88	243	280	530
SFDR (dBc)	**40.2@13.6GHz**	34.6@13.3GHz	37.0@13.7GHz	52.0@24.0GHz	32.1@13.3GHz	65.0@5.2GHz
IM3 (dBc)	**-47.0@13.6GHz**	N/A	-47.4@13.7GHz	N/A	-45.6@13.3GHz	-72.0@5.2GHz

oscillates around the balance point [9]. It is worth noting that the sampling and comparison of the orthogonal clocks are sustained, and calibration will proceed when the differences in count values exceed the preset thresholds.

IV. MEASUREMENT RESULTS

Fig. 7 presents the photomicrograph and performance a summary of the DAC. The proposed DAC was fabricated using a 28nm CMOS process. The core area of the chip is 0.15mm^2. The power consumption of the DAC core is 692mW when it operates at a 32-GS/s sampling rate, with approximately a quarter of power consumption attributed to the background calibration circuit.

The DAC output spectra before and after calibration are shown in Fig. 8. The measurement results confirm that the background calibration circuit effectively cancels the misalignments between the orthogonal clocks. Thanks to the background calibration, SFDR achieves an improvement of 19.9dB and reaches 55.6dBc at 5.2GHz. At high frequencies, the calibration brings a 26.7dB enhancement in SFDR and achieves a 40.2dBc SFDR at 13.6GHz. Fig. 9 plots the measurement results of SFDR and compares them with the state-of-the-art DACs with similar structures, sampling rates and resolutions [3]-[5], [10]. Fig. 10 shows the IM3 measurement results [2], [5], [10]-[11]. The proposed DAC exhibits a significant advantage over state-of-the-art DACs up to 14 GHz. Table I summarizes these performance and compares them with the state-of-the-art DACs.

V. CONCLUSION

This work presents an 8-bit 32GS/s 4-channel NRZ TI DAC with background clock calibration. The NRZ TI structure enables the proposed DAC to achieve a high sampling rate without high frequency clocks and reduces the design complexity. With a background algorithm based on sampling and an innovative adjustment circuit, the calibration circuit eliminates the misalignments between the orthogonal clocks and achieves a relatively accurate clock phase. The proposed DAC achieves a SFDR of 55.6dBc at 5.2GHz and 40.2dBc at 13.6GHz, with a significant advantage compared to state of the art DACs. The proposed DAC enables DDS to operate at higher frequencies and achieve better dynamic performance.

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