# A Single-Channel 12-Bit 2GS/s 1.7GHz-ERBW Aperture-Error-Free Pipelined ADC with Flash-Embedded MDAC


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*Abstract*—This paper proposes a flash-embedded MDAC that eliminates the aperture error between the flash quantizer and MDAC in SHA-less pipelined ADCs, enabling high ERBW at a high sampling rate. Additionally, the first-stage flash ADC reuses the switched-capacitor circuit in MDAC to generate accurate quantization threshold voltages with low power consumption. These techniques are demonstrated in a 12-bit 2GS/s single-channel pipelined ADC, achieving an ERBW of 1.7GHz. At the Nyquist input frequency, the measured SNDR and SFDR are 58.3dB and 73.4dB, respectively. Consuming 23.26mW from a 1V supply, the ADC achieves a FoMs of 168.4dB and a FoMw of 17.3fJ/conv.-step, respectively.



*Keywords*—pipelined ADC, wide ERBW ADC, aperture error elimination, threshold generation circuit


## I. Introduction

In software-defined radio (SDR) receivers, ADCs are desired to have GHz sampling rates, 12~14-bit resolution, and most importantly, high input bandwidth. While pipelined ADCs can achieve both high sampling rates and high resolution, maintaining a wide input bandwidth presents a significant design challenge.

A front-end sample-and-hold amplifier (SHA) is commonly employed in conventional pipelined ADCs to convert the first-stage input into a DC signal, thereby achieving high effective resolution bandwidth (ERBW) [1], [2], as shown in Fig. 1(a). However, implementing a high-linearity, low-noise SHA introduces significant power and area overhead. To improve efficiency, SHA-less pipelined ADCs remove the SHA and sample the input signal directly to the MDAC and flash quantizer. However, this approach induces sampling aperture error that significantly degrades performance for wideband inputs.

The prior art of [3] mitigates the aperture error by combining the MDAC and flash sampling capacitor, as shown in Fig. 1(b). After sampling, an extra hold phase ($\Phi_H$) is introduced to transfer the sampled MDAC voltage to the flash quantizer, such that the flash quantizer sees the exact sampled voltage, and thus aperture error is eliminated. However, the parasitic capacitance on the MDAC top plate introduces a gain error between the MDAC and the flash ADC, making it difficult to generate accurate multi-bit flash thresholds. It limits the resolution to 1.5-bit per stage, resulting in more pipelined stages and higher power consumption.

Generating quantization threshold voltages ($V_{QTH}$s) for the multi-bit flash is another challenge in pipelined ADCs. Typically, $V_{QTH}$s are generated by a resistor ladder, where the number of resistors increases exponentially with resolution. Furthermore, the RDAC's switches are hard to keep on for $V_{QTH}$s near $V_{ref}/2$.

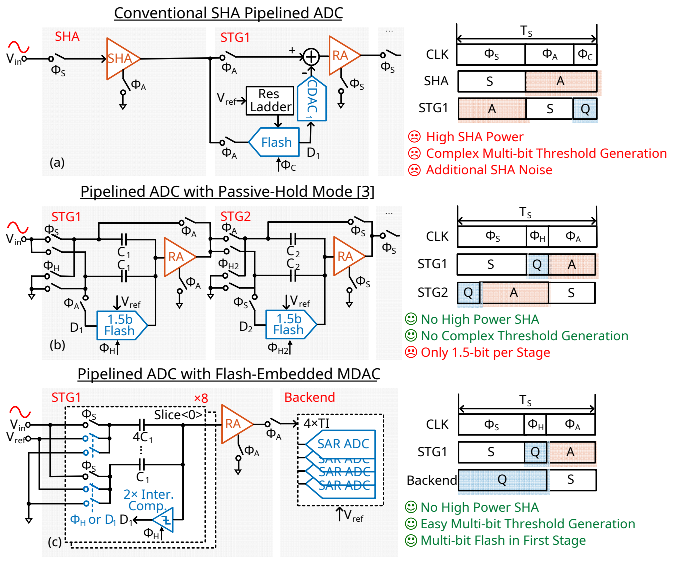


Fig. 1 (a)Conventional SHA pipelined ADC; (b)Pipelined ADC with passive holding mode [3]; (c)Proposed pipelined ADC with flash-embedded MDAC.

To overcome the two above-mentioned challenges in pipelined ADCs, this work proposes a flash-embedded-MDAC structure, as shown in Fig. 1(c). Different from [3], this approach reuses the MDAC for both the flash quantizer's sampling and $V_{QTH}$s generation, therefore a high-resolution flash quantizer can be deployed within the same hold phase. This approach eliminates aperture error while enabling multi-bit flash ADC with simplified $V_{QTH}$s generation circuits. Additionally, the multi-bit first stage not only effectively reduces the number of pipeline stages, but also relaxes the linearity requirement of the residue amplifier. Furthermore, a low-power TI-SAR ADC backend improves power efficiency [4].

With the proposed techniques, a prototype 12-bit 2GS/s single-channel pipelined ADC is implemented, achieving a high ERBW of 1.7GHz. At Nyquist frequency, the measured SNDR and SFDR are 58.3dB and 73.4dB, resulting in a FoMs of 168.4dB and a FoMw of 17.3fJ/conv.-step, respectively.

## II. ADC Implementation and Circuit-Level Design

### A. Flash-Embedded-MDAC Based ADC Architecture

Fig. 2(a) illustrates the block diagram of the proposed pipelined ADC with flash-embedded MDAC. The 4-bit first stage includes eight slices (Slice<0:7>), and each slice consists of a 3-bit CDAC and a 2× interpolated flash quantizer [5]. In the sampling phase, all eight Slice<0:7> sample the input signal simultaneously. In the following settling phase, the three MSBs of CDAC in eight slices are set with different preset codes, from 000 to 111, respectively.

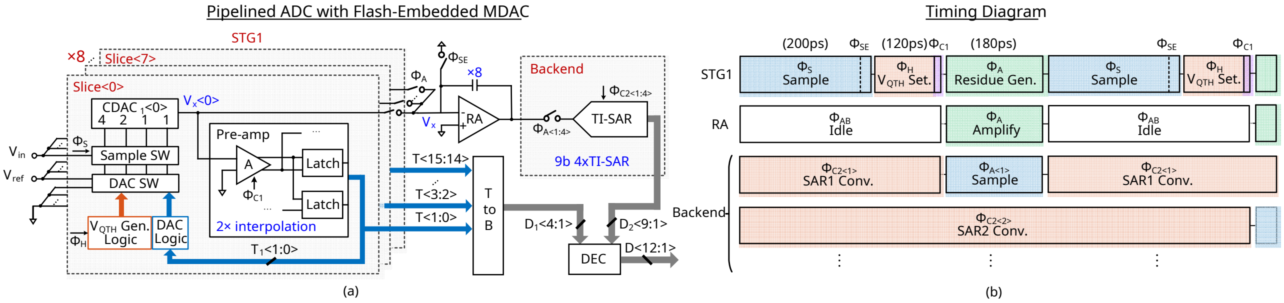


Fig. 2 Block and timing diagram of the proposed ADC.

Thereby, the embedded flash quantizers can resolve the MSBs by judging the CDAC's top plate voltages. After flash quantization, the eight CDACs are re-settled by the resolved MSBs and combined to generate the residue. By merging the MDAC and flash quantizer, aperture error during sampling is eliminated, and the ADC can accept over Nyquist input frequencies without backend saturation. The backend stage consists of 4× time-interleaved 9-bit, 500MS/s SAR ADCs. The total single-ended sampling capacitor of STG1 is 400fF, while that of the single-channel backend SAR ADC is 57fF. The residue amplifier employs a closed-loop OTA for 8× amplification.

Fig. 2(b) illustrates the timing diagram of the flash-embedded-MDAC pipelined ADC. The 200ps sampling phase ($\Phi_S$) controls the sampling of the eight flash slices. Following that, a 120ps $V_{QTH}$ settling phase ($\Phi_H$) activates the $V_{QTH}$ generation logic, connecting the bottom plates of the 3MSBs in CDAC $_1$<i> to generate V $_{QTH}$<i> for the flash quantizer. At the end of $\Phi$ $_H$, a short comparison phase ($\Phi$ $_{C1}$) triggers the 2× interpolated flash comparators in each slice, producing conversion results T<i+1:i>. The resolved MSBs instantly drive the CDACs, generating a subtraction between $V_{in}$ and T<i+1:i> on the top plates V $_x$<i>. After that, the top plates $V_x$<0:7> are all connected to the residue amplifier (RA) to perform amplification during the 180ps $\Phi_A$. Meanwhile, the 4× TI-SAR ADCs sample sequentially under the control of $\Phi_A$<1:4> and resolve the LSBs.

B. Threshold Voltage Self-Generation with Reused CDAC

The proposed multi-bit flash threshold generation method reuses the MDAC to generate the required V $_{QTH}$<i> for each slice. Fig. 3 illustrates an operation example for Slice<4>. The unit capacitance C $_u$ is 6.25fF, and the capacitor array is weighted in 4-2-1-1. During the sampling phase $\Phi$ $_S$, the top

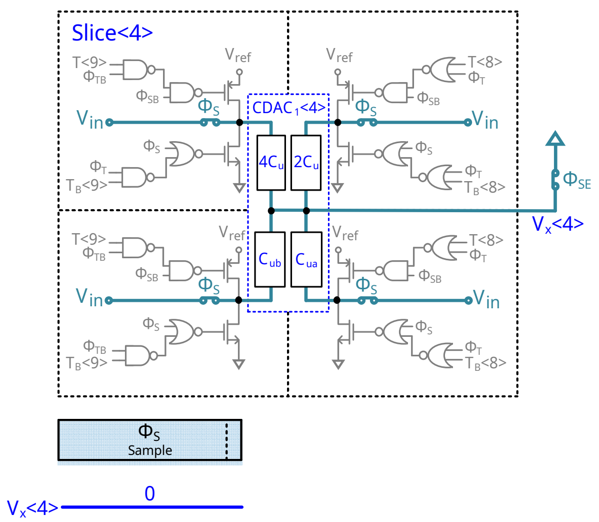


Fig. 3 Slice<4> in the sampling phase.

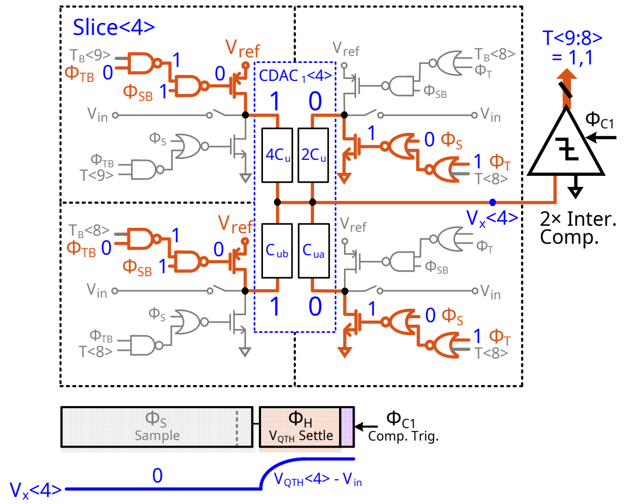


Fig. 4 Slice<4> in the $V_{QTH}$ settling phase.

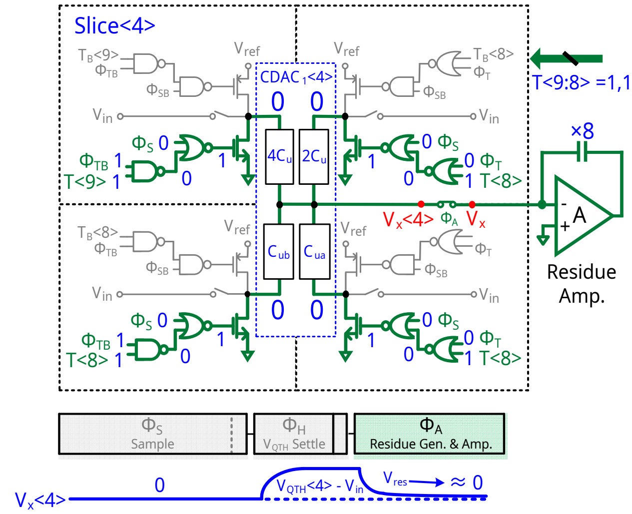


Fig. 5 Slice<4> in the residue generation and amplification phase.

plate of $CDAC_1$<4> ($V_x$<4>) is connected to $V_{cm}$, and the bottom plate is connected to $V_{in}$.

As shown in Fig. 4, $\Phi$ $_{SB}$ and $\Phi_{HB}$ are the inverted phases of $\Phi_S$ and $\Phi$ $_H$, respectively. Upon the arrival of $\Phi$ $_H$, V $_x$<4> remains floating, and the bottom plate of CDAC $_1$<4> is configured to generate $V_{QTH}$<4> for flash quantization. Controlled by $V_{QTH}$ generation logic, the bottom plates of $4C_u$, $2C_u$, $C_{ua}$, and $C_{ub}$ are connected to $V_{ref}$, GND, GND, and $V_{ref}$, respectively, forming $V_{QTH}$<4>=$5V_{ref}/8$. Besides, the corresponding digital code for V $_{QTH}$<4> is represented as 1-0-0-1. As $V_{QTH}$<4> settled, $V_x$<4> transitions to $V_{QTH}$<4>-$V_{in}$ by charge conservation. In the following, $\Phi_{C1}$ triggers the 2× interpolating comparators at the end of $\Phi$ $_H$, obtaining the comparison results of $V_{in}$ with $V_{QTH}$<4> and $V_{in}$ with the interpolated threshold ($V_{QTH}$<3>+$V_{QTH}$<4>)/2 from Slice<3>,

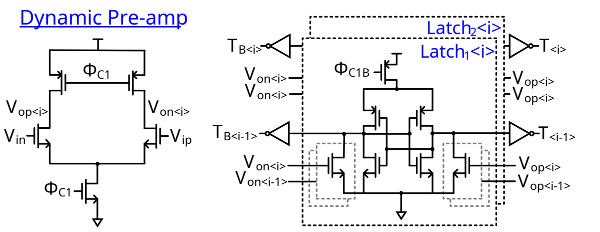

Fig. 6 Dynamic pre-amp and the interpolated latch pairs [5].

| | $4C_u$ | $2C_u$ | $C_{ua}$ | $C_{ub}$ |
|---|---|---|---|---|
| Slice<0> | 0 | 0 | 0 | 1 |
| Slice<1> | 0 | 0 | 1 | 1 |
| Slice<2> | 0 | 1 | 0 | 1 |
| Slice<3> | 0 | 1 | 1 | 1 |
| Slice<4> | 1 | 0 | 0 | 1 |
| Slice<5> | 1 | 0 | 1 | 1 |
| Slice<6> | 1 | 1 | 0 | 1 |
| Slice<7> | 1 | 1 | 1 | 1 |

| | Value |
|---|---|
| $V_{QTH}$<0> | $\frac{1}{8}V_{ref}$ |
| $V_{QTH}$<1> | $\frac{2}{8}V_{ref}$ |
| $V_{QTH}$<2> | $\frac{3}{8}V_{ref}$ |
| $V_{QTH}$<3> | $\frac{4}{8}V_{ref}$ |
| $V_{QTH}$<4> | $\frac{5}{8}V_{ref}$ |
| $V_{QTH}$<5> | $\frac{6}{8}V_{ref}$ |
| $V_{QTH}$<6> | $\frac{7}{8}V_{ref}$ |
| $V_{QTH}$<7> | $\frac{8}{8}V_{ref}$ |

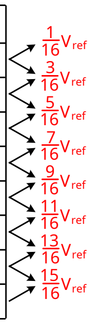

Fig. 7 $V_{QTH}$ corresponding digital code and interpolated $V_{QTH}$.

yielding T<9:8>. In this example, we assume T<9:8> = 11.

After quantization, $\Phi_H$ falls and disconnects the $CDAC_1$<4> bottom plates from $V_{QTH}$<4>, allowing them to be controlled by T<9:8> as shown in Fig. 5. Specifically, T<9> is assigned to the bottom plate of $4C_u$, while T<8> controls $2C_u$, $C_{ua}$, and $C_{ub}$ to ensure even weighting for each thermometer code. During the amplification phase $\Phi_R$, the $V_x$<i> in all slices are connected to the RA input, generating the residue $V_{res}$. The charge sharing between $CDAC_1$<0:7> and charge transfer of closed-loop RA occurs at the same time as the $V_x$ approaches virtual ground gradually.

Fig. 6 shows the dynamic pre-amp and the interpolated latch pairs in the flash quantizer. Fig. 7 depicts the digital code and corresponding $V_{QTH}$ for each flash slice to configure during the $\Phi_H$ phase, along with the interpolated $V_{QTH}$ values.

### C. Residue Amplifier and Backend Quantizer

As shown in Fig. 8, the residue amplifier adopts a two-stage miller-compensated OTA under a 1V supply. The single-channel 9-bit 500MS/s SAR ADC in the backend includes a 32LSB weight redundancy as shown in Fig. 8. To meet matching requirements, the total capacitance $C_{tot}$ is designed as 136fF, and the unit capacitor $C_{u2}$ is 0.5fF. In face of a large capacitor load, the second stage of RA must consume significant power for enough phase margin (PM). A 100fF $C_2$ is inserted and connected in series with the $CDAC_2$ to reduce the loading of the RA to 57fF while maintaining high $CDAC_2$ matching accuracy. Additionally, the power consumption of the second stage of RA is reduced from 5.5mA to 2.3mA after introducing $C_2$ while maintaining 60° PM. The additional noise contribution to the overall ADC remains negligible due to the high gain of RA.

## III. Measurement Results

The 12-bit 2GS/s flash-embedded-MDAC based pipelined ADC is implemented in a 28nm CMOS process, occupying 0.068mm² as shown in Fig. 9. Comparators' offset calibration is implemented on-chip, while inter-stage gain and CDAC mismatches are calibrated off-chip. The ADC consumes 23.26mW at 2GS/s, where the flash-embedded MDAC consumes 10.21mW, the RA consumes 6.40mW, the

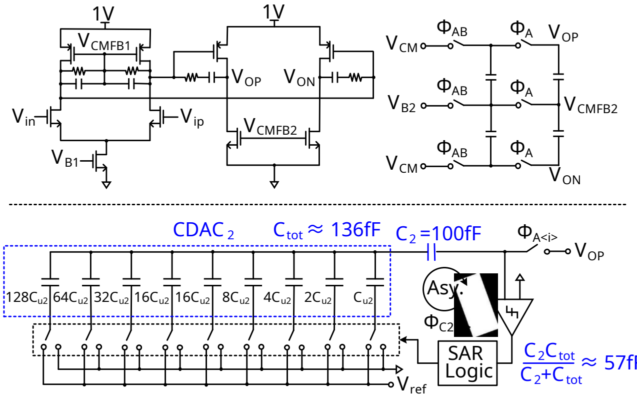

Fig. 8 Miller-compensated OTA and single-channel 9-bit 500MS/s SAR ADC.

TI-SAR backend consumes 3.89mW, and the clock generation consumes 2.76mW, respectively, as shown in Fig. 10.

As shown in Fig. 11, the measured SNDR and SFDR are 59.1dB and 77.3dB at 40MHz input, and 58.3dB and 73.4dB at Nyquist input, respectively. As shown in Fig. 12, the measured DNL and INL are within -0.83/+0.98LSB and -1.79/+1.52LSB. To evaluate wide ERBW, SNDR and SFDR are measured across input frequencies, as shown in Fig. 13, where the ADC exhibits <3dB SNDR drop up to 1.7GHz input. Additionally, no code-saturation of backend TI-SAR occurs across input frequencies up to 3.2GHz, verifying that the flash-embedded MDAC is free of aperture error.

Table I compares the performance of the proposed pipelined ADC with other state-of-the-art high-speed and high-resolution pipelined ADCs. The aperture-error-free flash-embedded-MDAC based pipelined ADC achieves a high ERBW of 1700MHz and a high FoMs of 168.4dB, with a minimized number of pipeline stages.

## IV. Conclusion

This work proposes a novel aperture-error-free method by merging the first-stage MDAC and multi-bit flash ADC, achieving high energy efficiency conversion. Additionally, a multi-bit flash quantization threshold voltage self-generation

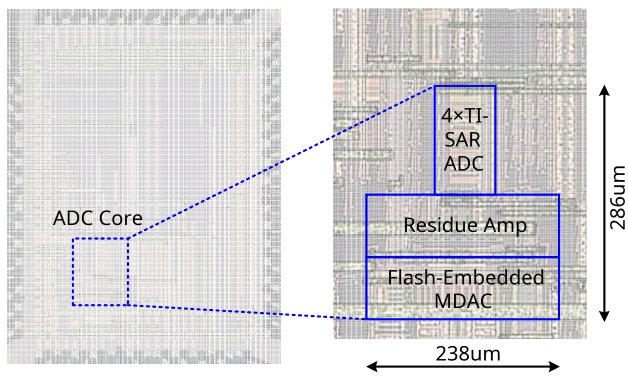

Fig. 9 Die photo.

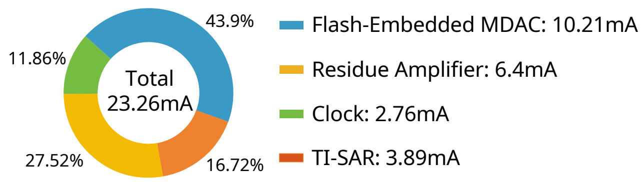

Fig. 10 Power breakdown of the proposed pipelined ADC.

TABLE I. PERFORMANCE SUMMARY AND COMPARISON WITH SOTA PIPELINED ADCS

| | This work | | ISSCC'23 Y.Cao | ISSCC'23 H.Sung | VLSI'16 A.Ali | ISSCC'19 B.Hershberg |
|---|---|---|---|---|---|---|
| Process [nm] | 28 | | 28 | 7 | 28 | 16 |
| Sampling Stage Architecture | Flash-Embedded MDAC | | Time-Domain SHA-Less | Differential-Sample SHA-Less | Conventional SHA-Less | Passive-Hold MDAC |
| Aperture-Error-Free | Yes | | No | No | No | Yes |
| Supply [V] | 1 | | 1 | 1/0.85 | 0.9 | 0.85 |
| Sampling Rate [MS/s] | 2000 | | 2000 | 1800 | 2500 | 3200 |
| TI Factor | 1 | | 1 | 2 | 1 | 4 |
| Resolution [bit] | 12 | | 12 | 12 | 14 | 13 |
| SNDR [dB] | 59.1(@LF) | 58.3(@Nyq.) | 60.4 | 60.16 | 62.0 | 61.7 |
| SFDR [dB] | 77.3(@LF) | 73.4(@Nyq.) | 75.8 | 69.2 | 73.0 | 73.3 |
| Power [mW] | 23.26 | | $27^{+}$ | $7.55^{+}$ | $1150^{++}$ | $61.3^{++}$ |
| FoMs [dB] | 168.4* | | 166.1 | 170.9 | 152.0 | 165.9 |
| FoMw [fJ/conv.-step] | 17.3 | | 15.8 | 5.08 | 447 | 19.3 |
| ERBW/BW [MHz] | 1700 | | $1100^{\#}$ | $900^{\#\#}$ | $1400^{\#}$ | $1900^{\#}$ |
| Number of Stages | 2 | | 4 | 8 | 6 | 10 |

$^{+}$: Include $V_{ref}$ buffer power. $^{++}$: Include $V_{ref}$ buffer and input buffer power. *: FoMs=SNDR(@ERBW) + 10log(ERBW/Power).

$^{\#}$ : The reported information is obtained based on measured performance versus input frequency figures.

$^{\#\#}$ : The reported information is the maximum measured input frequency.

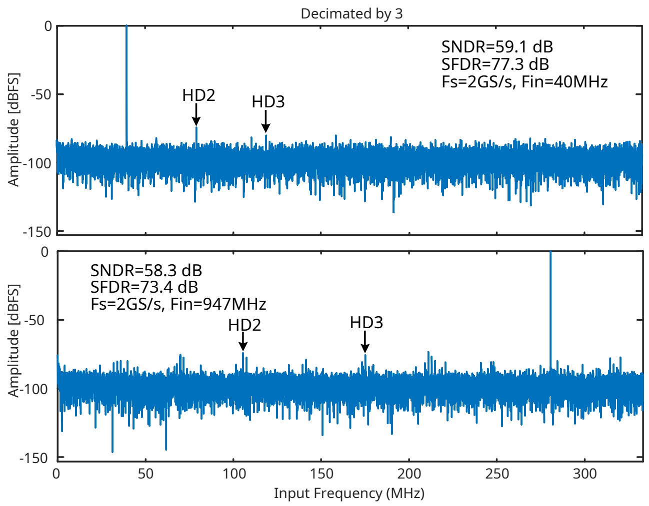


Fig. 11 Measured output spectra.

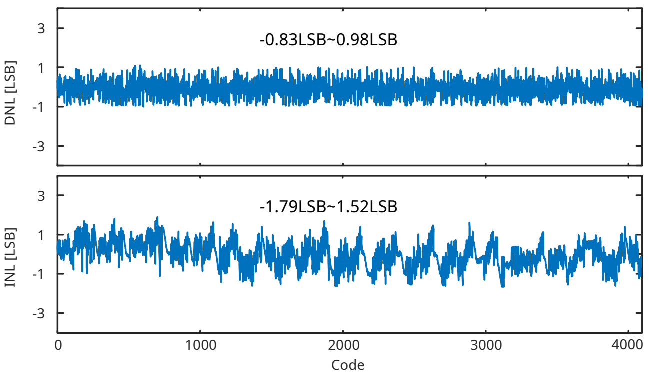


Fig. 12 Measured DNL/INL curves.

technique is introduced to generate accurate $V_{QTHS}$, supporting high-resolution flash ADC. The proposed method enables a 12-bit 2GS/s pipelined ADC prototype, achieving an SNDR of 58.3dB and an SFDR of 73.4dB at the Nyquist frequency, with an ERBW of 1.7GHz.

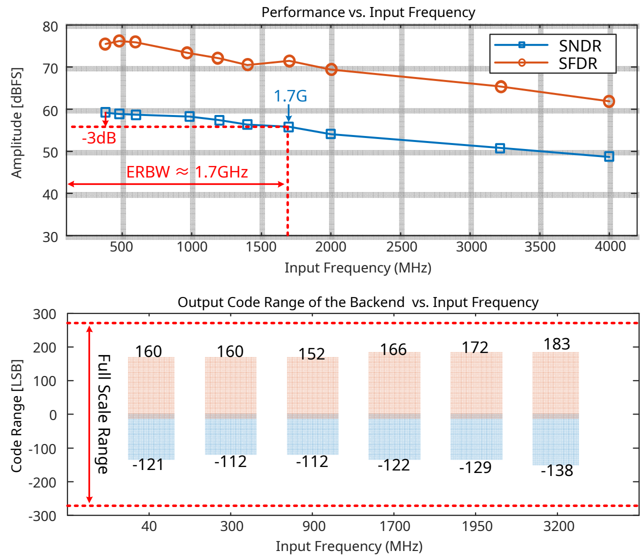


Fig. 13 Measured SNDR, SFDR, and output code range of the backend versus input signal frequency.

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