A 600-V Fully-Integrated Hybrid-Burst Capacitor Coupling Level Shifter with 130-V/ns Common Mode Transient Immunity

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***Abstract*—In this paper a 600-V fully-integrated capacitor coupling level shifter (CCLS) is presented. The solution exploits the advantages of using high-voltage capacitors (HVCs) as communication elements, which leads to a better isolation between different domains. Through this approach, only the HVCs are required to withstand the complete voltage range of the application. Furthermore, HVCs exhibit inherent symmetry, enabling them to withstand high voltage with both polarities. Thanks to a dedicated compensation structure, the design achieves high common-mode transient immunity (CMTI). The proposed level shifter is the first fully-integrated capacitive coupled solution capable of operating up to 600 V, allowing pulse width modulation (PWM) control signals to be applied to high-side power devices. The receiver structure of the CCLS is based on current mirrors. The proposed CCLS is implemented in a 0.4-µm high-voltage CMOS process with an area of 0.275 mm^2 and embedded within a complete half-bridge gate driver (GD), achieving a remarkable CMTI performance of 130-V/ns, while maintaining the propagation delay in the range of few nanoseconds.**

I. Introduction

For future industrial and automotive applications, the growing demand for robust, high-power-density devices operated at progressively higher voltages is presenting considerable challenges for pulse width modulation (PWM) control systems. Furthermore, the advent of wide-bandgap technologies, such as Gallium Nitride (GaN) and Silicon Carbide (SiC), results in increasing switching speed (dV/dt) and switching frequency (f_{sw}). Consequently, the implementation of level shifters (LSs), which are essential for transferring the signals from the low-voltage domain of the low-side switch to the high-voltage domain of the high-side switch, is becoming challenging, particularly when aiming for fully-integrated solutions, in which all crucial components of the LS block, transmitter, receiver, and high-voltage communication devices, are integrated within the same gate driver (GD) die. High-voltage fully-integrated LSs fabricated using BCD processes are typically implemented with active components [1], such as laterally diffused n-channel DMOS (LNDMOS) transistors, which must sustain the entire voltage range of the given application, using a junction approach for isolation, and inherently consuming static power.

An alternative approach for implementing a communication channel between the low-side and high-side domains at high voltage is the use of high-voltage capacitors. This approach is, however, typically implemented using external capacitors. In this work, we introduce a 600-V fully-integrated capacitor-coupling level shifter (CCLS), which exploits integrated capacitors with an hybrid-burst approach and a current-mirror-based receiver, achieving compact design, fast propagation delay, and very high common-mode transient immunity (CMTI) performance.

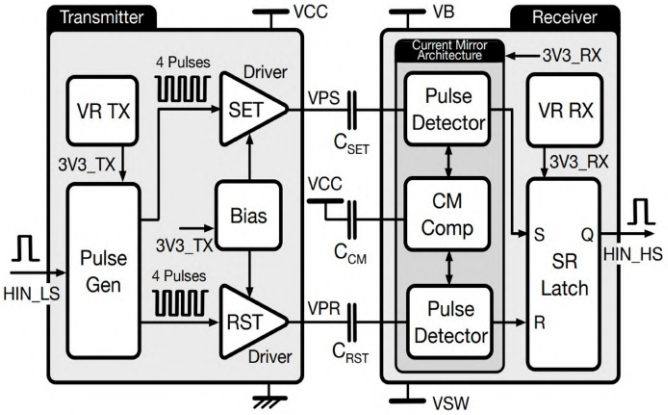

Fig. 1. Block diagram of the designed fully-integrated CCLS.

II. Proposed Fully-Integrated Capacitor Coupling Level Shifter (CCLS)

Fig. 1 illustrates the block diagram of the implemented fully-integrated CCLS. The structure is based on a latch approach, where the PWM information sent by the transmitter is stored in an SR latch at the receiver side. This solution has been selected rather than an OOK approach, with the goal of minimizing the static current consumption and maximizing the power efficiency. The transmitter must refresh the information each time the input signal (HIN_LS) changes, by either setting or resetting the latch at the receiver side. This is achieved by injecting into the latch current pulses, obtained through burst voltage transitions across the high-voltage capacitors.

A. Voltage Pulse Transmitter

The transmitter comprises a pulse generator, two drivers (set and reset), a bias block, and a voltage regulator. When a low-to-high transition of HIN_LS is detected, the pulse generator

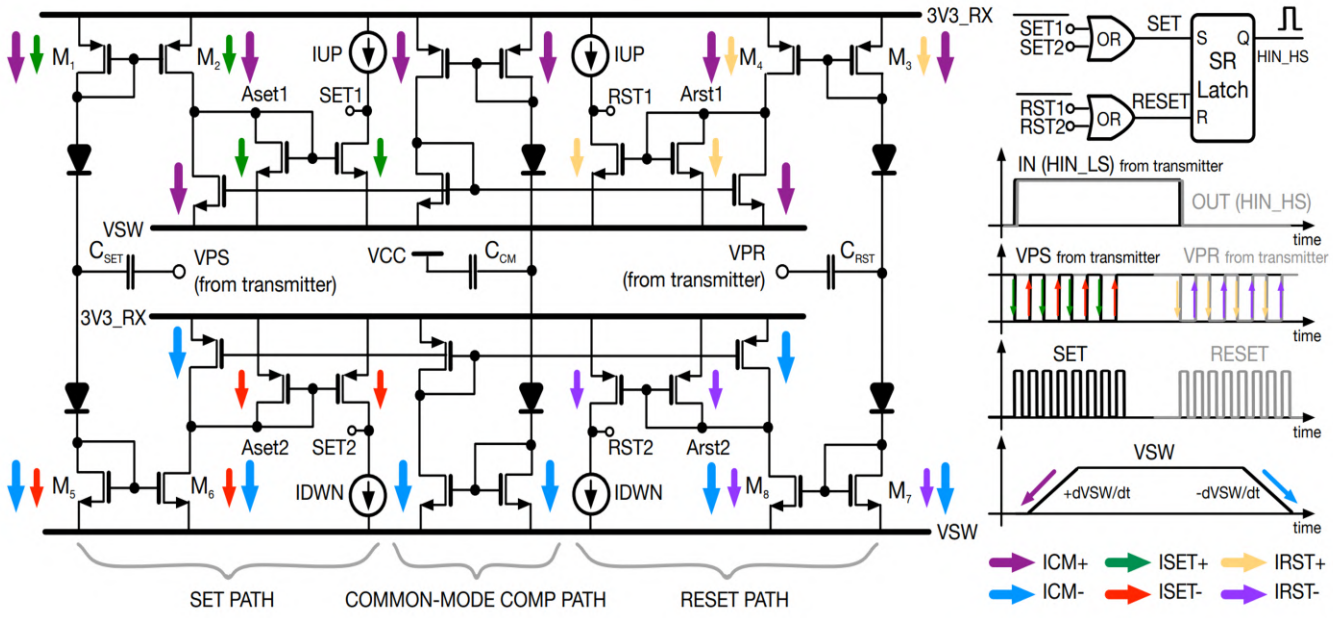

Fig. 2. Schematic diagram of the CCLS receiver.

produces a burst of four pulses, which are applied to the set driver. Conversely, a burst of four pulses is sent to the reset driver when a high-to-low transition of HIN_LS occurs. Therefore, whenever the transmitter needs to send information, eight consecutive voltage transitions (four high-to-low and four low-to-high edges) are applied to the bottom plate of the corresponding high-voltage capacitor (HVC) at an equivalent frequency of 80 MHz.

A 3.3-V supply for the pulse generator is produced on-chip starting from the low-side GD power supply (VCC) through a dedicated voltage regulator (VR TX) . The 3.3-V square waves produced by the pulse generator are level-shifted by the drivers to the VCC domain before being applied to the bottom plate of the HVCs (signals VPS and VPR), maintaining the desired pulse duration, which is essential for accurate detection in the receiver. The HVCs have a value of 100 fF, leading to current pulses with an amplitude of approximately 3-4 mA during both high-to-low and low-to-high transitions.

Two capacitors (C_{SET} and C_{RST}) are used to implement the set and reset paths toward the receiver, while an additional capacitor (C_{CM}) is required to generate a current at the receiver side proportional to the slew rate of the switching node VSW, used for common-mode compensation. The bottom plate of C_{CM} is connected to VCC. The HVCs are metal stack capacitors available within the high-voltage technology used.

B. Current Mirror Receiver

Fig. 2 depicts the proposed receiver structure, which is based on current mirrors. PMOS current mirrors (M1-M2 and M3-M4) and NMOS current mirrors (M5-M6 and M7-M8) are used in both the SET PATH and the RESET PATH to detect the injected currents. For the set burst, high-to-low and low-to-high transitions at node VPS generate injected currents ISET+ (green) and ISET– (red), respectively, within the SET PATH. When these currents become larger than the corresponding pullup (IUP) or pulldown (IDWN) currents, voltage pulses occur at nodes SET1 or SET2, respectively. Similarly, for the reset burst, high-to-low and low-to-high transitions at node VPR generate injected currents IRST+ (yellow) and IRST– (purple), respectively, within the RESET PATH. When these currents overcome the corresponding pullup or pulldown currents, voltage pulses are generated at nodes RST1 or RST2, respectively. The pulses at nodes SET1/SET2 and RST1/RST2 are combined through two OR gates, generating eight voltage pulses at the SET and RESET nodes. It can be observed that, while a single pulse is enough to set or reset the latch, eight transitions are used to ensure redundancy and prevent any missed cycle.

Rapid voltage transitions at node VSW generate common-mode currents (ICM) proportional to the value of the HVCs and to the slew rate, according to the relation $\text{ICM} = (d\text{VSW}/dt) \times \text{HVC}$. During the rising edges of VSW, the current through all capacitors is ICM+ (violet), while during the falling edges of VSW it is ICM– (light blue). These currents, which can be of the order of tens of milliamperes, flow through the PMOS or NMOS current mirrors, depending on the sign of the slew rate, and would lead to undesired transitions at the decision node. To address this issue, a compensation path is introduced to sense both the falling and rising edges of VSW and compensate for the common-mode current components ICM+ and ICM– at nodes Aset1/Arst1 and Aset2/Arst2, respectively. The value of the pullup (IUP) or

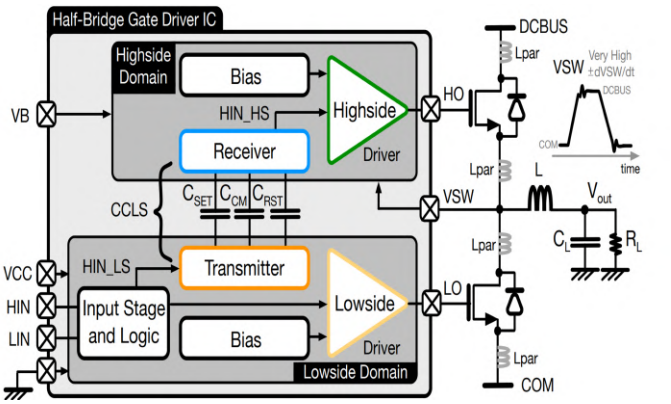

Fig. 3. Block diagram of the designed half-bridge gate driver.

pulldown (IDWN) currents is chosen to maintain the decision nodes in the correct state when there is no transmission on the HVCs, according to the matching specifications of the HVCs and the technology process and temperature variations of the entire receiver, thus ensuring a static common-mode transient immunity (CMTIstatic) of at least 100 V/ns. Conversely, the transmitted current pulses must be sufficiently large to overcome the pullup or pulldown current even during common-mode transitions, thus preventing distortion or missed cycles and ensuring the desired dynamic common-mode transient immunity (CMTIdynamic) of at least 20 V/ns.

III. Half-Bridge Gate Driver Implementation and Measurement Results

The proposed CCLS has been embedded in a half-bridge GD, as shown in Fig. 3, which interfaces the micro-controller outputs (LIN and HIN) to the gates of the power devices (HO and LO). In this case the external power devices are arranged in half-bridge configuration and connected between a 600-V DCBUS and COM. The capacitive coupling architecture offers a solution for achieving both signal transmission and high isolation between the high-side and the low-side domains in a single integrated solution. The complete device has been fabricated in a 0.4-µm, high-voltage CMOS process. The micrograph of the implemented half-bridge GD is depicted in Fig. 4. The CCLS solution has an active area of 0.275 mm^2, including transmitter, HVCs, and receiver.

The correct operation of the level shifter has been verified and tested inside the GD. The measured propagation delay of the CCLS is 5.88 ns, which aligns with the simulation results. Analysis of the measured waveforms for the switching gate driver inputs (LIN and HIN) and the corresponding outputs (LO and HO), along with the CCLS output (HIN_HS), confirm the correct operation of the entire circuit. The complete GD provides +2 A/−2 A output current, an output voltage ranging from 0 to 32 V and a propagation delay of 35 ns. During bench characterization, the maximum measured GD operating frequency ($f_{sw,\max}$) is 20 MHz for the HIN to HO chain. which is more than adequate for motor driving applications (f_{sw} up to hundred kilohertz).

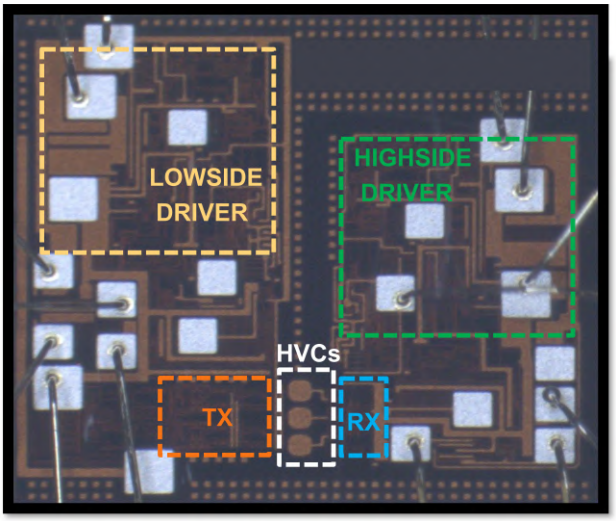

Fig. 4. Micrograph of the implemented half bridge GD.

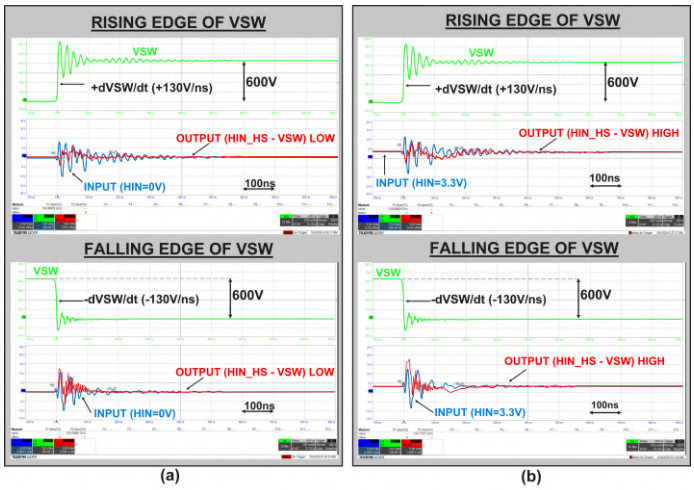

Fig. 5. Measured static common mode transition immunity (CMTIstatic), with output (a) low, (b) high.

A. CMTI Static Performance

A crucial parameter to consider is the resilience of the level shifter to common-mode transitions. Fig. 5(a) and (b) show signals HIN and HIN_HS in the presence of rising and falling edges of VSW, with the SR latch initially set to the high and low states, to demonstrate static common-mode transient immunity (CMTIstatic). The HIN_HS signal remains in the previously configured state in all possible scenarios, and no wrong information is stored in the SR latch. The proposed solution is capable of achieving proper common-mode compensation for both VSW rise and fall events with a slew rate up to 130 V/ns. Furthermore, during fast switching transitions the VSW voltage node can go below ground and the level shifter is able to keep the stored information, thanks to its symmetric structure.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH THE STATE-OF-THE-ART

Parameters	**ICCSS '22 [1]**	**TCAS-II '21 [2]**	**ESSCIRC '18 [3]**	**TCAS-I '23 [4]**	**This Work**
Note	Simulated	Simulated	Measured	Measured	**Measured**
LS Approach	LNDMOS	CCLS	CCLS	CCLS	**CCLS**
Process	BCD	BCD-on-SOI	BiCMOS	HV BCD	**HV CMOS**
Technology node L [µm]	0.8	0.18	0.18	0.5	**0.4**
Chip Area [mm²]	N.A.	0.010	0.007	0.051	**0.275**
Voltage,max [V]	600	200	50	50	**600**
Delay TD [ns]	5.9	0.67	1.36	1.26	**5.88**
f_{sw} [MHz]	20	20	120	50	**20**
Voltage,min [V]	N.A.	-200	N.A.	-5	**-600**
CMTIstatic [V/ns]	N.A.	N.A.	6	56	**130**
CMTIdynamic [V/ns]	N.A.	N.A.	N.A.	N.A.	**20**
FOM1=TD/(L*Voltage,max) [ns/(μm*V)]	0.0123	0.0186	0.1511	0.0504	**0.0246**
FOM2=TD/(L*Voltage,max*CMTIstatic) [ns^2/(μm*V^2)]	N.A.	N.A.	0.0252	0.0009	**0.0002**

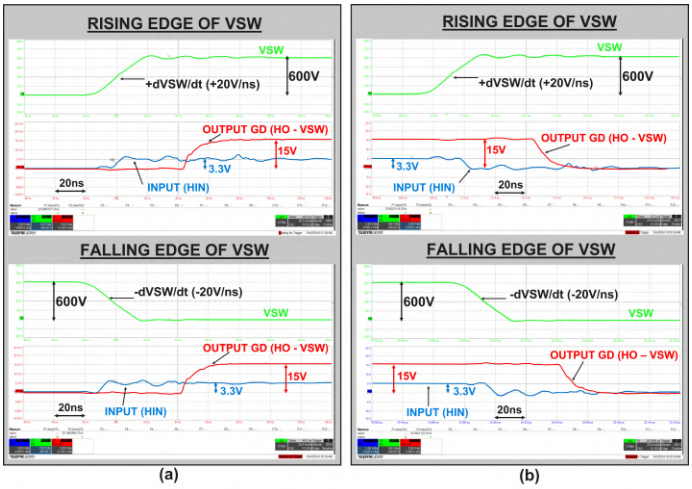

Fig. 6. Measured dynamic common mode transition immunity (CMTIdynamic), during (a) set, (b) reset.

B. CMTI Dynamic Performance

Thanks to the implemented common-mode compensation scheme, the proposed CCLS can successfully transmit set and reset information even during VSW transitions. Fig. 6(a) and (b) illustrate the measured dynamic common-mode transient immunity (CMTIdynamic) for both set and reset output. The high-side output of the GD (HO) is evaluated in the presence of rising and falling transitions of VSW. The proposed CCLS is capable of sending a turn-on and a turn-off signal without distortion for VSW slew rates up to $\pm$20 V/ns. For larger slew rate values, the HO signal is distorted. However, thanks to the redundancy provided by the burst pulses the missed cycle is avoided. To elaborate further, the transmission process must be maintained effectively, even if there is distortion, as this is critical for preserving the integrity of the current originating from the high-side power switch. This is essential to avoid any interruptions in the motor cycle, thereby ensuring continuous and efficient operation.

IV. CONCLUSION

This paper introduces a novel capacitor coupling level shifter that has been experimentally validated within a half-bridge gate driver. A summary of the CCLS performance is provided in Table 1, where it is compared to the state-of-the-art. Notably, while the solution does not achieve sub-nanosecond propagation delay, it is comparable to other fast approaches [1] and is uniquely suited for translating PWM signals in the high-side domain for industrial applications. This is due to its ability to operate at voltages up to 600-V, which is twelve times higher than other CCLSs with measured results. Furthermore, the proposed CCLS achieves the lowest Figure-of-Merit (FOM1) value of 0.0246 ns/(µm×V).

To provide a comprehensive evaluation of the architecture performance, the static common-mode transient immunity (CMTIstatic) has also been considered, and a new Figure-of-Merit (FOM2) has been introduced. The proposed CCLS achieves a remarkable FOM2 value of 0.0002 ns^2/(µm$\times$V^2), representing a performance improvement of more than four times better than [3] and [4]. This is particularly significant, as the innovative CCLS presented is specifically designed for translating PWM signals, unlike the solutions reported in [3] and [4].

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