Towards Ultra Low Thermo-Mechanical Sensitive Capacitors in CMOS

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***Abstract*—Fully integrated capacitors in CMOS with a low sensitivity to temperature and externally applied mechanical forces are crucial for highly stable, fully integrated frequency references. Thermal changes and external forces alter the physical structure of capacitors, affecting their capacitance. This paper presents measurements of the temperature dependency and mechanical stress sensitivity of several custom back-end capacitors, with a front-end capacitor for benchmarking. On-wafer and in-package measurements were conducted to (try to) separate thermal and stress effects. We show that both measured sensitivities are hardly (cor)related for backend capacitors. Thermal effects appear to be mainly related to inter-terminal oxide material whereas external force sensitivity shows a dependency on the capacitance direction and the distance from the top of the backend.**

***Index Terms*—Accuracy, Capacitance temperature coefficient, Capacitors, Mechanical stress, Packaging, Temperature.**

I. Introduction

The performance of electronic systems is ultimately limited by the accuracy of their references, such as voltage, current and frequency references. Quartz crystals are the *de facto* standard in industry for high frequency accuracy [1] but cannot be integrated in commercial IC technologies. Alternatively, high frequency accuracy for fully (CMOS) integrated oscillators can be achieved by locking to an external clock, e.g., provided via an I/O bus [2] or via a wireless channel [3]. For integration and for tampering reduction [4], [5] reasons, there is a strong drive towards (fully) integrated reference circuits.

The highest accuracy to date of fully CMOS integrated frequency references is achieved using LC-oscillators [6]. As shown in [6], [7] the reference frequency accuracy is ultimately determined by the inductance L, the (effective) capacitance C, their temperature coefficients $\mathrm{TC_L}$ respectively $\mathrm{TC_C}$, and the spread thereof. The work in [6] achieves a frequency accuracy of 0.7 ppm/°C over a temperature range from −63 °C-165 °C using a single room-temperature trim. This requires $\mathrm{TC_L}$ and $\mathrm{TC_C}$ to spread less than about 1 ppm/°C. To further improve performance, innovation must be implemented at the device or component level. For CMOS based inductors, both L and $\mathrm{TC_L}$ depend on the inductor geometry and material properties, via e.g. Eddy currents and the temperature dependency of resistance ($\mathrm{TC_R}$) [8]. As CMOS based inductors are typically relatively large (easily 50 µm diameter or more), the impact of changes in geometry due to e.g., mechanical stress and temperature variations on L and $\mathrm{TC_L}$ are negligibly small. Consequently, $\mathrm{TC_L}$ and its dependencies are well known, allowing to design inductors with low, well-defined $\mathrm{TC_L}$ [8].

This work focusus on CMOS (back-end) capacitors; these metal-oxide-metal (MOM) capacitors are more stable over lifetime and temperature compared to front-end (gate-oxide-silicon) capacitors [9], [10]. Back-end capacitors typically exhibit small $\mathrm{TC_C}$ values with little spread. While they can occupy relatively large areas, their capacitance C depends on small plate-plate or finger-finger distances. Changes in these distances — caused by thermal effects or due to external (possibly temperature dependent) stress — impact C and $\mathrm{TC_C}$. These effects become significant when aiming for single-digit $\mathrm{TC_C}$ values, essential for highly accurate CMOS integrated frequency references [11], [12].

This paper dives into multiple aspects that impact the stability of (MOM) CMOS back-end capacitors over temperature and stress. MIM capacitors are excluded as these are not available in all commercial CMOS technologies. To focus on capacitors' $\mathrm{TC_C}$ and stress sensitivity, we explicitly aim to discard the impact of inductive and resistive effects in wiring and in the plates on Cs and $\mathrm{TC_C}$s. First, the theoretical background underlying the $\mathrm{TC_C}$ and stress sensitivity is discussed briefly. Next, the custom designed capacitors and measurement setups used are described. After that, measurement results are presented, and conclusions are drawn.

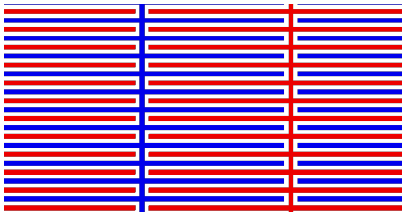
II. Theoretical background

The capacitance of a capacitor is determined by its geometry and the permittivity of the dielectric between and around the plates. Since the plates of a back-end capacitor are made of (highly conductive) metals, negligibly low (temperature dependent) effects of space charge is expected, in contrast to the situation of front-end capacitors [10].

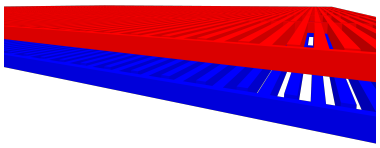
We assume that the $\mathrm{TC_C}$ is due to geometry changes of the capacitor structure induced by thermal effects. These temperature-driven geometry changes depend on the coefficient of thermal expansion (CTE) and on the material stiffness (expressed in Young's modulus E and Poisson ratios ν) of all materials in and around the IC. Note that these include the silicon wafer and (if packaged) include the lead frame and package material. With increasing temperature, materials tend to expand, but are restricted by neighboring materials with differing expansions, leading to mechanical stress and strain.

A very much related temperature effect can be formulated for material permittivities. Ignoring frequency-dependent factors like dipoles and polarizations [13], and assuming amorphous dielectric layers, we focus solely on volume changes due to the interplay of materials' CTEs and Es. These changes affect mass density, linking permittivity to material quantity—a phenomenon commonly known for gases [14].

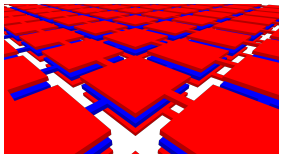
Note that this implies that back-end capacitors are sensitive to external (e.g., package) stress, complying with the findings



(a) Top view of a part of a single-layer comb capacitor



(b) Side view of a dual-layer "plate" capacitor



(c) 3D view of a triple layer square capacitor

(d) Back-end stack

Figure 1. (a)-(c) Renders of examples of the different back-end capacitors wherein the two plates are color-coded; the dielectrics are not shown; (d) the relevant, simplified cross section of the back-end of the utilized technology. Relevant capacitor metals and -dielectrics are between 250 nm-400 nm thick.

in [15]. Whereas the impact of stress on various properties of *front-end devices* like BJTs is well known [16]–[19], it is not well described for back-end components like capacitors and inductors which is probably due to their much lower sensitivities. However, for highly stable CMOS integrated frequency references, even the low TC_C and stress sensitivity of back-end capacitors are crucial.

III. Devices

To study TC_Cs and the impact of mechanical stress, several custom MOM capacitors were designed in a commercial CMOS technology. Different geometries were made to distinguish effects originating from the dielectric type, place in back-end stack and type of capacitor (lateral or horizontal, plate or fringe). The capacitors can be classified in 3 groups. The first group consists of interdigitated combs in a single metal layer (see Figure 1a), forming a lateral parallel plate capacitance with a significant fringe capacitance. The second group consists of a similar structure, but fabricated in two metal layers directly above each other where each metal layer holds a different capacitor plate, see Figure 1b. Adhering to density rules, this yields a vertical plate capacitance with minimal fringe capacitance. All comb capacitors have the same finger spacings. The third group consists of a grid of squares in multiple layers, also creating horizontal parallel plate capacitors, see Figure 1c. All of these types were fabricated with the same metal, but in several different layers, surrounded by different dielectrics, as depicted in Figure 1d. These capacitors were benchmarked to a PDK-supplied Alternate Polarity MOM (APMOM) capacitor consisting of staggered interdigitated combs in multiple metal layers having mainly fringe capacitance. A list of devices with specifics is summarized in Table I.

IV. Measurement Setups

Three different measurement setups were used. Absolute capacitance and its TC_C were measured using S-parameters on a wafer-prober (see Section IV-A), a proven highly accurate method [8].

Mechanical stress sensitivity was measured using dedicated on-chip charge based capacitance measurement (CBCM) [20] circuits, which can continuously measure the capacitance when external forces are applied, and can be used in closed packages while having the accuracy-defining equipment outside of it. Each capacitor has its own CBCM readout; some basics of CBCMs are reviewed in Section IV-B. All mechanical stress measurements were done on (grinded down to 250 µm thickness) dies that are glued and bonded in (HV)QFN-72 packages. For external point stress measurements (see Section IV-C) we used open cavity QFN packages to enable applying point stress at the capacitors using a pressing probe needle (PPN) [16]. For uniform external stress measurements (see Section IV-D), we used HVQFN plastic molded packages. In our mechanical stress measurement setups, the temperature is not controlled, resulting in a relatively low capacitor readout resolution of about 100 ppm.

A. On-wafer Setup

To measure TC_Cs, a 725 µm thick wafer with various capacitors in dedicated RF measurement configurations, was probed on a FormFactor SUMMIT 200 system at −40 °C, 25 °C, and 100 °C, using a Keysight N5227B PNA to measure the two-port S-parameters. The calibration was done via an LRRM (Line Reflect Reflect Match) procedure. The effect of the on-wafer pads and interconnects is de-embedded at all three temperatures in post-processing using measured on-wafer short, open and load dummies. Final capacitance values were extracted from the Y_{DUT} parameters.

B. CBCMs for Stress Measurements

The most basic CBCM method works with two switches S_1 and S_2, which alternatingly charge and discharge a connected capacitor C_{DUT} with a known frequency f to a voltage V_s and ground respectively. A sketch of our implemented CBCM is shown in Figure 2. The (average) current delivered by the source V_S over an integer charge/discharge cycles is $\overline{I_{\mathrm{DUT}}} = f \cdot V_s \cdot (C_{\mathrm{DUT}} + C_{\mathrm{parasitic}})$ where $C_{\mathrm{parasitic}}$ includes, e.g., switch-, wiring- and junction capacitances. To de-embed $C_{\mathrm{parasitic}}$, a CBCM copy without C_{DUT} is added, drawing $\overline{I_{\mathrm{DUM}}} = f \cdot V_s \cdot C_{\mathrm{parasitic}}$. The estimated value of C_{DUT} is then

$$\hat{C}_{\mathrm{DUT}} = \frac{\overline{I_{\mathrm{DUT}}} - \overline{I_{\mathrm{DUM}}}}{f \cdot V_s}. \tag{1}$$

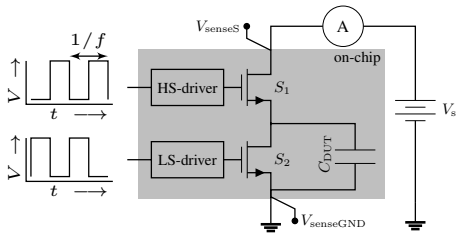


Figure 2. Basic schematic of the DUT part of our implemented CBCM.

Switches S_1 and S_2 are usually implemented as a "pseudo-inverter", with a P- and NMOS respectively. We chose to implement S_1 as a bootstrapped NMOS to improve switching speed and matching. The two clock signals are provided from (phase locked) off-chip function generators. The V_s voltage sources were implemented via 4-point SMUs.

C. PPN Measurement Setup

We used a manually controlled PPN setup to measure mechanical point-sensitivity of the capacitors. The probe was manually landed approximately in the middle of the capacitor under test (see Figure 3) with forces of approximately 1 g (1 mN) and 2 g (2 mN). To prevent influences from both the thermal and electrical conductivity of a traditionally used tungsten needle, a glass needle was made from a tapered glass fiber [21], glued to a tungsten needle several millimeters away from the IC. The needle tip diameter is estimated to be approximately 40 µm, with a contact radius of just a few µm, which translates into an applied pressure over 100 MPa. A micrograph of the setup, also indicating DUM/DUT CBCMs and the RF structures, is shown in Figure 3.

All listed capacitors were measured with their own DUT/DUM pair of CBCMs. The PPN measurements were done on single dies, in open QFN72 packages measured in an open socket on a PCB. In this setup, the temperature cannot be controlled accurately which limits measurement resolution; consequently for several capacitors only an upper boundary of about 150 ppm of "no effects" can be given.

D. Uniform Stress Measurement Setup

Two capacitors, the front-end one and the M3M4 capacitor, were also tested in a molded plastic HVQFN-72 package under a uniform force. The package was soldered on a PCB mounted on a load cell (to measure the pressure) in a mechanical clamp, applying forces up to 500 N. Optimistically assuming that this force is uniformly applied across the package, i.e. neglecting the different stiffness of the 4.9 mm^2 silicon die and the 100 mm^2 surface of the HVQFN72 package material, this translates into a conservative estimation of up to 5 MPa pressure.

V. Measurement Results

The measured TC_Cs can be found in Table I. Looking at the TC_Cs, it is obvious that back-end capacitors have a smaller TC_C than a front-end capacitor. The primary dielectric (that dominantly determines the capacitance) seems to impact the TC_C; capacitors with TEOS dielectrics seem to have a lower or even negative TC_C compared to capacitors with fluorine doped TEOS (FTEOS) dielectrics. Moreover, it appears that

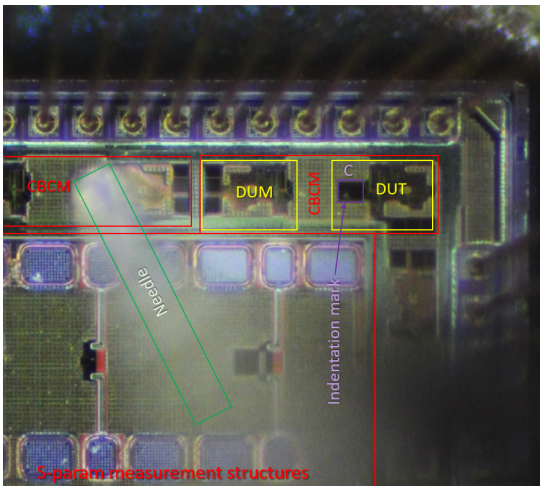


Figure 3. Micrograph of the PPN setup, highlighting a part of the die, the glass pressing needle, the CBCM circuitry and S-parameter test structures.

horizontal plate-based capacitors exhibit a smaller TC_C. This can be caused by the type of capacitor, or by the fact that the vertical distances between plates are over two times larger than the horizontal distances between the plates of the comb-type of caps (a few hundred nms).

The sensivitity of the capacitors for point stress is also shown in Table I, where '0' denotes an effect below 150 ppm (our measurement resolution). For capacitors with a noticable effect, this is in the order of 200 ppm–1000 ppm. The front-end capacitor, despite its small size and position below the back-end stack, is sensitive to point pressure from above (from, e.g., fillers in the package), but the horizontal plates higher in the back-end stack are most sensitive, as expected.

Applying 500N of plane force on an M3M4 plate capacitor in a plastic package, shifts up to about 1500 ppm occur. About 500 ppm of residual shift remains after force release, which disappears only after heating, e.g. after applying 150 °C air for a few minutes. The front-end gate capacitor shows a shift of approximately 400 ppm under plane force, without significant hysteresis.

Our measurements of temperature coefficients and mechanical stress sensitivity cannot be directly related to each other, as the mechanical stress is only applied in one direction, while thermomechanical stress is applied in all directions. Nonetheless, our results highlight the impact of stress on capacitance and provide valuable insights for designing capacitors with low TC_C and reduced sensitivity to external mechanical stress.

Our work aims at extremely thermo-mechanical insensitive capacitances for highly accurate frequency references. These systems require single-digit ppm accuracy values and low and precise TC_Cs that remain stable over lifetime, typically after a single one-temperature trim [6]. This paper indicates that even for TC_C– and mechanical-stress–optimized capacitors, wafer scale trimming before packaging may be insufficiently accurate for high performance over the full product lifetime, that packaged ICs should be trimmed individually for extreme accuracy numbers over PVT and lifetime.

Table I
MEASURED CAPACITORS WITH SPECIFICS, CAPACITANCE AND TC_C AT $f = 1.0\,GHz$.

Name	Layers	Type	Capacitance* [fF]	TCC [ppm/°C]	Pressure sens. to point stress**	Main dielectric(s)	Area [μm^2]	Metal usage [%]
PDK Gate	Front-end	H-Plate	488	-97	++	Gate oxide	33	N/A
Comb Fingers	M1	V-Plate+Fringe	611	27	N/A	FTEOS	3030	50
Comb Fingers	M2	V-Plate+Fringe	554	20	0	FTEOS	3030	50
Comb Fingers	M3	V-Plate+Fringe	666	20	0	FTEOS	3030	50
Comb Fingers	M4	V-Plate+Fringe	597	8	0	TEOS	2560	50
Comb "Plate"	M2M3	H-Plate	214	13	0	FTEOS	3060	50
Comb "Plate"	M3M4	H-Plate	219	-21	+++++	TEOS	3060	50
Plates	M2M3M4	H-Plate	641	1	0	FTEOS&TEOS	6240	65
Small plates	M2M3M4	H-Plate	700	0	+	FTEOS&TEOS	5740	72
PDK Ref	M1M2M3M4	Fringe	631	13	0	FTEOS&TEOS	670	51

* values at T=25 °C. ** '0' denotes a sensitivity below the measurement resolution.

VI. CONCLUSIONS

A number of very accurate reference systems in CMOS rely (among others) on the stability of capacitances. The most stable capacitors can be realized in the back-end. Assuming a production trim at a single temperature, the most important stability metrics are the capacitance's sensitivity to temperature changes and the sensitivity to external (possibly thermally induced) stress. We report temperature coefficients of a variety of capacitances realized in a commercial CMOS technology. Moreover, we measured sensitivities to point stress as well as a plane stress for some capacitors. Within our measurement accuracy, we can set an upper limit to the sensitivity of several capacitors. For large plane stress on a plastic package, hysteresis was observed. This finding suggests package stress (over lifetime and temperature) may influence even highly accurate back-end capacitors and care should be taken when trimming accurate circuits in factory.

VII. ACKNOWLEDGMENTS

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