# A 0.05mm$^2$ 18.5-to-38.6GHz Injection-Locked Frequency Multiplier Incorporating Injection-Spur-Isolation FTL and Single-Transformer Quad-Mode VCO Achieving –121.7dBc/Hz PN$_{@1MHz}$ in 55nm CMOS

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***Abstract*—A compact mm-wave injection-locked frequency multiplier (ILFM) integrates the quad-mode VCO in a single transformer. The quad-mode operation benefits not only expanded locking range but also the increasing output power. The injection-spur-isolation frequency tracking loop keeps the VCO with a time-invariant impedance that reduces the injection spur significantly. Prototyped in 55nm CMOS, our ILFM gains a PN$_{@1MHz}$ of –121.7dBc/Hz at 24GHz carrier with an injection spur of –39.3dBc. The ILFM covers a locking range of 70.4% from 18.5 to 38.6GHz with mere 0.05mm$^2$.**

***Keywords*—Injection-locked frequency multiplier (ILFM), single transformer, quad-mode VCO, locking range, injection-spur-isolation, output power, frequency tracking loop.**

## I. Introduction

Local oscillators (LOs) with ultra-low phase noise (PN) and wide frequency-tuning range (FTR) spanning from RF to mm-wave frequencies are required for 5G+ multiband wireless radios using dense modulation. In order to reduce the PLL operating frequency by N times (N, frequency multiplication factor), the ILFM exhibits the potential to lower the PN and widen the FTR of the mm-wave LO. It is a momentous challenge for the mm-wave ILFM to pursue low PN, wider spectrum coverage and large output power simultaneously. [1] utilized an injection-current boosting (ICB) and 6$^{th}$-order transformer for locking-range extension. Yet, the 6$^{th}$-order resonator implements the wide-range 0° phase response at the cost of low output impedance, penalizing the output power (Fig. 1 top). To improve the locking range while sustaining an adequate output power, frequency-tracking loops (FTLs) for calibration have been presented. [2] showed an envelope detector to enable the FTL operating at low frequency. Yet, it could not maintain the excellent jitter performance due to the frequency drift between $f_{VCO}$ and $N \cdot f_{inj}$. [3] implemented an ultra-low power FTL to achieve a real-time frequency tracking. Yet, the extra GHz-range quadrature-pulse generation incurs considerable power consumption. Besides, the sampling phase detector (PD) associated with the time-variant VCO loading impedance results in a large injection spur (Fig. 1 middle). Finally, both [2] and [3] suffer from a narrow locking range due to the single-mode VCO.

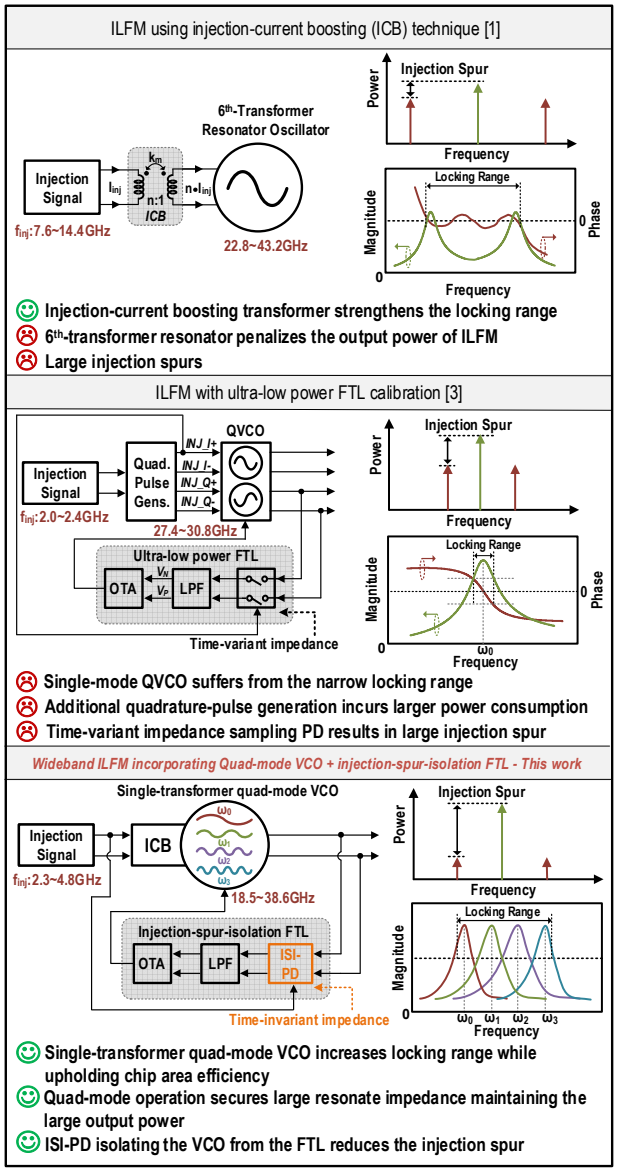



Fig. 1. Conceptual diagrams and key features of the existing and proposed ILFMs.

## II. Proposed Wideband ILFM

### A. Working principle of the ILFM

To acquire low PN, low injection spur and wide locking range, while ensuring small area footprint and adequate output power, this paper reports a mm-wave ILFM featuring a single-transformer quad-mode VCO + injection-spur-isolation FTL (ISI-FTL) (Fig. 1 bottom). Fig. 2 depicts the simplified schematic and working principle of our wideband mm-wave ILFM. The pure sine-wave injection signals $INJ_N$ and $INJ_P$ are routed to the ICB transformer that feeds out the strengthening harmonic injection current into the quad-mode VCO. Since the superior jitter filtering nature of injection locking could be maintained only if the free-running VCO frequency ($f_{VCO}$) is consistent with the $N \cdot f_{inj}$, the frequency-tracking loop is essential to sustain the frequency alignment

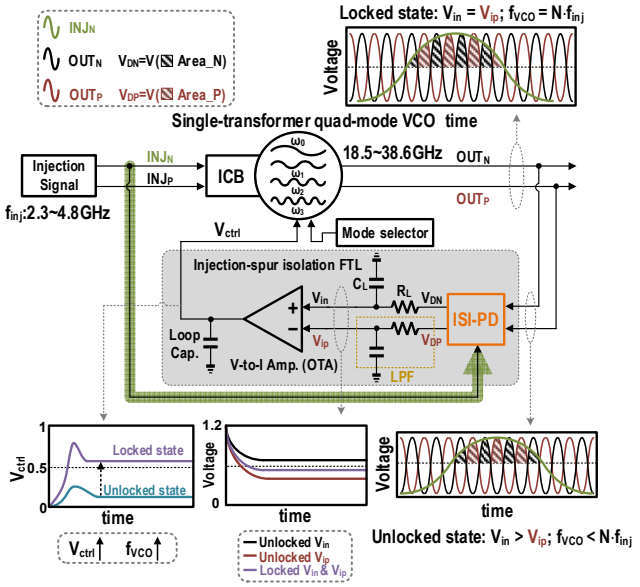



Fig. 2. Block diagram and working principle of the proposed ILFM.

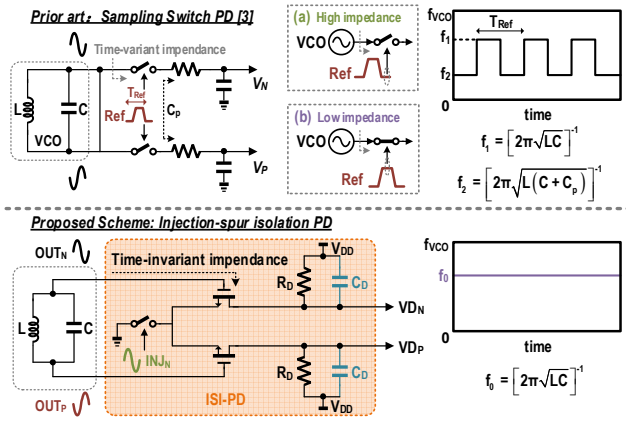



Fig. 3. Injection spur analysis of prior sampling PD and proposed ISI-PD

cross PVT. When $f_{VCO}$ deviates from N·$f_{inj}$, the phase relationship between $INJ_N$ and $OUT_{N(P)}$ would be distorted instantaneously, and the $INJ_N$ approaches either $OUT_N$ or $OUT_P$. The proposed ISI-FTL compares the overlapped area of $INJ_N$ & $OUT_N$ (Area_N) and $INJ_N$ & $OUT_P$ (Area_P) that indicates the frequency difference between $f_{VCO}$ and N·$f_{inj}$. When $f_{VCO}$ is lower than N·$f_{inj}$, the ISI-PD outputs $V_{DN}$ will be higher than $V_{DP}$. The cascade low-pass RC-filters extract the DC voltages $V_{in}$ and $V_{ip}$. Then, the V-to-I amplifier charges the loop capacitor to tune up the $V_{ctrl}$. Ultimately, the ILFM will return back to the locking state.

### *B. Injection-Spur-Isolation Analysis*

The time-variant impedance loading in VCO sampling process and charge-injection effect may induce a large injection spur in ILFM. Fig. 3 shows the prior sampling-switch PD (SS-PD) [3] and the proposed ISI-PD. For the SS-PD, the VCO is routed to the drain terminals of the switching transistors that would modulate the VCO frequency periodically, leading to a considerable output injection spur. On the contrary, the proposed ISI-PD links VCO with the gate terminals, which secures a constant loading regardless of the switching state [4]. Hence, the unmodulated $f_{VCO}$ aids in achieving a low injection spur. During the sampling process (Fig. 4), the injection charge $\Delta Q_1$ ($\Delta Q_3$) from the injection switch feeds back to the VCO tank ($\Delta Q_{tank}$

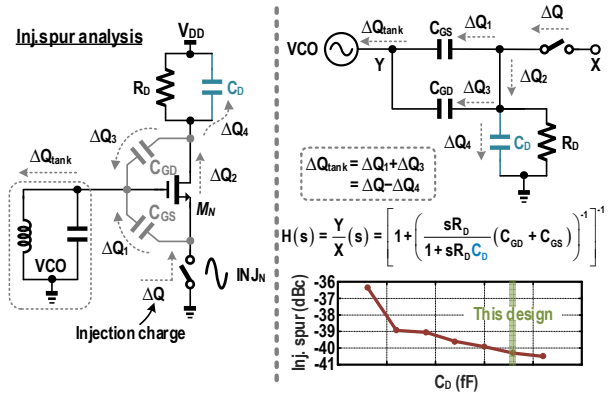



Fig. 4. Injection spur analysis of proposed ISI-PD and design consideration of $C_D$.

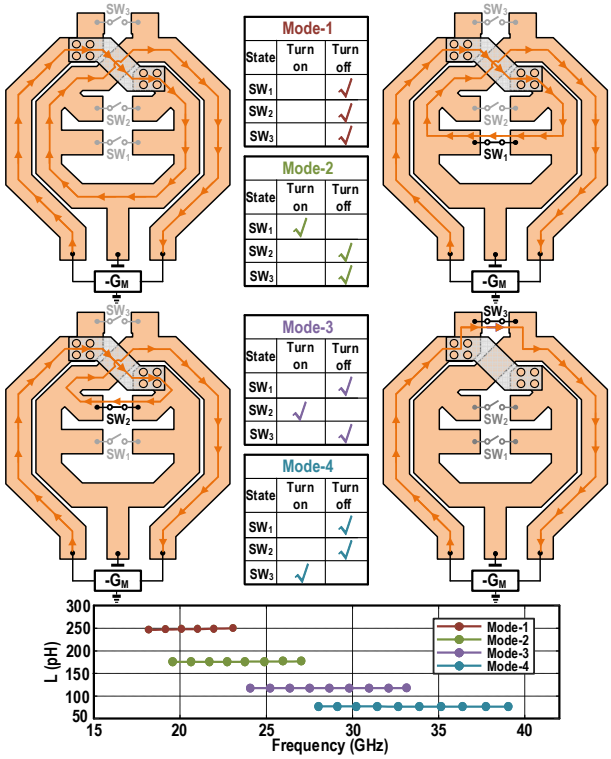



Fig. 5. Transformer configuration of proposed quad-mode VCO with simulated effective inductance in four operating modes.

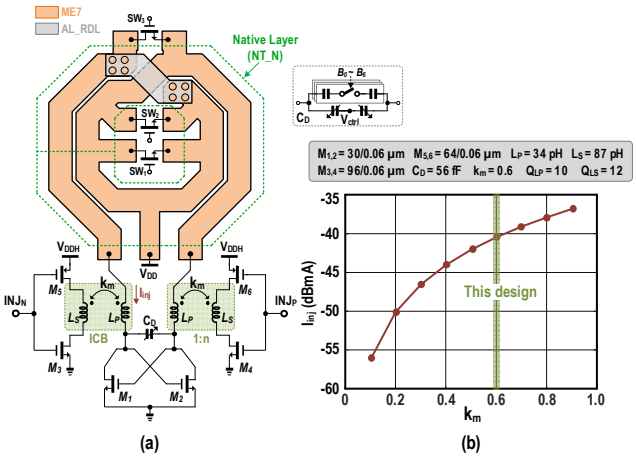



Fig. 6. (a) Detailed layout and schematic of ILFM and (b) design consideration of $k_m$.

=$\Delta Q_1$+$\Delta Q_3$) through the parasitic capacitor $C_{GS}$ ($C_{GD}$) of transistor $M_N$. The additional periodical $\Delta Q_{tank}$ injection to

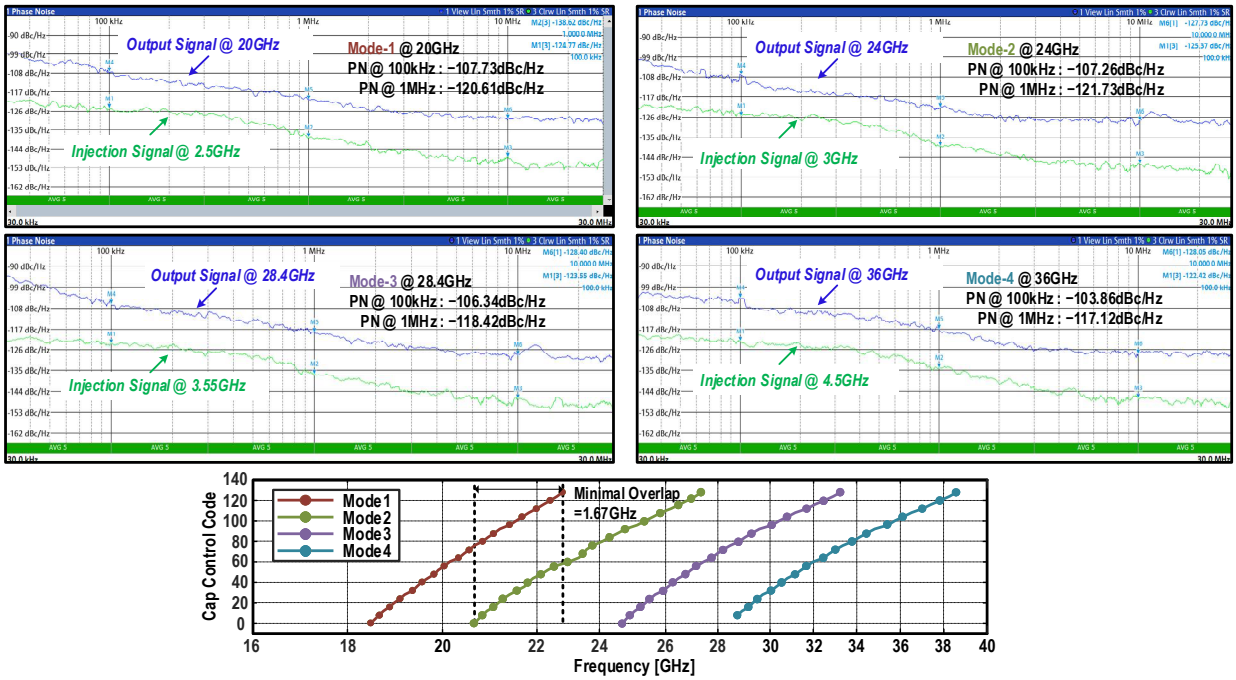
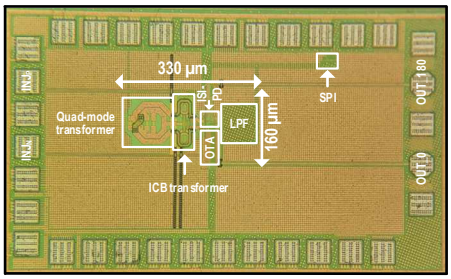



Fig. 7. Measured PN profiles and frequency-tuning range of the proposed mm-wave ILFM.




| Power Consumption (mW) | |
|---|---|
| VCO | 9.5 |
| ISI-PD | 0.46 |
| OTA | 0.62 |
| Total | 10.58 |

Fig. 8. Die photograph and power breakdown.

VCO penalizes the injection spur [5]. Verified by transfer-function calculation and simulation, a large sampling $C_D$ aids in reducing the $\Delta Q_{tank}$ delivery. To alleviate the charge-injection-induced spur and consider the locking failure with an excessive $C_D$, a large $C_D$ (36fF) is chosen, suggested by simulation.

## C. Quad-Mode VCO

Since the mm-wave ILFM suffers from the trade-offs between PN and locking range, we innovate a quad-mode VCO to expand the locking range while implementing a single transformer to uphold a compact chip area. Fig. 5 displays the four operating modes. The lowest operating frequency (mode-1) is excited by turning off the switches $SW_{1-3}$. Thus, the tank current would flow through the entire coils, which contributes to the largest effective inductance ($L_{eff1}$=247pH). For the mode-2, the switching-on $SW_1$ gathering the tank current in the upper internal coils reduces the tank inductance to $L_{eff2}$=176pH. Similar case is performed in the mode-3 with the $SW_2$ on and the $SW_{1,3}$ off, the shortened current flowing paths lessen the tank inductance to $L_{eff3}$=117pH. Finally, by turning the $SW_3$ on and the $SW_{1,2}$ off, the internal coils will be bypassed resulting in the minimum inductance $L_{eff4}$=76pH. Thus, our VCO can oscillate at the highest frequency (mode- 4). Fig. 6 (a) details the layout and schematic of proposed ILFM except the ISI-FTL. The n:1 ICB transformer in series with the quad-mode transformer aids in boosting the injection

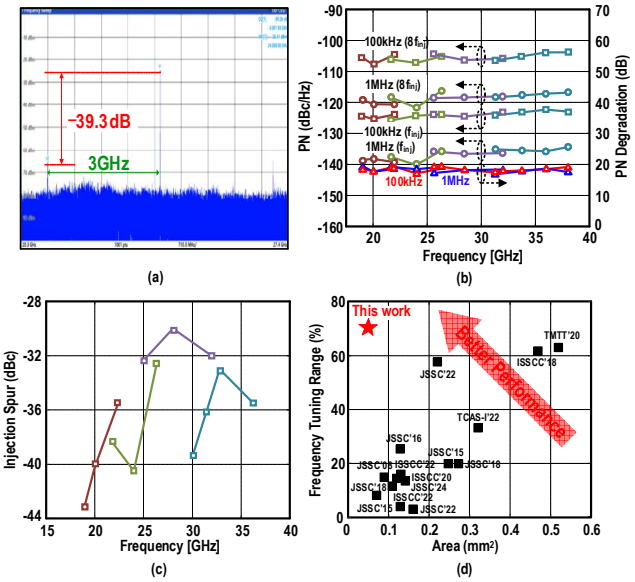



Fig. 9. Measurements: (a) Output spectrum of 24GHz. (b) PN and PN degradation and (c) injection spurs across the entire locking range. (d) frequency tuning range and area comparison.

current $I_{inj}$. As simulated in Fig. 6(b), when the coupling factor $k_m$ of the ICB transformer varies from 0.1 to 0.9, the $I_{inj}$ benefits a 30% improvement from –50 to –35dBmA. To cover a wide tuning range with a small $k_{VCO}$ for stability consideration, 7-bit ($B_0$~$B_6$) switched-capacitor arrays together with a pair of varactors are added at the drain terminals of the $-G_M$ transistors $M_{1,2}$. The native layer (NT_N) is exploited to surround the quad-mode transformer except for the inner space where we placed the $SW_{1,2}$.

## III. Measurement Results

The proposed mm-wave wideband ILFM fabricated in 55nm CMOS dissipates 9.8 to 11.8mW with a core area of 0.05mm$^2$ (Fig. 8). Fig. 7 plots the measured PN profiles of four operating modes (at 20, 24, 28.4, and 36GHz), ranging from –121.7 to –116.2dBc/Hz at a 1MHz offset,

TABLE I
MEASUREMENT COMPARISON WITH THE RECENT MM-WAVE ILFMS.

| | This Work | ISSCC'17 [3] | ISSCC'16 [2] | JSSC'24 [6] | JSSC'22[7] | ISSCC'18 [1] |
|---|---|---|---|---|---|---|
| Key Technique | **Single-transformer quad-mode VCO + reference-spur isolation FTL** | Single-mode QVCO + phase-deviation averaging FTL | Single-mode QVCO + envelop-detection FTL | Class-F VCO + frequency tripler w/o calibration | Reconfigurable ×2/×3 freq. multiplier w/o calibration | Injection-current boosting frequency tripler w/o calibration |
| Process | **55nm** | 65nm | 130nm | 65nm | 55nm | 40nm |
| Injection Freq.(GHz) | **2.3 ~ 4.8** | 2 ~ 2.4 | 8.8 ~ 10 | 8 ~ 9.4 | 4.5 ~ 9.6 | 7.6 ~ 14.4 |
| Output Freq. (GHz) | **18.5 ~ 38.6** | 27.4 ~ 30.8 | 26.5 ~ 29.7 | 24 ~ 28 | 20.7 ~ 43.8 | 22.8 ~43.2 |
| Bandwidth (BW) | **70.4%** | 11.7% | 11.4% | 15.4% | 71.6% | 61.8% |
| Inj. Spur (dBc) | **- 42.9 ~ - 30** | - 30[&] | - 33.1[&] | N/A | - 27.8 | - 15[&] |
| PN (dBc/Hz) @ 100kHz ?f | **- 107.7 ~ - 103.8** | - 93.1 @ 29.3G | - 88.5[&] @ 26.5G | - 111.9 @ 26.3G | - 109.6 @ 39G | - 94.6 @ 39G |
| PN (dBc/Hz) @ 1MHz ?f | **- 121.7 ~ - 116.2** | - 115.6 @ 29.3G | - 106.8 @ 26.5G | - 113.8 @ 26.3G | - 114.6 @ 39G | - 111.8 @ 39G |
| $Jitter_{RMS}@f_{OUT}$ [Integ. Range] | **32.5fs @28.4G [30k-30M]** | 86fs @29.3G [1k-100M] | 174fs @26.54G [100k-100M] | 37.1fs @26.3G [10k-30M] | N/A | N/A |
| Power (mW) | **9.8 ~ 11.8** | 24.3 | 23.2 | 12.1 | 9.6 | 19.8 |
| FoM (dB) @ 1MHz | **275 ~ 288.1** | 261.8 | 255.3 | N/A | 272.9 | 253.6 |
| $FoM_A$ (dB) @ 1MHz | **288 ~ 301.1** | 271.3 | 265.7 | N/A | 284.5 | 256.8 |
| Die Area ($mm^2$) | **0.05** | 0.11 | 0.09 | 0.14 | 0.07 | 0.47 |

$FoM = |PN/1Hz| + 10\log_{10}(f_0^2 \times BW(\%)/10^9 \div P_{DC}(mW)) - Inj.\ Spur$ $FoM_A = FoM + 10\log_{10}(1mm^2/A)$ [&] Estimated from the figures in reference

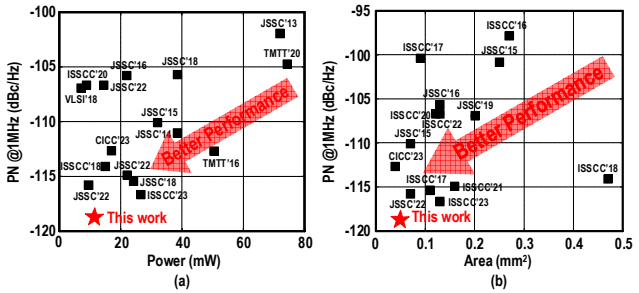


Fig. 10. $PN_{@1MHz}$ survey versus (a) power and (b) chip area.

respectively. The measured PN profile is consistent with the theoretical calculation staying around 20log(8)dB = 18dB. As shown in Fig. 7 (bottom), the wideband continuous locking range of 70.4% is achieved with a 1.7GHz minimal overlap between the adjacent modes, and the 4 bands vary from [18.5 to 22.5], [20.8 to 26.8], [24.6 to 32.7] and [28.6 to 38.6] GHz, respectively. Fig. 9 (a) illustrates the injection spur of –39.3dBc when locked at 24GHz. Thanks to the ISI-FTL, the injection spur throughout the whole locking range varies from –42.9 to –30dBc, as shown in Fig. 9 (c).

Compared with [2-3] and [1, 6-7], this work exhibits a superior FoM ($FoM_A$) that is at least 2.6dB (3.5dB) better. As surveyed in Fig. 9 (d) and Fig. 10, this work demonstrates the wide locking range and the best-in-class $PN_{@1MHz}$ (normalized to a 30GHz carrier) with a compact core area of mere $0.05mm^2$.

## VI. CONCLUSION

This work reports a compact mm-wave injection-locked frequency multiplier that integrates the injection-spur-isolation frequency tracking loop and single-transformer quad-mode VCO for injection spur reduction and locking range extension. Validated in 55nm CMOS, the ILFM achieves a $PN_{@1MHz}$ of –121.7 ~ –116.2dBc/Hz with a low injection spur of –42.9 ~ –30dBc across the locking range of 70.4% from 18.5 to 38.6GHz. Thanks to the single-transformer quad-mode VCO, the core area of the ILFM is mere $0.05mm^2$.


## ACKNOWLEDGMENT

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