A 0.16 ppm/°C Voltage Reference with On-Chip Self-Heating and Highly Flexible Auto-Calibration High-Order Compensation

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***Abstract*—This paper introduces a sub-ppm/°C voltage reference that supports pseudo two-point calibration at room temperature by incorporating a self-heating control loop, thereby reducing calibration costs. The design also features a highly flexible auto-calibration high-order compensation system that is resilient to model inaccuracies and process variations. Measurement results from 40 chips in 180 nm BCD and 55 nm CMOS show TC of 0.46 and 0.16 ppm/°C (best) and 1.47 and 1.41 ppm/°C (average).**

Keywords—Voltage Reference, On-Chip Self-Heating, Auto-Calibration High-Order Compensation

I. Introduction

The reference voltage has a significant impact on the performance and accuracy of analog systems [1]. The accuracy of the reference voltage is critical, as any instability or error will directly affect the measurement results of the ADC. For a 12-bit ADC with a 100 °C operating temperature range, the temperature coefficient (TC) of the reference voltage must be less than 1.22 ppm/°C to achieve an error of less than 1/2 LSB. The traditional first-order compensation scheme, based on the base-emitter voltage (V_{BE}) and ΔV_{BE} of the BJT, has difficulty meeting the stringent requirements of high-precision applications.

High order compensation is designed in [2] based on temperature independent (TI) current biased BJT and [3] based on strong inversion MOSFETs. However, the temperature characteristics of these compensation terms do not exactly match V_{BE}, resulting in poorer compensation across a wider temperature range. Piecewise compensation schemes enable the application of different appropriate compensation in different temperature ranges, making them highly effective in achieving a low TC over wide temperature ranges. For example, [4] used five-piece linear compensation to achieve 0.9 ppm/°C. However, fabrication process limitations introduce errors that can degrade the TC, and these errors must be corrected by calibration, which can increase production costs by 10-20% [5].

Fig. 1 shows the cost and precision of different calibration schemes. High and low temperature calibration (e.g., -40 °C and 125 °C) offers high accuracy, but requires special equipment and takes a long time to calibrate, making it expensive. Room temperature and high temperature calibration (e.g., 27 °C and 125 °C) require external heating at a moderate cost. However, the high-order temperature error of the V_{REF} causes the low-temperature range curve to disperse.

To reduce calibration costs while maintaining a low TC, this paper introduces three techniques: 1) an on-chip integrated heater with closed-loop temperature control, which enables equivalent two-point calibration at room temperature at a low cost; 2) a highly flexible compensation scheme that corrects high-order errors caused by inaccurate models, thereby achieving a low TC; 3) automatic calibration for high-order compensation to mitigate the impact of process variations and mismatches on the effectiveness of high-order compensation.

The proposed bandgap voltage references were fabricated and verified across two distinct technology nodes: standard 55 nm CMOS and 180 nm BCD processes. The best TC for 40 chips was 0.16 ppm/°C (with an average of 1.41 ppm/°C) for the 55 nm CMOS, and 0.45 ppm/°C (with an average of 1.47 ppm/°C) for the 180 nm BCD, over a temperature range of -40 °C to 125 °C.

This paper is organized as follows: Section II presents the proposed voltage reference. Section III presents the measurement results. Section IV concludes this paper.

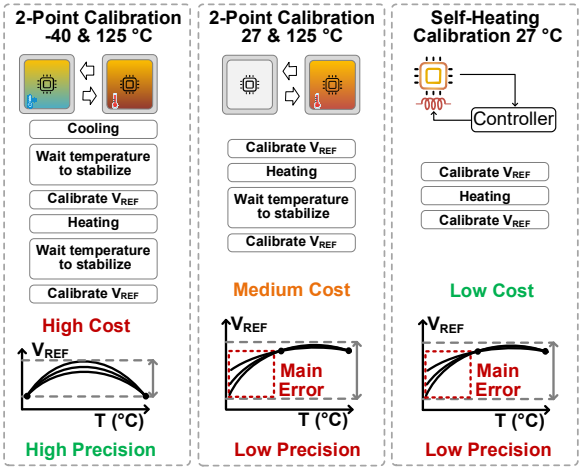

Fig. 1. Calibration Solutions for Voltage Reference.

II. Proposed Voltage Reference

Fig. 2 illustrates the concept of the proposed on-chip self-heating and auto-calibration voltage reference. It includes the bandgap core, resistor strings, a highly flexible high-order compensation module (I_2), and a self-heating calibrated first-order compensation module (I_1). The bandgap core generates V_{BG}, which is then divided resistively to produce a reference voltage, V_{REF}, of 1 V. The self-heating loop regulates the temperature and uses I_1 to correct the first-order error. More importantly, it also automatically calibrates the high-order compensation based on the results of the first-order calibration.

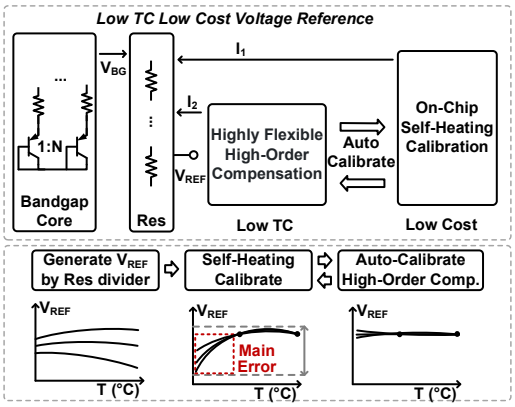

Fig. 2. Proposed Low TC Low Cost Voltage Reference Concepts.

A. On-Chip Heater

Fig. 3 depicts the circuit architecture of the proposed voltage reference, which mainly consists of four components: the bandgap core, the voltage-divider resistor string, the first-order compensation current I_1 for self-heating calibration, and the highly flexible and automatically adjustable high-order compensation current I_2.

To minimize the calibration cost, an on-chip integrated heater fabricated with Metal-3 is used to cover the area that requires heating.

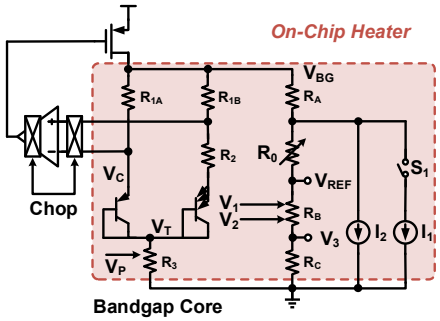

Fig. 3. Proposed Circuit Diagram for Voltage Reference and Self-Heating Calibration.

The closed-loop temperature control system monitors the change in ΔV_{BE} through a feedback loop, using it as an intrinsic temperature sensor within the bandgap core. The control loop automatically adjusts the heater current to maintain the desired target temperature, ensuring a stable and calibrated on-chip environment.

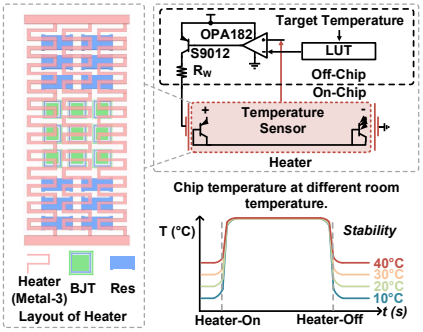

Fig. 4. On-Chip Heater and Self-Heating Control Loop.

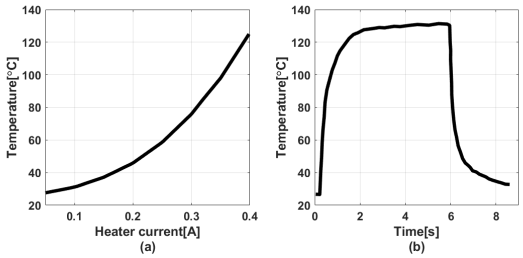

Fig. 5. The Relationship between Heater Current, Heating Time and Chip Temperature.

Fig. 5(a) presents the relationship between the current of the on-chip heater and the chip temperature. Under room-temperature conditions, to maintain the chip at 125 °C, a heating current of 0.4 A is needed. This heating current is only active during the calibration period and no current is consumed during normal operation.

Fig. 5(b) indicates that when the self-heating control loop is activated at room temperature, the chip temperature stabilizes at 125 °C within 1.8 seconds. Since the time required for the chip to heat up and cool down is extremely short, it is possible to perform multiple heating and cooling cycles within a short time span to calibrate the output voltage.

B. Self-Heating Calibration

To adjust only the temperature coefficient during self-heating calibration without affecting the output voltage value, the first-order calibration circuit shown in Fig. 6 was used [5]. The CTAT current, I_C, is generated by the combination of V_C and R_C, while the PTAT current, I_P, is generated by V_T and R_P. These two currents flow through a 7-bit current DAC(D_1), then pass through the resistor string to produce the first-order compensation current, I_1=I_P-I_C.

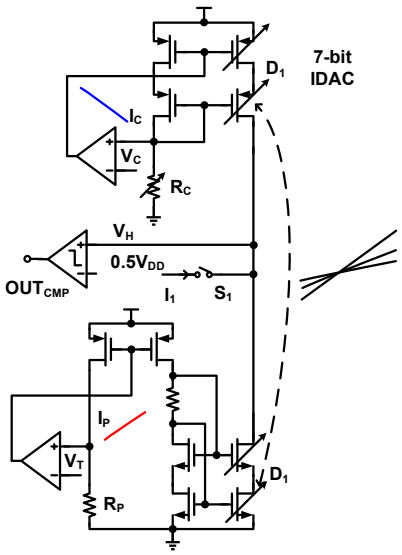

Fig. 6. The First-Order Compensation Circuit in Self-Heating Calibration.

The self-heating calibration procedure, outlined in Fig. 7, consists of four steps:

1) At temperature T_1 (e.g., 27 °C), adjust R_C to ensure that the first-order compensation current, I_1, is 0 A.

2) Also at T_1, adjust R_0 so that the output voltage, V_{REF}, is 1 V.

3) Increase the chip temperature to T_2 (e.g., 125 °C) using an on-chip heater and closed-loop temperature control system. Adjust the IDAC D_1 to maintain V_{REF} at 1 V.

4) Finally, based on the value of D_1, automatically calibrate the high-order compensation.

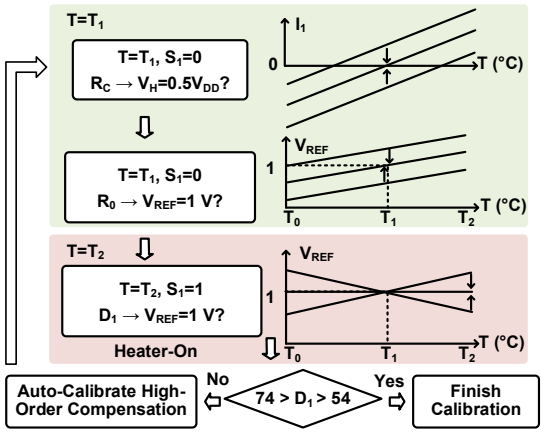

Fig. 7. Self-Heating Calibration Flow.

C. *Auto-Calibration High-Order Compensation*

In order to mitigate the errors in the low-temperature region, it is essential to introduce a high-order compensation scheme. High-order compensation can be realized by utilizing MOSFETs operating in the sub-threshold region. However, due to factors such as model inaccuracies and process variations, achieving sub-ppm/°C accuracy is challenging [6-8].

To overcome these challenges, this paper presents a novel auto-calibration high-order compensation approach that enhances flexibility and accuracy. The system consists of three key components: 1) a voltage divider with V_{REF} and resistor strings to generate temperature-independent (TI) voltages $V_1/V_2/V_3$; 2) an operational amplifier and R_H to generate TI currents (I_0) that bias the differential pair; and 3) two differential pairs operating in the subthreshold region.

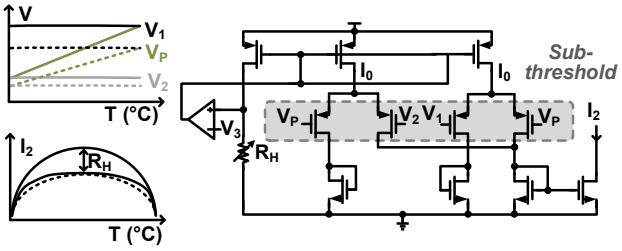

Fig. 8. Highly Flexible High-Order Compensation.

The high-order compensation current, I_2, can be highly flexibly adjusted by modifying V_P, V_1, and V_2, allowing for compensation of errors resulting from model inaccuracies. To mitigate amplitude errors in I_2 caused by process variations and component mismatches, the value of R_H is automatically adjusted during calibration.

For instance, in a 7-bit IDAC, when high-order compensation is properly applied, the value of D_1 will range from 54 to 74 (based on test results, this value is normally 64±10). If high-order compensation is insufficient, as shown on the left side of Fig. 9, additional IDAC are activated to equalize the voltages at both room and high temperatures, causing D_1 to exceed 74. In this case, R_H should be reduced to enhance high-order compensation. Conversely, if D_1 falls below 54, as shown on the right side of Fig. 9, it indicates excessive compensation, and R_H should be increased to reduce the high-order compensation.

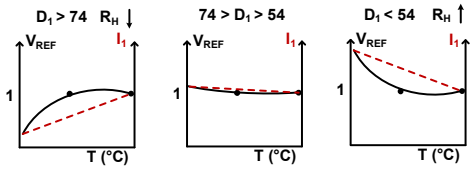

Fig. 9. Auto-Calibrate High-Order Compensation.

III. Measurement Results

The proposed bandgap voltage reference was fabricated using both 55 nm CMOS and 180 nm BCD processes to validate the effectiveness of the highly flexible auto-calibration high-order compensation. Fig. 10 and Fig. 11 present the output voltage versus temperature curves after two-point chamber calibration and self-heating calibration for both the 180 nm BCD and 55 nm CMOS processes.

Following the application of the proposed self-heating calibration process, the TC for 40 chips (20 from each process) tested across the -40 °C to 125 °C range are as follows: for the 55 nm CMOS process, the best and average TC are 0.16 ppm/°C and 1.41 ppm/°C, respectively; for the 180 nm BCD process, the best and average TC are 0.45 ppm/°C and 1.47 ppm/°C, respectively. These results are comparable to those obtained through chamber calibration, demonstrating the effectiveness of the proposed cost-efficient calibration method.

Table I compares the proposed voltage reference with existing state-of-the-art low TC references. By utilizing a highly flexible auto-calibration high-order compensation scheme and a self-heating-based calibration process, this work achieves a superior temperature coefficient.

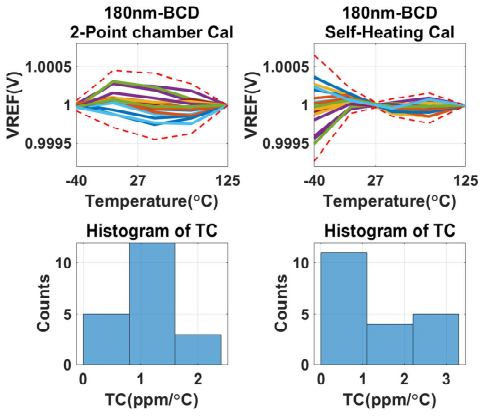

Fig. 10. Normalized Temperature Characteristics of 180nm BCD Reference Voltage.

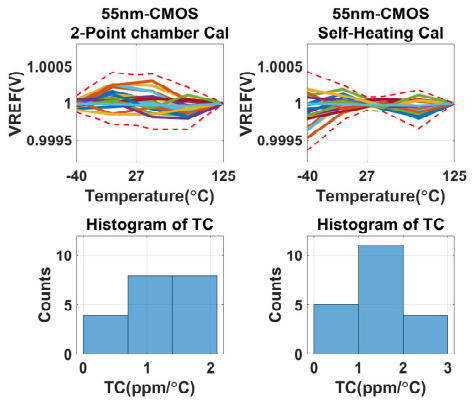

Fig. 11. Normalized Temperature Characteristics of 55nm CMOS Reference Voltage.

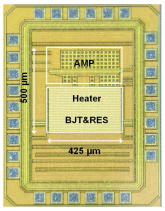

Fig. 12. Diephoto of 180nm BCD Voltage Reference.

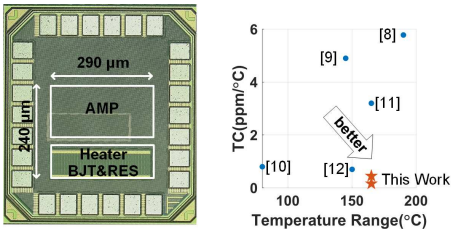

Fig. 13. Diephoto of 55nm CMOS Voltage Reference.

TABLE I. PERFORMANCE SUMMARY AND COMPARISON TABLE

		This Work		JSSC 2021[11]	JSSC 2021[8]	ISSCC 2019[9]	TCAS-I 2021[10]	TCAS-I 2022[12]
Process		55nm CMOS	180nm BCD	180nm CMOS	130nm CMOS	12nm CMOS	65nm CMOS	180nm CMOS
Supply Voltage (V)		2.5	5	1.8	3.3	0.7	2.5~3.6	3.2~3.7
Current(µA)		34	29.6	17	120	9.83	40*	409
Output Voltage (V)		1		1.1419	1.16	0.207	1.1458	2.14
Temperature Range (°C)		-40~125		-40~125	-40~150	-20~125	0~80	-25~125
TC (ppm /°C)	Best	0.16	0.45	3.2	5.78	4.9	0.8~0.87	0.7
	Avg	1.41	1.47	4.3	8.75	40.51		1.18
	Worst	2.87	3.25	5.5	13.5	82.3		1.56
Measure Samples		20	20	18	7	35	3	6
Curvature Correction		Yes		Yes	Yes	No	Yes	Yes
Trimming		Self-Heating 27°C		1-Point 27°C	No	No	3-Point 0/27/80°C	3-Point -25/27/100°C
PSRR (dB)		68 @DC	90 @DC	76 @DC	82 @10Hz	N/A	N/A	63.4 @10Hz
Area (mm²)		0.07	0.2	0.38	0.08	0.065	0.006*	0.256

*: Power and area of off-chip op-amps are not included.

IV. CONCLUSION

To maintain the high accuracy of the reference voltage while reducing calibration costs, this work proposes three techniques. First, through the integration of an on-chip self-heater and a closed-loop temperature control circuit, low-cost pseudo two-point calibration is achieved without the need for external heating and temperature control equipment. Second, a highly flexible and adjustable high-order compensation scheme is designed to address the challenge that the compensation result is affected by the model accuracy. Third, the high-order compensation is automatically calibrated according to the magnitude of the first-order compensation. This solves the problem of large low-temperature errors in two-point calibration at room and high temperatures. Based on these techniques, temperature coefficients as low as 0.16 ppm/°C have been realized at two different process nodes over the temperature range -40 °C to 125 °C.

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