A 7.7-to-10.1GHz Transformer-Based VCO Achieving 194.7dBc/Hz FoM and 206dBc/Hz FoM_A with Third-Harmonic Impedance Expansion and Dual Common-Mode Resonances in 65nm CMOS

Kaitian Yang and Xiaolong Liu
School of Microelectronics, Southern University of Science and Technology, Shenzhen, China
Email: liuxl@sustech.edu.cn

***Abstract*—This paper presents a transformer-based voltage-controlled oscillator (VCO) with low power consumption, low phase noise, and high figure-of-merit (FoM). By leveraging a triple-coil transformer, the tank achieves differential-mode (DM) resonance expansion at the third-harmonic frequency while simultaneously enabling dual common-mode (CM) resonances at the second- and fourth-harmonic frequencies, significantly suppressing noise upconversion. Fabricated in a 65-nm CMOS process, the proposed VCO achieves a frequency tuning range of 27% from 7.7 to 10.1 GHz, with phase noise ranging from -137 to -132 dBc/Hz at a 10-MHz offset. It consumes only 1.2 mW from a 0.9 V supply. The peak FoM is 194.7 dBc/Hz, and the core area is 0.074 mm², resulting in a peak FoM_A of 206 dBc/Hz.**

Keywords—CMOS, harmonic shaping, transformer, voltage-controlled oscillator (VCO), differential-mode, common-mode, noise self-cancellation, low power.

I. Introduction

Voltage-controlled oscillators (VCOs) with low power consumption, compact size, and low phase noise are essential for high-speed wireless communication and radar systems in mobile and portable devices. Recent studies have extensively explored the use of common-mode (CM) and/or third-harmonic differential-mode (DM) resonances to significantly enhance the phase noise performance and figure-of-merit (FoM) of *LC* VCOs [1]–[8]. As shown in Fig. 1(a), the resonant tank inherently provides a CM resonance at twice the oscillation frequency (F_O) without requiring an additional tail inductor [1], [2]. However, this approach may suffer from a low CM quality factor (Q_{CM}) due to the unavoidable magnetic-flux cancellation. Moreover, it necessitates manual harmonic tuning with single-ended capacitors to maintain optimal performance over a wide tuning range, which can further degrade the tank's Q. To eliminate the need for manual harmonic tuning, a head resonator was introduced to broaden the CM resonance bandwidth [3], as shown in Fig. 1(b). However, this head filter occupies an additional area and cannot fully prevent noise current injection from the ground. To address the issue of CM noise injected from the power supply and ground [4], a dual-core class-F_{23} VCO with CM noise self-cancellation and isolation was proposed in [5] [Fig. 1(c)]. Nevertheless, the second-harmonic CM and third-harmonic DM resonances remain narrowband without manual harmonic tuning, reducing the effectiveness of flicker and white noise suppression. Consequently, existing harmonic-shaping VCOs either suffer from degraded CM Q_{CM} [1], [2], require an additional filtering inductor [3], [4], exhibit misaligned harmonic resonances over a wide frequency tuning range [5], or experience CM noise coupling [1]–[4].

To overcome these challenges, this paper presents a triple-coil transformer-based complementary VCO featuring third-harmonic impedance expansion, dual CM resonances, and CM noise self-cancellation, as shown in Fig. 1(d). The proposed VCO achieves a peak FoM of 194.7 dBc/Hz at a 10-MHz offset, a peak FoM_A of 206 dBc/Hz, and a frequency tuning range of 27% from 7.7 to 10.1 GHz with a low power consumption of 1.2 mW.

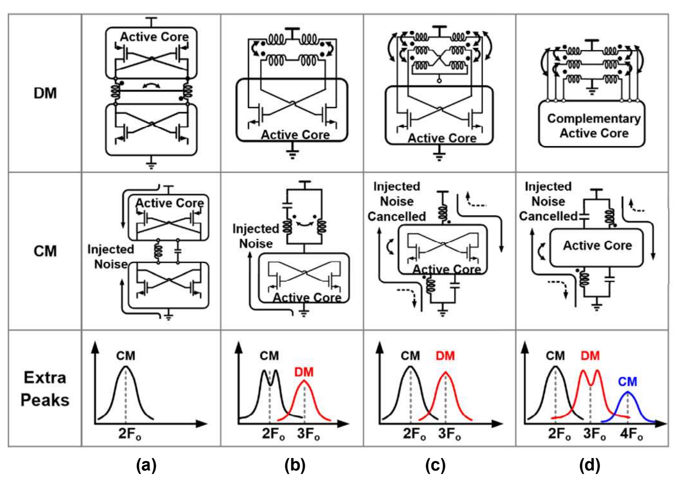

Fig. 1. Simplified DM and CM equivalent circuits and high harmonic impedance responses of reported harmonic shaping oscillators. (a) Implicit CM resonance technique [1], [2], (b) CM resonance expansion with class-F operation [3], (c) class-F_{23} operation with injected noise cancellation [5], and (d) the proposed work with DM expansion, dual CM resonances, and injected noise cancellation.

II. Proposed Transformer-Based Complementary VCO with DM Expansion, Dual CM Resonances, and Injected Noise Cancellation

Fig. 2(a) shows the proposed triple-coil transformer under DM excitation. In the DM, two coupled third-harmonic resonators ($L_{2,dm}C_2$, $L_{3,dm}C_3$) are placed at the sources of the PMOS and NMOS cross-coupled pairs. By carefully selecting the design parameters and ensuring that $2L_{2,dm}(C_{2,fix} + 0.5C_{2,cm}) \approx L_{3,dm}(C_{3,fix} + 0.5C_{3,cm})$, two peaks can be achieved at around $3F_O$, as shown in Fig. 2(b). The simulated impedance exceeds 120 Ω across a fractional bandwidth greater than 30% at the center frequency of $3F_O$, providing robust protection against third harmonic misalignment due to process, voltage, and temperature (PVT) variations. Additionally, the primary coil $L_{1,dm}$ is positioned at the gate terminals of the transistors and resonates at F_O with the differential capacitor array C_1, as illustrated in Fig. 2(a).

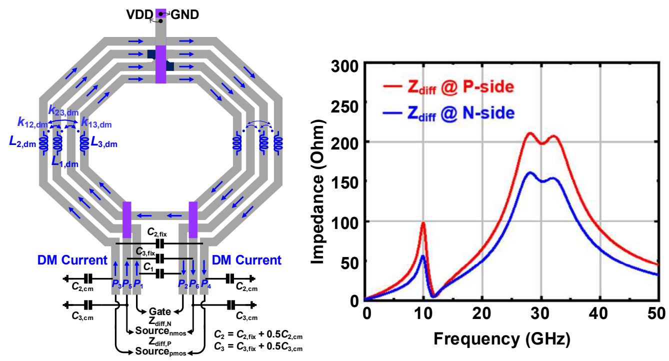

Fig. 2. (a) Proposed triple-coil transformer in DM excitation and (b) simulated impedance in DM seen from the sources nodes.

In the CM, the $L_{1,cm}$ is effectively disabled, and C_1 is not visible due to the absence of a CM point. This configuration allows the two coupled resonators ($L_{2,cm}C_{2,cm}$, $L_{3,cm}C_{3,cm}$) to reconfigure and create dual CM resonances at $2F_O$ and $4F_O$, as demonstrated in Fig. 3(a). Note that the additional fourth-harmonic CM resonance further improves the phase noise performance of the VCO [7], [9]. Unlike conventional implicit CM designs with low Q_{CM} [1], [2], the proposed implicit approach breaks the trade-off between the Q_{CM} and the mutual coupling coefficient K of the resonant coils, which previously followed the relationship $Q_{CM} \propto 1–K$. This enables a high Q_{CM} without requiring a low K (which would necessitate a larger inductor area) or an unrealistically small amount of CM capacitance [1]. The simulated Q_{CM} for $L_{2,cm}$ and $L_{3,cm}$ is 22 and 18 at $2F_O$, respectively, comparable to their DM Q_{DM} values.

Furthermore, the proposed topology intrinsically blocks injected CM noise coupling from VDD and GND to the gates of the cross-coupled pairs. As shown in Fig. 3(b), by introducing nearly equal and opposite magnetic coupling between $L_{2,cm}/L_{3,cm}$ and $L_{1,dm}$, the injected CM noise can be effectively self-canceled, nullifying its impact on the gate. The EM simulation results show that $K_{1dm,2cm} \approx |K_{1dm,3cm}| < 0.003$ at $2F_O$, suggesting that the injected CM noise is isolated.

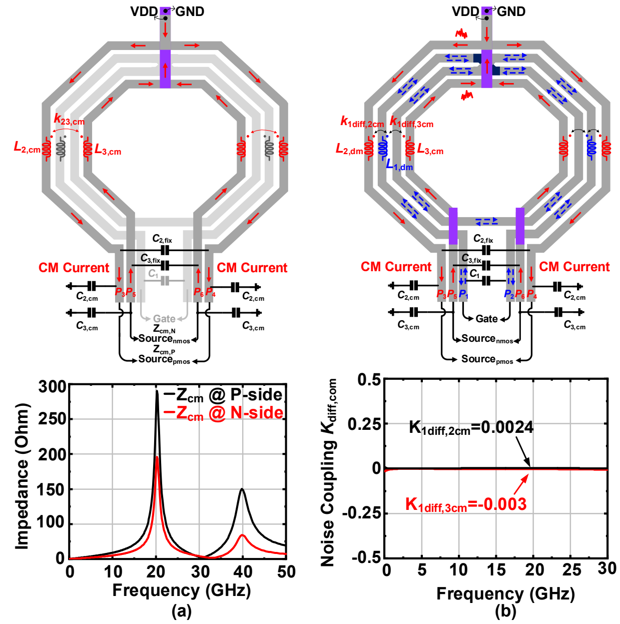

Fig. 3. (a) Proposed triple-coil transformer in CM excitation and (b) CM injected noise cancellation scheme.

III. Circuit Implementation

Fig. 4 details the schematic of the proposed triple-coil transformer-based complementary VCO. A 4-bit differential switched-capacitor array (SCA) and a pair of varactors are connected to the gates for fundamental frequency tuning. Meanwhile, a pair of differential fixed capacitors and two 4-bit single-ended switched capacitors are strategically placed at the sources of the PMOS and NMOS transistors to support the DM and CM harmonic resonances while minimizing tank Q degradation. By tuning the single-ended capacitors in conjunction with the SCA, both the impedance-expansion DM resonance and the dual CM resonances can shift with F_O, thus simultaneously aligning the first-to-second/fourth and first-to-third harmonic resonances.

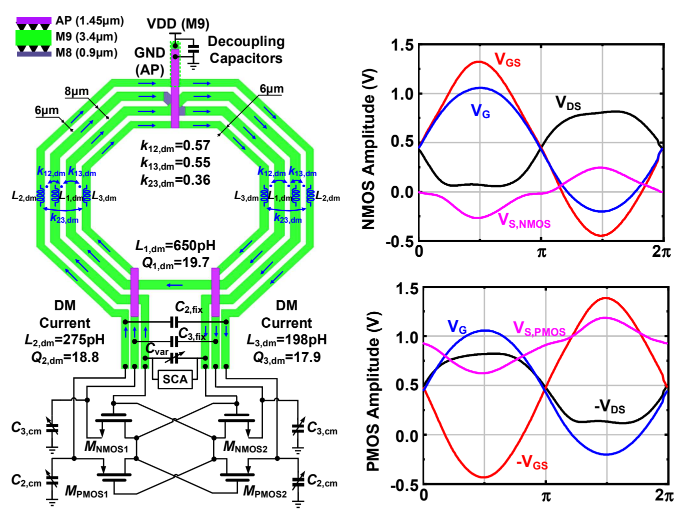

Fig. 4. Detail schematic and transformer layout of the proposed VCO and the simulated voltage waveforms.

The proposed triple-coil transformer is mainly implemented using the 3.4 μm thick M9 layer to maximize the Q, with cross-connection utilizing the 1.45 μm thick AP and 0.9 μm thick M8 layers. The EM simulated DM inductances and Qs are: $L_{1,dm}$ = 650 pH, $Q_{1,dm}$ = 19.7, $L_{2,dm}$ = 275 pH, $Q_{2,dm}$ = 18.8, and $L_{3,dm}$ = 198 pH, $Q_{3,dm}$ = 17.9. Benefiting from the complementary topology, the implementation of the triple-coil transformer stacks the center taps of VDD (M9) and GND (AP), and the CM current return path is minimized through the decoupling and parasitic capacitors, as illustrated in Fig. 4, ensuring the maintenance of a low flicker noise corner.

In addition, with transformer feedback [10], the V_{GS} swing is significantly boosted, improving power efficiency. As shown in Fig. 4, the gate voltage V_G can oscillate above the supply voltage, while the out-of-phase source voltage V_S can swing below the ground potential, effectively boosting the V_{GS} oscillation amplitude by around 40%. Furthermore, the rise and fall edges of the V_{GS} waveform become sharper due to the introduction of the $3F_O$ harmonic at the source, reducing noise contributions from the active transistors. The transient simulation results show that the source voltage V_S contains an F_O and $3F_O$ components of 160 mV and 30 mV, respectively.

The simulated impulse sensitivity functions (ISFs) and effective ISFs of the NMOS and PMOS transistors are plotted in Fig. 5, demonstrating that CM and DM harmonic shaping creates a zero region in the ISF, corresponding to the flat region of V_{DS}. The effective ISF exhibits good symmetry, resulting in a low DC value, thereby preventing flicker noise upconversion.

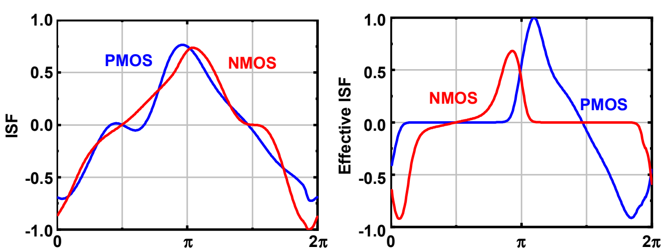

Fig. 5. Simulated ISFs and effective ISFs of NMOS and PMOS transistors.

IV. MEASUREMENT RESULTS

The proposed transformer-based VCO was designed and fabricated in a 65-nm CMOS process. Fig. 6 shows the die micrograph. The core area is 0.074 mm^2, excluding the decoupling capacitors and pads, and the power consumption is 1.2 mW with a supply voltage of 0.9 V. The open drain buffer is used for testing.

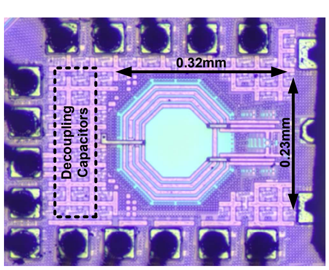

Fig. 6. Chip micrograph.

Fig. 7 illustrates the measured phase noise at the minimum and maximum carrier frequencies. At 7.7 GHz and 10.1 GHz, the measured phase noise is -115.1 dBc/Hz and -110.7 dBc/Hz at 1-MHz offset, while the 10-MHz offset phase noise is -137 dBc/Hz and -132 dBc/Hz, respectively. Fig. 8 presents the measured phase noise and FoM across the whole frequency tuning range. The FoM ranges from 191.3 to 194.7 dBc/Hz at a 10-MHz offset. The measured frequency tuning range is 27%, from 7.7 to 10.1 GHz, corresponding to a peak FoM_T of 203.3 dBc/Hz.

As shown in Fig. 9, the measured flicker noise corner varies from 180 to 250 kHz across the entire frequency tuning range. With the proposed compact triple-coil transformer, the VCO achieves a peak FoM_A of 206 dBc/Hz.

Table I summarizes the performance of the proposed VCO and compares it with recently reported state-of-the-art oscillators. The proposed VCO demonstrates low power consumption, a wider frequency tuning range, high FoM and better FoM_A, and a small flicker noise corner.

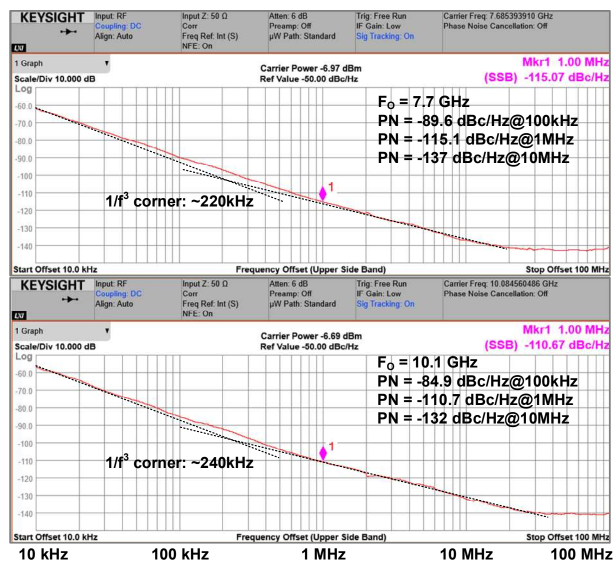

Fig. 7. Measured phase noise at 7.7 GHz and 10.1 GHz.

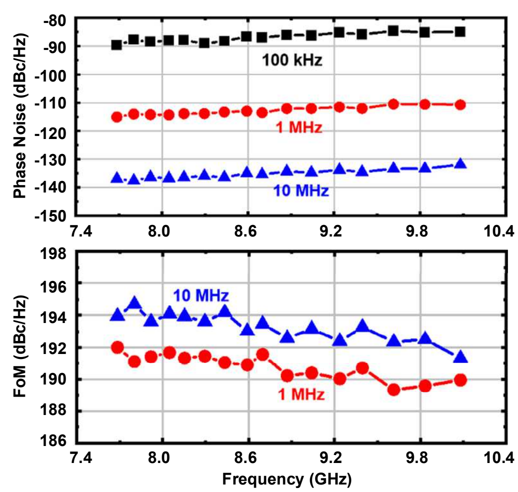

Fig. 8. Measured phase noise and FoM across the frequency tuning range.

TABLE I. PERFORMANCE COMPARISON WITH THE STATE-OF-THE-ART *LC* OSCILLATORS

Reference		JSSC'16 [2]	JSSC'15 [4]	ESSERC'24 [11]	ISSCC'25 [12]	VLSI'23 [13]	This work
Technology		40nm CMOS	55nm CMOS	65nm CMOS	28nm CMOS	28nm CMOS	65nm CMOS
Frequency (GHz)		5.4 to 7	7.4 to 8.4	9.9 to 11.8	8.1 to 9.9	7.8 to 9.4	7.7 to 10.1
Tuning Range		25%	13%	17.5%	20%	18.1%	27%
Supply (V)		1	1.5	1.2	0.9	0.58	0.9
Power (mW)		12	6.3	12.7	33.5	0.64	1.2
PN (dBc/Hz)	1M	-126.7	-118[(a)]	-121.4	-128.7	-103.8	-115.1 to -110.5
	10M	-146.7	145.5	-141.6	-146.3	-127.2	-137 to -132
FoM[(b)] (dBc/Hz)	1M	190.5	188.1	190.4	191.4	183.6	192 to 189.3
	10M	190.5	195.6	190.6	189	187	194.7 to 191.3
FoM_T[(c)] (dBc/Hz)	1M	198.5	190.3	195.2	197.4	188.8	200.6 to 197.9
	10M	198.5	197.8	195.5	195	192.2	203.3 to 199.9
FoM_A[(d)] (dBc/Hz)	1M	199.4	195.3	199.6	199.4	197.3	203.3 to 200.6
	10M	199.4	202.8	199.8	197	200.7	206 to 202.6
$1/f^3$ Corner (kHz)		60 to 130	200 to 400	240	320 to 380	600	180 to 250
Core Area (mm^2)		0.13	0.19	0.12	0.16	0.043	0.074

(a) Estimated from plots (b) $FoM = -PN + 20\log_{10}(f_{LO}/\Delta f) - 10\log_{10}(P_{DC}/1mW)$
(c) $FoM_T = FoM + 20\log_{10}(TR/10\%)$ (d) $FoM_A = FoM + 10\log_{10}(1mm^2/Area)$

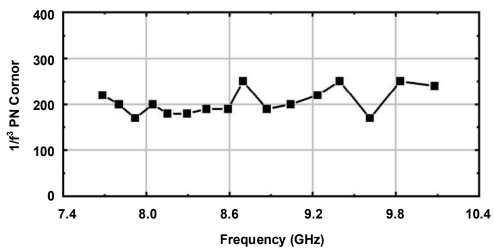

Fig. 9. Measured flicker noise corner across the frequency tuning range.

V. CONCLUSION

In this paper, a low-power, low-phase-noise, transformer-based VCO is presented. The proposed compact triple-coil transformer enables DM third harmonic impedance expansion and dual CM resonances, effectively improving the phase noise performance. Implemented in a 65-nm CMOS process, the proposed VCO achieves a frequency tuning range of 27% from 7.7 to 10.1 GHz, a peak FoM of 194.7 dBc/Hz, and a peak FoM_A of 206 dBc/Hz, while consuming only 1.2 mW and occupying a small core area of 0.074 mm^2.

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