On the Unusual HCI Degradation of Nanoscale Back-Bias RFETs in 22nm FDSOI Technology

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***Abstract*—In this study, we experimentally evaluated the hot carrier injection (HCI) degradation in Reconfigurable FETs (RFETs) processed on a 22 nm FDSOI technology, and identified the underlying mechanism. The HCI behavior in these devices differs from traditional MOSFETs: RFETs primarily show a threshold voltage (V_{th}) shift instead of the on-current (I_{on}) degradation typical in MOSFETs. In addition, the reversed-biased source Schottky junction in RFETs places the peak electric field at the source side, whereas in MOSFETs the highest field is near the drain. The source side degradation was confirmed by measuring transfer characteristics in both forward and reverse modes before and after hot-carrier stress. Furthermore, the V_{th} shift follows a power-law dependence on stress time, with a stress-voltage-dependent time exponent. These findings help in developing suitable degradation models and in understanding the aging effects of polymorphic circuits built from RFETs.**

***Index Terms*—Reconfigurable Field Effect Transistors, 22nm FDSOI, Hot Carrier Injection, Schottky Barrier Transistor.**

I. Introduction

As CMOS scaling approaches physical and economic constraints, researchers are increasingly exploring next-generation device architectures to extend functionality beyond conventional CMOS. RFETs are one type of emerging Schottky barrier FETs (SB-FETs) [1] that can function as either n-type or p-type. Their polarity can be dynamically programmed and their versatile operation modes enable new levels of functionality in integrated circuits. In digital, RFETs provide logic functions with fewer transistors, enabling polymorphic logic gates, ultra-compact designs, and new hardware security schemes [2]–[5]. In the analog domain, their non-linear behavior, coming from their ambipolar nature can be exploited for applications such as frequency doublers [6], [7]. Moreover, RFETs can be integrated into existing FDSOI technology without the need for extra critical process steps or materials [6], [8], [9].

For circuit designers, device reliability is as important as initial performance. RFETs inherit many of the same reliability concerns as CMOS transistors but, at the same time, the reconfigurability may bring new concerns [10]. A critical aspect in circuits is hot carrier injection (HCI), which occurs when high-energy carriers damage the gate oxide layer, gradually causing performance loss over time. The hot carrier effect in SB-FETs has previously been utilized in charge-trapping memory cells, where hot carriers enable localized programming and erasing operations within the charge-trapping layer [11]–[15]. Despite this existing knowledge about the hot carrier effects in SB-FETs, it has not been throughout investigated yet how the device parameters age in response to a prolonged hot carrier exposure.

In this study, we focus on examining the effect of hot carrier stress on Back-Bias RFETs (BB-RFETs) fabricated on industrial 22 nm FDSOI hardware. The electrical characteristics of the BB-RFET are introduced first, followed by the HCI measurement procedure. The unique impact of HCI degradation on BB-RFETs is then presented and analyzed, emphasizing the differences between RFETs and traditional MOSFETs. Finally, the time- and voltage-dependences of the hot electron degradation are discussed.

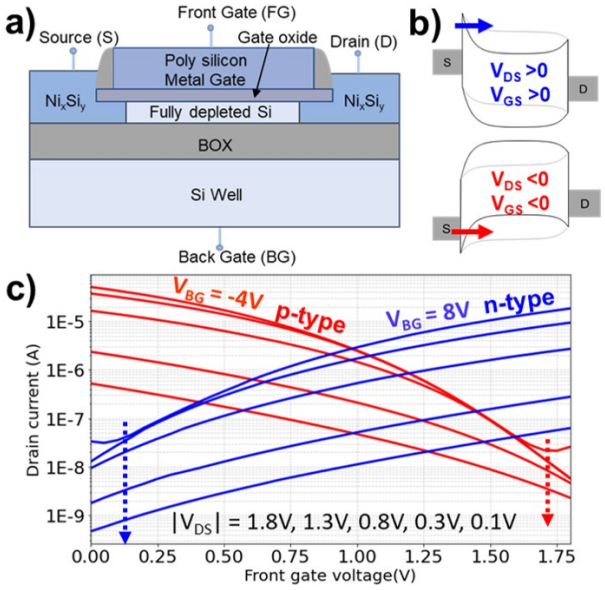

Fig. 1. a) Schematic drawing of the BB-RFET in FDSOI technology. b) Band diagram of n-type conduction (blue) and p-type conduction (red), the grey line stands for the off-state and the black line corresponds to the on-state. c) Full set of measured transfer characteristics with multiple $|V_{DS}|$.

II. Device characteristics

BB-RFETs are four-terminal devices with Schottky contacts at the metal-semiconductor interfaces (Fig. 1). Both the front and back gates extend over these contacts, giving electrostatic control of the Schottky barriers and the entire channel energy bands. Carriers from the metal can either cross the barrier by thermionic emission or tunnel through it, with tunneling dominating the drive current, which depends on the barrier

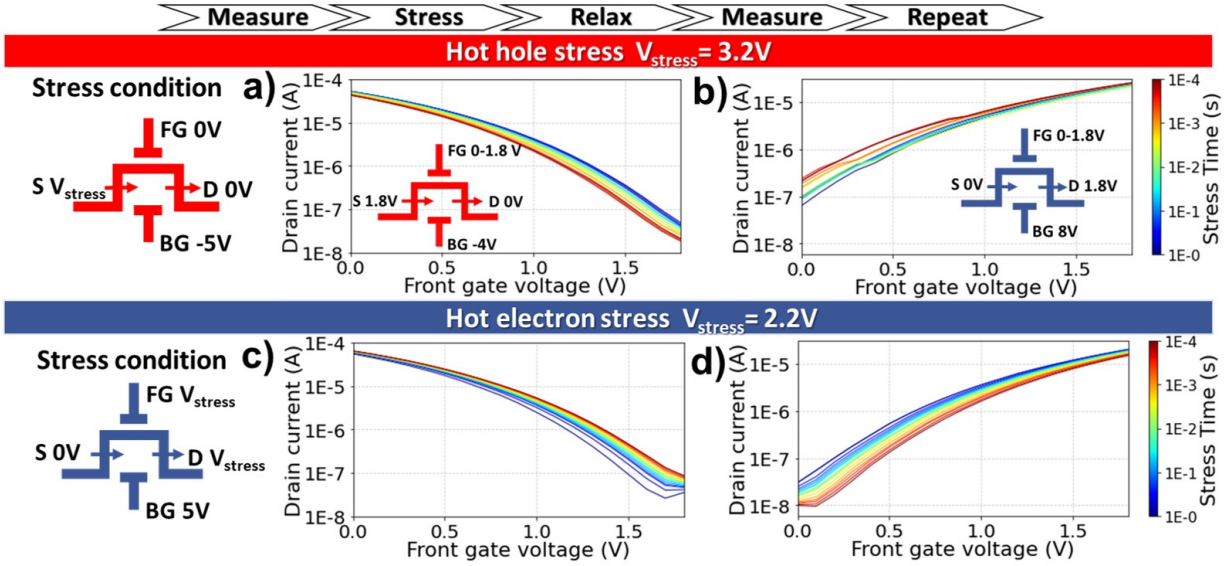

Fig. 2. Reliability assessment of BB-RFET showing the effects of hot hole stress on the transfer curves in (a) p-conduction mode and (b) n-conduction mode, and the effects of hot electron stress on the transfer cures in (c) n-conduction mode and (d) p-conduction mode. The flow chart at the top illustrates the HCI measurement routine. The insets show the stressing and measurement bias conditions, and the arrow indicates the carrier direction.

width. The current magnitude is jointly controlled through both the front and back gate voltages by tuning the Schottky barrier width. In the BB-RFET, the back gate is utilized as the polarity gate by pre-bending the channel energy bands. This allows the front gate to sweep the transistor purely in either p-mode or n-mode within a common operating voltage range (e.g., 0 V to 1.8 V). When a negative back bias is applied along with a negative V_{DS}, the source-side Schottky barrier becomes thin enough for hole tunneling at moderate front-gate voltages, while the barrier on the drain side blocks electrons. As a result, the device operates as a p-type transistor. Conversely, a positive back bias lowers the source-side barrier for electrons and raises it for holes, enabling n-type operation over the same front-gate voltage range [6], [7].

III. Reliability Analysis

Different to standard MOSFETs, RFETs can conduct both electrons and holes, so a single stress mode can affect both types of carriers. This gives rise to four possible degradation-measurement scenarios: (1) hole-channel response under hot-hole stress, (2) electron-channel response under hot-hole stress, (3) electron-channel response under hot-electron stress, and (4) hole-channel response under hot-electron stress. In this work, hot carrier degradation is analyzed at stress conditions where V_{GS}=V_{DS} following the channel hot carrier (CHC) model [16]. We set V_{BG} to 5 V to ensure a high stress current, thereby targeting a pronounced HCI effect. The measurement procedure starts with evaluating the fresh device in both p-mode and n-mode with quasi-stationary measurement. Next, we apply stress voltages in either p-mode or n-mode. After each stress phase, we include a 10-second relaxation period to allow parasitic transient bias temperature instability (BTI) effects to recover, ensuring we only measure the permanent component of HCI-induced degradation. After relaxation, the device is measured again in both modes. This stress–relax–measure cycle is repeated with increasing stress durations (five data points per time decade) until reaching a total stress time of 10^4 seconds.

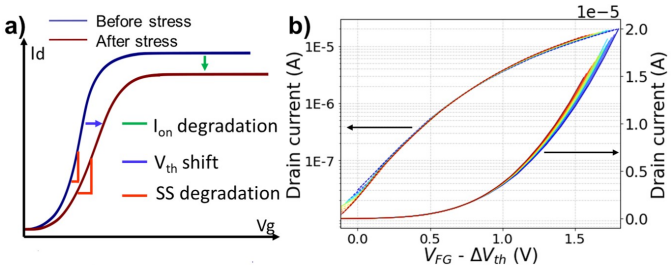

Fig. 3. a) Theoretical effects of hot carrier stress on transfer curves. b) V_{th} corrected plot of measured transfer curves after hot electron stress.

Fig. 2 shows how hot carrier degradation differs for hole and electron mode (p-type and n-type curves) after the same stress mode in a BB-RFET. Under hot-electron stress, the electron channel suffers stronger degradation: the entire transfer curve shifts toward a higher threshold voltage over time. Conversely, the hole channel shows less significant degradation in the opposite direction. Under hot-hole stress, the p-type curves exhibit clear degradation, shifting toward higher V_{th}, whereas the n-type curve shifts in the opposite direction. These opposing shifts arise because each hot carrier type creates different charge trapping in the oxide, while hole and electron conduction respond inversely to the same oxide charges. Under high electric fields, energetic (“hot”) electrons can gain enough energy to induce impact ionization, creating additional electron−hole pairs. These hot electrons may then be injected into the gate oxide or generate interface traps at the Si/SiO_2 interface. Both mechanisms introduce charges that

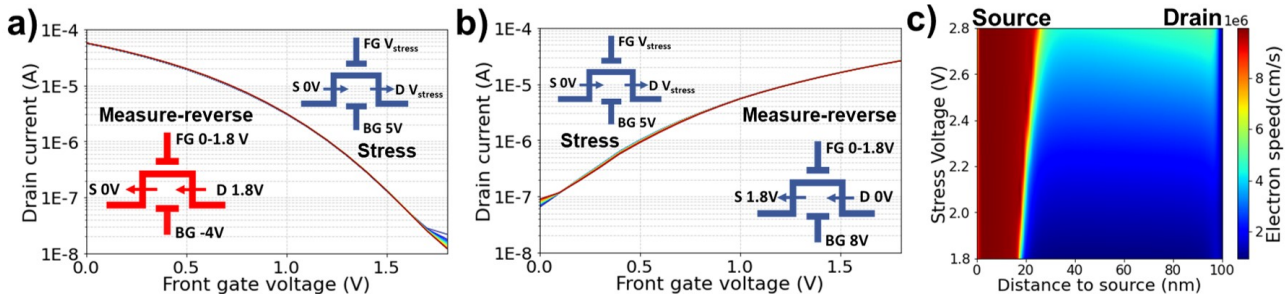

Fig. 4. Transfer characteristics of a) p-type type and b) n-type mode of the BB-RFETs measured in reverse direction as compared to the applied hot-electron stress voltage of 2.2 V. c) Simulated electron speed (color scale) versus distance from the source and stress voltage extracted from a fitted TCAD model.

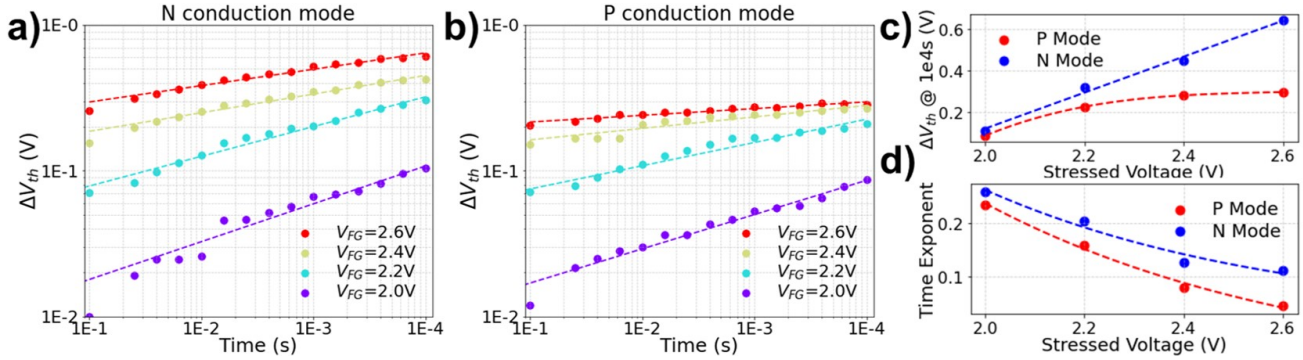

Fig. 5. Hot-electron-induced threshold voltage shifts (ΔV_{th}) as a function of stress time for a) n-type conduction and b) p-type conduction under different stress voltages. The slope of the linear fits denotes the time exponent. Extracted c) threshold voltage shifts (ΔV_{th}) at t=10^4s and d) time exponents.

shift the electron conduction threshold upward over time while shifting the hole conduction threshold in the other direction. Hot holes similarly shift their own conduction mode to higher thresholds but move the electron channel the opposite way. Notably, hot-hole stress requires a higher stress voltage (3.2 V) to achieve comparable degradation as hot-electron stress (2.2V). This observation is in line with the literature, that found the degradation from hot holes to be less significant than from hot electrons, mainly because holes have lower mobility and energy, shorter mean-free path, reduced ionization rate and a higher oxide barrier (4.5 eV) for injection [17].

Fig. 3a) shows three typical hot-carrier-induced degradation effects on transistor transfer curves: (1) V_{th} shift from trapped charges in the gate oxide, (2) Subthreshold Slop (SS) stretch-out caused by interface-state generation, and (3) mobility degradation that reduces transconductance and on-current. To isolate these three effects in our results (Fig. 2d), each transfer curve is replotted against (V_{FG}-ΔV_{th}), subtracting the V_{th} shift so all curves share the same threshold voltage. Once corrected for V_{th} shifts, the curves nearly overlap (Fig. 3b), meaning that V_{th} shift is the main degradation. The small increase of the on-current and negligible subthreshold slope degradation confirm their minor roles compared to the V_{th} shift. An RFET operates differently from a standard MOSFET, causing hot-carrier degradation to behave differently. In a MOSFET, carriers flow through an inversion channel and the largest electric field is typically near the drain, resulting in drain-side hot-carrier damage. In an RFET, carriers tunnel through a reverse-biased Schottky barrier at the source, inducing a peak in the electric field that promotes a localized injection of carriers into the nearby gate oxide. [18], [19]. The oxide charges directly influence Schottky barrier gating at the source side and therefore cause a threshold-voltage shift. This results in little on-current loss because the doping-free channel in an RFET is less prone to mobility degradation. To confirm that HCI in the RFET mainly occurs near the source side, we measured the device in reverse mode. Any oxide charges or traps created by HCI are fixed near the original source region at the Si/SiO_2 interface and do not move when the measurement electrodes are swapped. In SB-FETs, charges at the drain side have a smaller impact on the transfer characteristic because the drain Schottky barrier does not strongly control carrier injection. Therefore, any HCI-induced damage should have a limited effect when we reverse the measurement direction. Indeed, the measurements show no degradation when the source and drain are reversed, supporting the idea that HCI damage occurs at the original source side. As seen in Fig. 4a) and b), the p- and n-type characteristics after hot electron stress change only slightly under the reverse measurement. This confirms that most of the damage is concentrated at the source side and indicates asymmetrical HCI damage in the RFET. TCAD simulations support this conclusion: the electron speed heatmap (Fig. 4c) shows that electrons are fastest near the source region at higher stress voltages, highlighting where hot carrier effects are most pronounced. We used hot-electron stress results to study our

HCI degradation model. The absolute threshold-voltage shift, extracted via the constant current method, serves as the indicator of HCI degradation. In Fig. 5, the V_{th} shifts are analyzed across different stress times and voltages. The data follows a power-law time dependence with nearly straight lines, suggesting constant time exponents. N-type conduction (Fig. 5a) exhibits higher magnitude shifts but steadier time exponents with voltage. In contrast, p-type conduction (Fig. 5b) shows a smaller overall shift but shows a more pronounced change in its time exponent and a different voltage dependence. Hot-electron stress impacts its own conduction mode (n-mode) more strongly compared to the opposite conduction mode (p-mode). Fig. 5c) and d) compare a single time slice (10^4s) and time exponent from Fig. 5a) and b), plotting threshold-voltage shift versus stress voltage. The n-type threshold-voltage shift rises roughly linearly with stress voltage, while the p-type shift follows a square-root trend. These findings will aid in predicting long-term parameter shifts and mitigating HCI effects during circuit operation.

IV. Conclusion

Understanding transistor reliability is essential for any circuit application. Since HCI is a dynamic process typically occurring during switching, reconfigurable devices like RFETs require attention to their hot-carrier behavior. We studied the unique HCI effect in BB-RFETs fabricated on industrial 300 mm FDSOI wafers. Unlike conventional MOSFETs, which typically show I_{on} degradation, HCI in RFETs mainly induced V_{th} shifts in the transfer curves, with negligible changes in subthreshold slope and I_{on}. Specifically, after hot-electron stress, the V_{th} shifted to higher voltages for p-channel operation and to lower voltages for n-channel operation. Conversely, after hot-hole stress, the V_{th} increased in the p-channel mode and decreased in the n-channel mode. These observations can be explained by hot-carrier generation at the source edge, where trapped charges modify the local Schottky barrier gating and consequently affect the threshold voltage. Additionally, hot-electron stress had a stronger effect than hot-hole stress, and it impacted the n-type conduction mode more significantly than the p-type conduction mode. Finally, the V_{th} shift follows a power-law dependence on stress time, with a field-dependent time exponent: larger stress voltages generally correspond to smaller exponents. These investigations on HCI effects in RFETs are critical for accurately predicting device aging and ensuring reliable performance in dynamic circuit applications.

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