A 3MHz Calibration-Free CT-DSM Achieving 102.3dB SFDR using MASH Dual Quantization

Ahmed Abdelaal*, David-Peter Wiens*, Matteo Dalla Longa†, Jonathan Ungethüm*, John G. Kauffman*, Francesco Conzatti†, Maurits Ortmanns*

*Institute of Microelectronics, University of Ulm, Ulm, Germany
†Infineon Technologies, Villach, Austria

***Abstract*—Multi-bit (MB) quantization allows Delta-Sigma Modulators (DSMs) to achieve low oversampling ratios (OSRs), improved jitter tolerance, and relaxed dynamic requirements of the loop-filter (LF) while maintaining high maximum stable amplitude (MSA). However, the nonlinearity caused by the outermost feedback digital-to-analog converters (DACs) is challenging. This work applies a Multi-stage noise SHaping (MASH) digital DSM (DDSM) in a dual quantization (DQ) continuous-time delta-sigma modulator (CT-DSM), resulting in significantly relaxed element mismatch sensitivity while eliminating the need for DAC calibration. In addition, high jitter robustness is achieved by combining MB quantization with a 4-tap finite impulse-response (FIR) filtering. Dual return-to-zero (DRZ) is introduced into the 4-tap FIR to reduce the effect of dynamic errors. Finally, the power-efficient tri-level DAC encoding is combined with a mid-tread asynchronous successive-approximation-register (A-SAR) to improve matching and noise. The prototype of the CT-DSM shows a 102.3dB spurious-free dynamic range (SFDR) in a 3MHz bandwidth. Implemented in 28nm CMOS, the CT-DSM is clocked at 120MHz and achieves a Schreier figure of merit of 170dB.**

***Index Terms*—analog-to-digital converter (ADC), continuous-time (CT), DSM, dual quantization, multibit DAC, MASH, FIR-DAC, calibration-free.**

I. Introduction

Continuous-time delta-sigma modulators (CT-DSMs) are an attractive choice for many applications, such as wireless communication systems (GSM) and IoT sensing, due to their inherent anti-aliasing filter, resistive input impedance, and high power efficiency [1]. The use of single-bit (SB) quantization has proven effective in numerous applications due to the intrinsic linearity of the corresponding digital-to-analog converter (DAC). However, it suffers from several limitations, including a reduction in maximum stable amplitude (MSA), increased susceptibility to clock jitter, dynamic errors (inter-symbol-interference (ISI)), and more demanding loop-filter (LF) requirements due to increased signal swing. Combining SB with finite impulse-response (FIR) filtering improves jitter tolerance and reduces LF requirements [2]. However, SB quantization requires larger oversampling ratio (OSR) and higher sampling frequencies, increasing power consumption and jitter sensitivity. Finally, higher-order LFs greatly affect the stability of Delta-Sigma Modulators (DSMs), and cascaded architectures require analog-digital matching [3]. Multi-bit (MB) quantization enhances MSA, reduces clock jitter sensitivity, and can achieve high resolutions with low OSR [3]. However, element mismatch in the MB DAC degrades the linearity [5]. Various linearization techniques have been proposed to tackle this issue. Methods including dynamic element-matching (DEM) and data-weighted averaging (DWA) have been utilized [6] [7]. These methods exhibit reduced effectiveness at low OSRs and may elevate switching activity, thereby exacerbating dynamic mismatches and ISI. Many foreground to background calibration methods have been introduced [8] [9]. However, calibration requires startup sequences and consumes power and chip area [10]. Dual quantization (DQ) architectures have been proposed to leverage the advantages of MB quantization while preserving the linearity of SB DAC [4] [11]. As shown in Fig. 1, [4] employs a 3b quantizer as the main quantizer of the CT-DSM, a second-order single loop (SL) digital DSM (DDSM) subsequently applies upsampling and noise shaping to transform the 3b quantizer output $Y[n]$ into a 1.5b upsampled output $Y_D[n]$. Consequently, the mismatch sensitivity in the linearity-critical DAC_3 is mitigated by employing the inherently linear 1.5b architecture [12]. However, such SL DDSM suffered from increased power consumption and sensitivity to ISI due to upsampling.

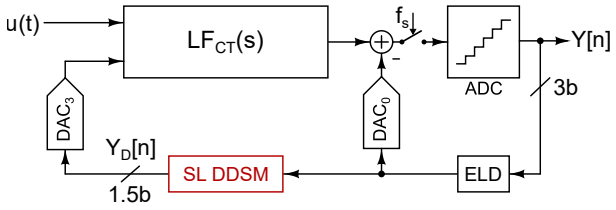

Fig. 1. CT-DSM using SL DDSM for DQ [4].

By realizing a Multi-stage noise SHaping (MASH) rather than a SL DDSM, [11] avoids upsampling of the DDSM and achieves a higher order DDSM by cascading lower order DDSMs. Although Sturdy Multi-stage noise SHaping (SMASH) circumvents the use of digital cancellation filters (DCFs) and the related digital-analog matching, it does so at the expense of a more complex LF than MASH. This work implements the first DQ CT-DSM using MASH DDSM. In order to simplify the DCFs, noise coupling (NC) is applied in the MASH DDSM. The calibration-free MB CT-DSM achieves 102.3dB linearity in a 3MHz bandwidth. Section II describes the architecture, while implementation details are

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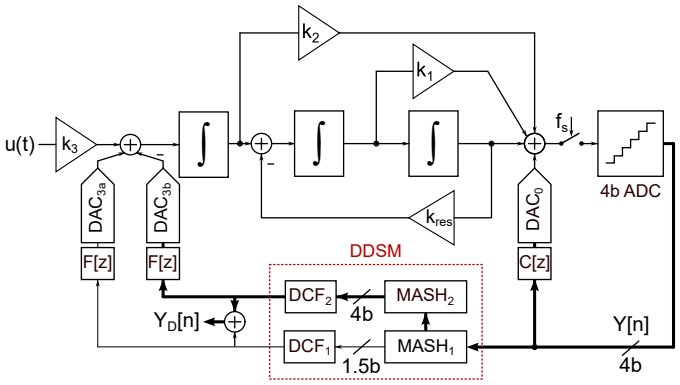

Fig. 2. Architecture of the implemented CT-DSM with MASH DDSM [11].

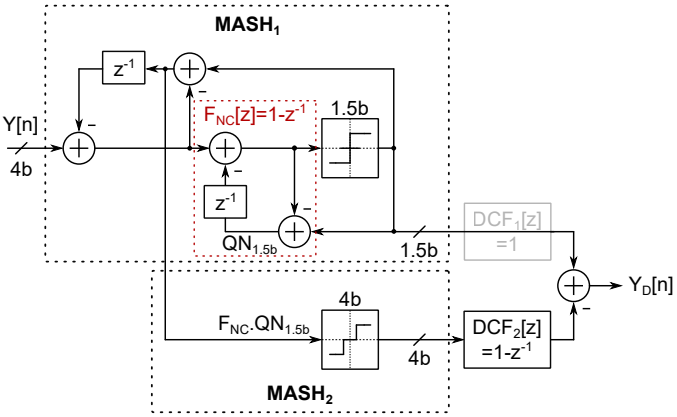

Fig. 3. 2-0 MASH DDSM with NC in error feedback topology.

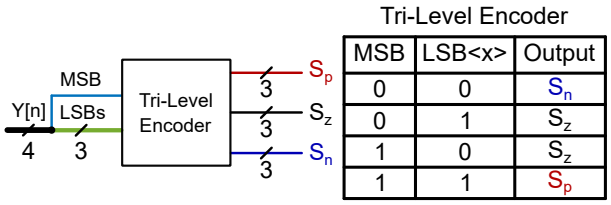

Fig. 4. Tri-level encoding to combine MSB and LSBs of the QTZ output.

shown in Section III. Section IV and Section V provide the measurement results and conclusion of the work.

II. Architecture

A. CTDSM

Due to its power efficiency, cascade-of-resonators with distributed feedforward (CRFF) topology is chosen for the main LF with 4b quantizer (QTZ) cf. Fig. 2. The MASH DDSM is applied in the outer feedback path to achieve intrinsic linearity of DAC_3 [11]. A 2-0 MASH (Leslie-Singh [13]) employing 1.5b and 4b quantizers in the 1st and 2nd stages is used to effectively suppress the in-band digital quantization noise (QN) of the DDSM. Furthermore, a 4-tap FIR filter $F[z] = 0.25(1 + z^{-1} + z^{-2} + z^{-3})$ is applied at the output of the DDSM to filter out the out-of-band (OOB) digital QN; this also results in significantly improved jitter robustness [11, Fig. 21]. To restore the ideal noise transfer-function (NTF), a 4-tap compensation filter C[z] is added in the inner feedback to compensate for the delay of $F[z]$ [14]. The CT-DSM in Fig. 2 is synthesized for an OSR = 20 and OOB gain = 3 using *www.sigma-delta.de* [15], and excess loop-delay (ELD) of 0.5Ts is compensated using a direct path around the QTZ through the 4-tap $C[z] = 1.4 + 1.3z^{-1} + z^{-2} + 0.5z^{-3}$.

B. MASH DDSM

The 2-0 MASH DDSM is implemented in error feedback topology to reduce its implementation complexity [3] [11]. Fig. 3 shows the block diagram of the DDSM where NC is applied in the 1st stage to reduce digital QN tonality [11], [16], and the 1st order shaped $QN_{1.5b}(1\text{-}z^{-1})$ is passed to the 4b quantizer of the 2nd stage. Due to NC and the unity gain signal transfer function (STF) of the 2nd stage, the required MASH DCFs are simplified to:

$$DCF_1[z] = 1, \quad DCF_2[z] = 1 - z^{-1} \tag{1}$$

DCF_2 is then combined with $F[z]$, resulting in $F[z] \cdot DCF_2 = 1 - z^{-4}$ as a modified FIR filter.

C. Tri-level Encoding

Tri-level encoding can significantly reduce the implementation effort of the DACs. It provides the advantages of reduced thermal noise and improved matching [17] [18]. Consequently, tri-level encoding is employed to implement all MB DACs. The 4b output of the QTZ can be divided into a most-significant bit (MSB) and least-significant bits (LSBs) (cf. Fig. 4). In a binary weighted 4b DAC, the MSB would control 8 DAC cells, while the LSBs would control 7 DAC cells. Nevertheless, in this work, the MSB is combined with the individual LSBs to generate the S_p, S_z, and S_n control signals of the DAC cells, resulting in either no current or twice the current of the original DAC cells [19]. Consequently, this combination implies that the MSB controls 7 DAC cells instead of 8. In order to prevent nonlinearity caused by a weighting mismatch, the QTZ must be adjusted to match the weight of the MSB of the DAC.

III. Circuit Implementation

A. Loop-filter

Fig. 5 shows the schematic of the CT-DSM, the LF is implemented using active RC integrators, and an active summer is implemented for the feedforward paths and the direct feedback path for ELD compensation. The integrators are implemented using three-stage positive-feedforward compensated operational trans-conductance amplifiers (OTAs) [19], and their limited gain-bandwidth (GBW) is compensated using closed-loop fitting [3].

B. DACs

Due to the improved matching and noise performance, DAC_3 and DAC_0 are tri-level encoded [17]. Furthermore, dual-hexa switching is applied in DAC_3 to reduce the impact of dynamic errors and ISI [12] [19]. Rise and fall time mismatches are avoided by dividing the DAC control signals into 2-phases, thus switching activity is independent of the input signal. Fig. 6 shows the implementation of the DAC_3

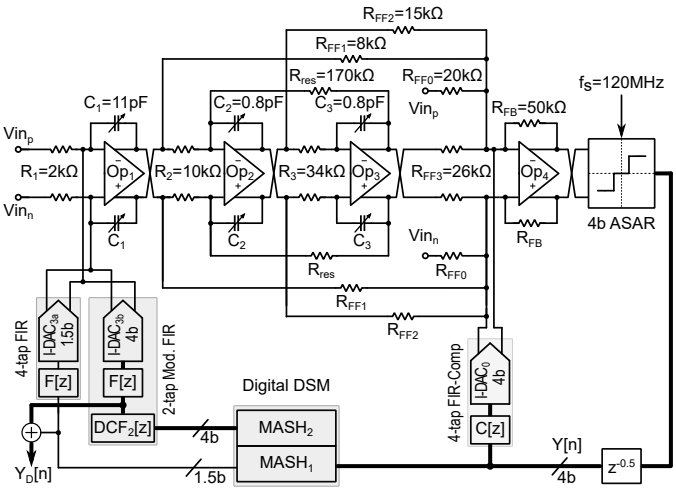

Fig. 5. Schematic of the implemented CT-DSM.

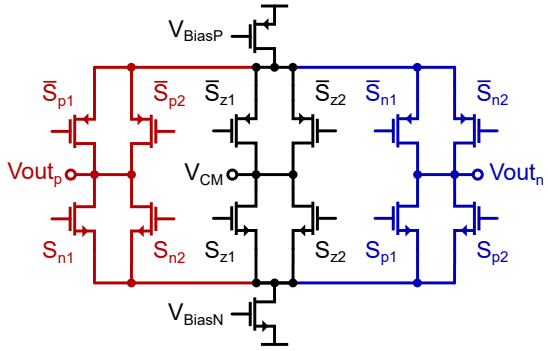

Fig. 6. Current steering DAC cell applying tri-level encoding.

cell, each of the tri-level switches is duplicated to allow for the 2 phases. DAC_3 and DAC_0 are sized for 0.1% and 0.2% mismatch respectively. Furthermore, the inner DAC_0 does not require dual-hexa switching because its nonlinearity is 3rd order shaped by the LF.

C. ASAR

An asynchronous successive-approximation-register (A-SAR) is used instead of a Flash as the main QTZ to avoid thermo-to-binary conversion and nonlinearity due to mismatch between Flash comparators. Fig. 7 shows the 4b A-SAR using bottom plate sampling, with $C_u = 1.5$fF. Since tri-level encoding is applied, the capacitive DAC (C-DAC) is modified such that the MSB $= 7C_u$ instead of $8C_u$, thus MSB weighting is equal to the sum of LSB weighting. The asynchronous control logic, based on [20], uses an on-chip sampling pulse to start the conversion. The comparator clock and the C-DAC control signals generated by the control logic allow for resolving 4b in less than 0.25Ts. The remaining 0.25Ts is then used for further processing by the MASH DDSM.

IV. Measurement

Fig. 8 shows the prototype CT-DSM. Fabricated in 28nm CMOS, the CT-DSM operates of a single 0.9V supply and occupies an active area of 0.105mm^2. The CT-DSM consumes

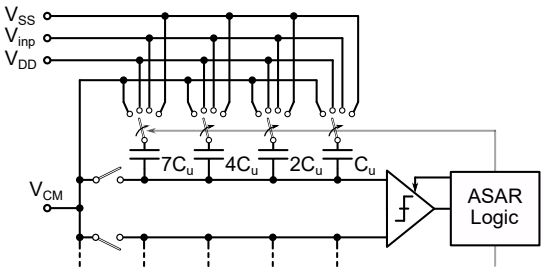

Fig. 7. A-SAR schematic including adjusted MSB weighting.

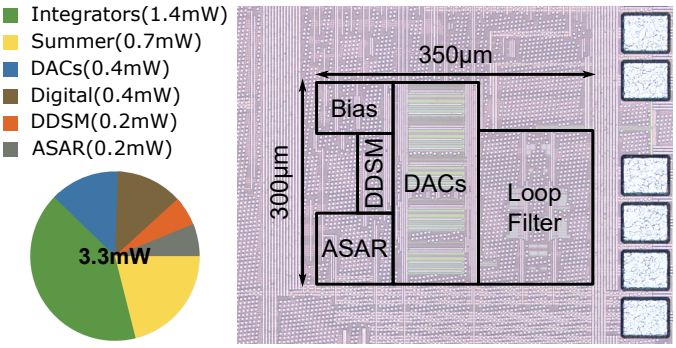

Fig. 8. Power consumption and chip micrograph with area breakdown.

a total of 3.3mW, with DDSM consuming only 0.2mW. As shown in Fig. 9, the CT-DSM has a dynamic range (DR) of 84dB with a large -1dBFS MSA due to using MB quantization. The linearity of the CT-DSM is measured using an input signal with -3dBFS amplitude at 800KHz. As shown in Fig. 10, the CT-DSM achieves an spurious-free dynamic range (SFDR) $=$ 102.3dB. Furthermore, Fig. 11 shows the measured SFDR $\geq$ 99.5dB for 4 different devices. Table I shows a comparison to state of the art (SoA) calibration-free DSMs. While the SoA uses DWA, this work presents the first DQ CT-DSM prototype using MASH DDSM for DAC linearization. Moreover, it is clear from Table I that DWA is able to reach high linearity for large OSR $= 32$ and large DAC supply (1.8V) [6], it however becomes less effective for the smaller OSR [7], while DQ is able to maintain high linearity even for low OSRs and supply.

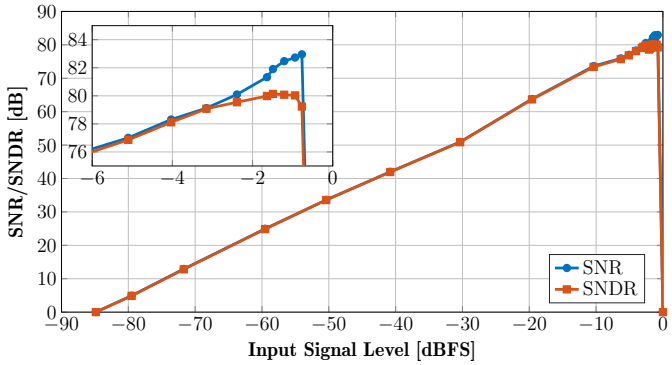

Fig. 9. Measured SNDR and SNR versus input signal amplitude.

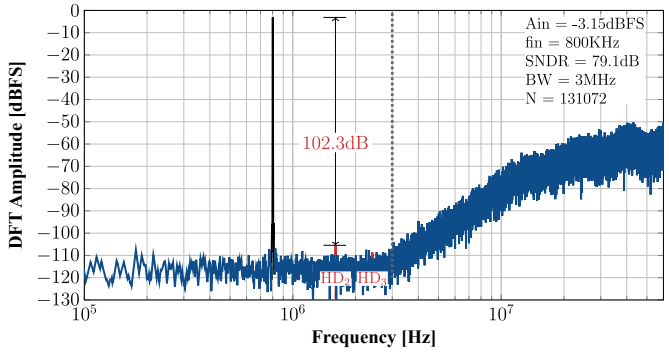

Fig. 10. Measured output spectrum.

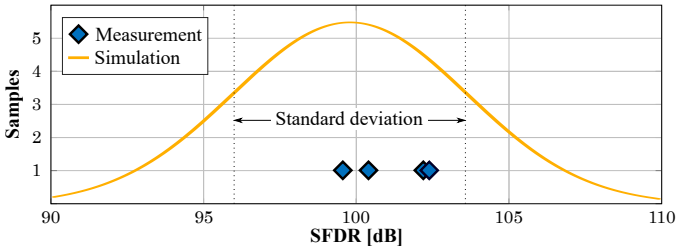

Fig. 11. Comparison of SFDR distribution from Monte Carlo simulation against measured SFDR of 4 devices.

V. Conclusion

This paper presents a 3MHz CT-DSM achieving 102.3dB SFDR without calibration. Using DDSM and FIR filtering, the CT-DSM effectively harnesses the advantages of MB quantization (Low OSR, enhanced MSA and jitter robustness) while significantly mitigating the nonlinearity of the MB DAC.

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Table I
Comparison to Other Calibration-Free DSMs

	This work	[6]	[21]	[22]	[7]
Process[nm]	28	55	65	65	14
OSR	20	32	80	32	10
BW[MHz]	3	2.2	2	2	4
QTZ bits	4b	4b	1b	3b	4b
Supply[V]	0.9	1.2/1.8	0.7	1.2	1.05
Power[mW]	3.3	4.5	0.26	4.5	0.88
SNDR[dB]	80	90	69	79	75
SFDR[dB]	102.3	104	81	100[3]	84.2
DR[dB]	84	92	76.2	80	75
Area[mm^2]	0.105	0.09	0.013	0.084	0.083
Calibration	Without (DQ)	Without (DWA)	Without (SB)	Without (DWA)	Without (DWA)
FOM_{SNDR}[dB][1]	170	177.3	168	165.5	171.3
FOM_{DR}[dB][2]	173.7	178.9	175	166.5	171.5

[1] FOM_{SNDR} = SNDR+10log$_{10}$(BW/Power)
[2] FOM_{DR} = DR+10log$_{10}$(BW/Power) [3] Estimated

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