A 282 GHz lens free source with on-chip antenna in 45 nm CMOS SOI

Mehmet Aylar, Alexandre Siligaris, José Luis Gonzalez-Jimenez, Benjamin Blampey
Grenoble-Alpes University, CEA-Leti, France
{name.surname}@cea.fr

***Abstract*—A 282 GHz source with integrated on-chip antenna is presented in this paper. It is based on a sub harmonic injection locked oscillator (triple push) driven by a doubler, realizing a ×6 frequency multiplication from the input signal. The broadside EIRP is -4 dBm and the total radiated power is -1.1 dBm at 282 GHz. A constant radiated power is obtained across the oscillator 4.2% locking range (LR). The circuit, implemented in a 45nm partially depleted SOI CMOS process, consumes 75 mW resulting in a record 1% DC-to-RF efficiency for CMOS technologies. The injection locked phase noise is as low as -110 dBc/Hz at 1 MHz offset. This compact oscillator (0.4x0.9mm) and its on-chip antenna constitute an efficient source for sub-THz imagery and radcom applications.**

***Keywords*—Triple push oscillator, injection locking, THz source, integrated antenna, CMOS, PD SOI.**

I. Introduction

The sub-THz frequencies are receiving increase interest because of interesting applications such as imagery, radar and ultra-large bandwidth communications. One of the most critical components in this context is the sub-THz source that should provide high power, low-phase noise and large tuning range. Traditional sub-THz signal generation methods, such as frequency multiplication chains, provide satisfying phase noise characteristics and high frequency tuning range. However, they suffer from low DC-to-RF efficiency and substantial power losses at each stage, requiring bulky amplification and filtering components. Fundamental oscillators, on the other hand, offer a compelling alternative due to their inherent simplicity, efficiency, and ease of integration [1]. However, fundamental oscillators are still unavailable above 300 GHz in CMOS technologies. A potential solution consists in implementing a harmonic-based *N*-push oscillator that enhances a specific harmonic of the fundamental oscillation to maximize the output frequency with good efficiency.

In this work, triple-push oscillator (TPO) topology is selected. A very first TPO has been demonstrated in 65 nm CMOS at 482 GHz delivering –7.9 dBm of output power [2]. In these oscillators, the signal generation and wanted harmonic extraction highly depend on the circuit physical layout symmetry. Most of the previously reported TPOs showing power levels above -5 dBm perform signal extraction at the center of the oscillator and require an external bias-tee at the output [3]. This prevents scalability, and complexifies the use of these oscillators in integrated transmitters or the integration of on-chip antennas. Despite its simplicity and efficiency advantage compared to multiplier chains, TPO suffer from poor phase noise and lack of stable output signal when operating in free running mode.

In this paper, a compact, lens-free sub-THz source based on a subharmonic injection locked triple push oscillator with integrated on-chip antenna is presented. Designed in CMOS PD SOI 45 nm technology, it exhibits one of the best performances, radiating -1.1 dBm of total power at 282 GHz with 1 % efficiency in just 0.4×0.9 mm^2, enabling its use in arrays.

II. Circuit Description

The source presented in this paper combines harmonic *N*-push frequency generation and sub harmonic injection locking, in a compact circuit providing a high frequency output signal with low phase noise starting from a lower frequency signal. Fig.1 shows the circuit schematic, composed by four sub blocks. From input to output, the first two blocks are a single to differential transconductor buffer that drives a frequency doubler based on a push-push topology. The input signal is around 46 GHz, and the input buffer amplifies it to overcome path loss from external signal generator and correctly drive the next stage. The push-push doubler combines the differential currents from the buffer trough a transformer. The 2nd harmonic of the input signal is extracted at the common drain node. The doubler output signal amplitude is optimized by the sizing of TLD_1 and TLD_2 transmission lines. The next stage is a common source injector used to drive the TPO input (biasing not shown). It is matched to the TPO transistor using the TL_{INJ} transmission line.

The TPO consists of three common source stages forming a ring oscillator, as shown in Fig.1. LD_{1-3} inductive transmission lines, associated with transistors parasitic capacitance define the fundamental free running oscillation frequency f_0 around 92 GHz. However, when locked by the injector circuitry its fundamental oscillation frequency is $f_0 = 2f_{in.}$ Ideally, each stage generates a drain current with a 120° phase shift from each other, and identical in amplitude. As a consequence, the resulting fundamental and 2nd harmonic oscillation currents at the common node are cancelled out because of 120° phase shift at f_0 and 240° at $2f_0$. At the third harmonic, the 360° phase

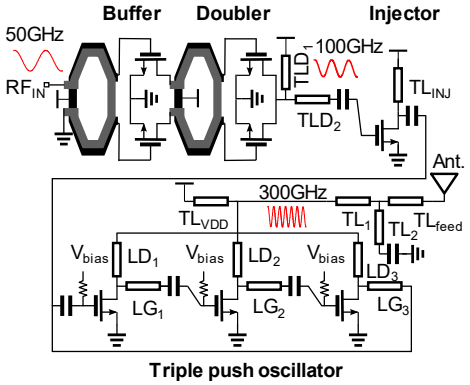

Fig. 1. The proposed injection locked triple push THz source.

shifted currents are constructively combined to form an oscillating signal at $3f_0$. LG_{1-3} transmission lines dimensioning allows to optimize the phase and amplitude of the drain current at the third harmonic [2].

III. Circuit and Antenna Design and Packaging

The back-end of the 45-nm PDSOI CMOS process used in this design includes 4 thin Cu layers (M1-M4), one intermediate thickness Cu layer (M5), 2 thick Cu layers (M6-M7) and an Al top-layer (M8). Drain inductors are implemented as microstrip transmission lines on M7 and gate inductors are implemented on M6 to reduce inter-coupling capacitance due to their proximity. TPO transistors width need a tradeoff between maximum achievable oscillation frequency and transconductance (g_m). A 40 µm width transistor is chosen to satisfy Barkhausen criteria at f_0. To reduce parasitic and thus improve the maximum frequency, transistors are divided into 4 cells with double gate contact. The layout is optimized to reduce extrinsic parasitics. The injector transistor width is minimized to reduce its parasitic impact on the TPO. The self-oscillation fundamental frequency can be tuned from 92 GHz to 94 GHz using the TPO transistors biasing voltages V_{bias}. However, this also impacts the extracted third harmonic current value through the g_m dependency on gate voltage. TL_{VDD} DC supply transmission line is optimized to present a high impedance at $3f_0$.

The patch antenna is designed on stacked top M6-M8 layers to minimize resistive loss. The antenna structure must be compatible with CMOS process rules metal densities and it includes dummies. Its size is 100×200 µm² and has been optimized to radiate in the desired frequency band. Because of 50 Ohms impedance matching cannot be guaranteed for the TPO output or the antenna input at such a high frequency, a co-design is required to optimize the radiation efficiency. Firstly, TL_{1-2} lines are tuned to optimize the voltage swing at the output to maximize the third harmonic output power. Secondly, a load-pull simulation at TL_2 output allows to determine the optimal output impedance Z_{opt} to deliver the maximum power. Finally, TL_{feed} is sized to match Z_{opt} at the wanted frequency band (274-288 GHz) taking into account the antenna load.

The final circuit layout is shown in Fig. 2.a. The core circuit including the on-chip antenna occupies only 0.4×0.9 mm² (excluding pads), which enables arrayed sources at $\lambda/2$ pitch to increase the radiated power. The IC is integrated into a 1.5×1.2 mm² metalized cavity fabricated on the MCL-E-705G substrate board as shown in Fig 2.b and Fig. 3. The PCB has 3 copper layers. The cavity is implemented between the two first layers in such a way that the IC is buried by 60 µm bellow the PCB top surface. A simplified model of the assembly, including wire bonding and V-band RF input connector is created to perform 3D electromagnetic simulations.

IV. Experimental Results

A version of the proposed sub-THz source circuit is also fabricated by replacing the antenna by GSG pads for on-wafer characterization. The version with the antenna is measured over the air in an anechoic chamber.

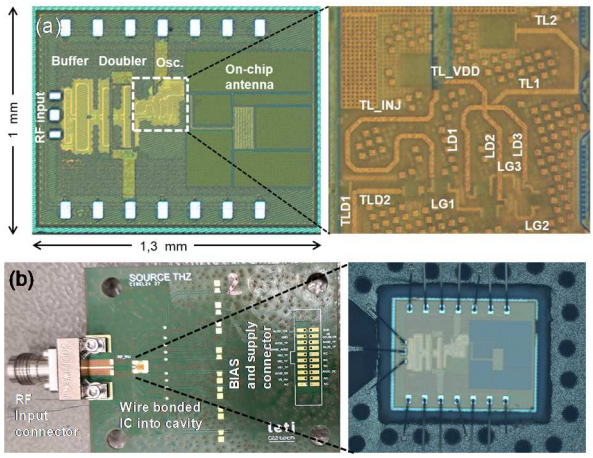

Fig. 2. (a) Chip microphotograph of the THz source IC, details of the oscillator layout, and (b) its integration in the cavity of a MCL-E-705G substrate board.

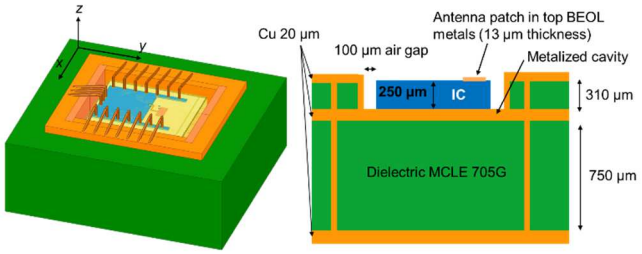

Fig. 3. Antenna integration details and board stack description.

A. On wafer measurement setup and results

For the on-wafer tests, the output signal frequency and power measurements were performed with a R&S FSW 67 spectrum analyzer (SA), calibrated with Erikson PM5 power meter, and coupled to a WR3.4 external downconverter mixer configured as a SA extender. The input signal was injected using an Agilent PSG E8257D signal generator, connected via GSG Infinity V-band probes. For output signal measurement, a GSG WR3.4 Infinity probe with a 50 µm pitch was used, followed by an S-bend WR3.4 waveguide to interface with the down-conversion mixer. Power measurements were de-embedded using the manufacturer's calibration data for the probes and interconnects. The estimated insertion loss for the output signal is approximately 10 dB at 280 GHz, and around 5 dB for the input injection signal at 46 GHz.

Figure 4.a presents both the measured and simulated free-running oscillation output frequency, showing a simulation error of less than 1%. The circuit's power consumption varies between 45 mW and 140 mW, depending on the applied bias voltage. In injection-locking mode, three bias points were selected for evaluating the locking range, as illustrated in Fig. 4.b. For an input signal power of 0 dBm, the measured locking ranges (LR) are 273–286 GHz, 276–286 GHz, and 277–287 GHz for bias voltages of 0.3, 0.58, and 0.9 V, respectively, corresponding to a 4.2% range centered around the nominal frequency. Harmonic rejection was also evaluated for the 1st, 3rd, and 5th harmonics, as shown in Fig. 4.c. The output measurement setup including probes, waveguides, and the 220–325 GHz extender was reconfigured for each

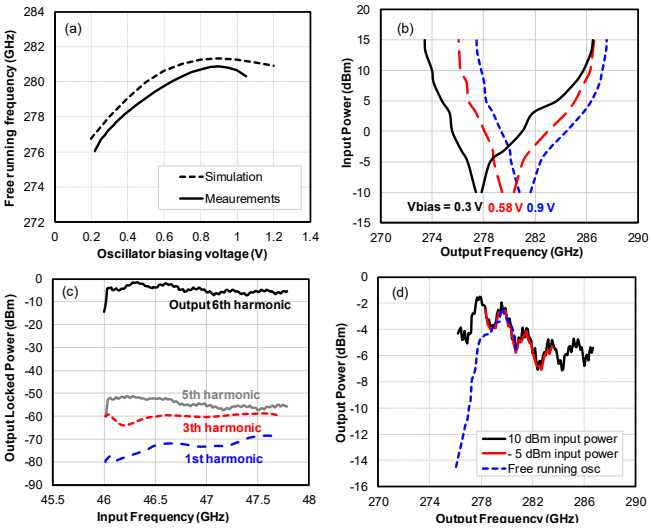

Fig. 4. On-wafer oscillator measurements: (a) simulated and measured free running frequency. (b) Oscillator locking range for different bias conditions. (c) Output harmonic power measurements for 6th, 5th, 3th, 1st harmonic. (d) Output power in free running and locking mode for several input power depending on output frequency.

frequency band (V-Band, D-Band, and J-Band). Measurements of the 2nd and 4th harmonics, around 94 GHz and 190 GHz respectively, were not performed due to the lack of appropriate WR10 and WR5 equipment. A minimum rejection of 45 dB was observed between the targeted 6th harmonic output and the lower-order 5th, 3rd, and 1st harmonics. Fig 4.d compares the output power in locking mode for input powers of –5 dBm and 10 dBm against the free-running case. In injection-locked operation, the frequency tuning range more than doubles, while the output power is both increased and stabilized, thereby improving overall system efficiency. In locking mode, the output signal phase noise is copied from the injected signal and does not depend on the TPO oscillator intrinsic properties [4]. Fig. 5.b shows the measured phase noise at 280 GHz and the generator phase noise at 46 GHz. The oscillator phase noise corresponds exactly to the input phase noise scaled up by $20\log(6)$ according to the multiplication factor. The measurement setup SA phase noise floor is around -110 dBc/Hz due to the down-conversion mixer high level noise. The SA noise floor is reached at 1 MHz offset.

B. Free space propagation setup and measurement results

The compact source with on chip antenna mounted on the PCB cavity is measured in an anechoic chamber as shown in Fig. 6.a. The proposed sub-THz module is placed on a mechanical platform that rotates around *x* and *y* axis. The module is placed at a far field distance of 3 meters from the Rx sensor, which consists in the same WR3.4 SA externed previously described and a 20 dBi standard horn antenna. The Rx can be set to measure either the vertical or the horizontally polarized field. Another calibrated WR3.4 extender is used as a reference Tx source to characterize the free space path loss and the Rx gain as a function of frequency. This reference measure is used to extract the equivalent isotropically radiated power measurement (EIRP) values from the far-field measured power

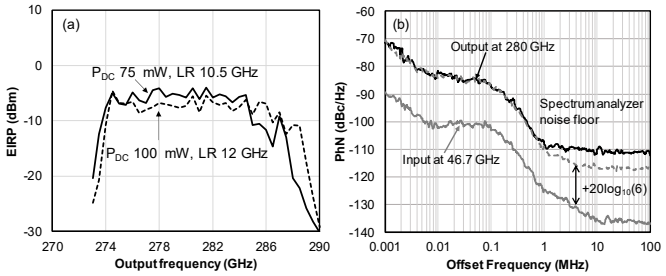

Fig. 5. (a) Two different broadside EIRP versus frequency measurements, corresponding to two different LRs (b) Phase noise measurements, comparing the input and output phase noise.

at the Rx. Fig. 5.a shows the EIRP measured in the broadside direction as a function of frequency for the vertical polarization (across the *y* axis direction). The EIRP power remains constant around -6 dBm over frequency, limited by the TPO locking range (274-288 GHz). A peak broadside EIRP of -4 dBm is observed at 282 GHz.

The normalized (co-polarization) radiation pattern is characterized in the two orthogonal *xz* and *yz* planes, and compared to simulations as depicted in Fig. 6.b. The asymmetry observed on the radiation diagram in the *yz* plane (confirmed by the simulations) is attributed to reflections on the metallic input signal connector. Due to these reflections, the radiated power is spread across a broader angle and also is sent to the cross-pol direction (see Fig. 7). A raw angular integration of the power measured at 282 GHz from both polarizations (after compensating for the path loss and receiver gain) results in -1.1 dBm, very close to the -1 dBm output power obtained from the on-wafer measurements at the output of the circuit. The simulated and measurements mismatch at some angles may be due to oversimplification in the PCB 3D model used in the EM analysis tool to reduce simulation time.

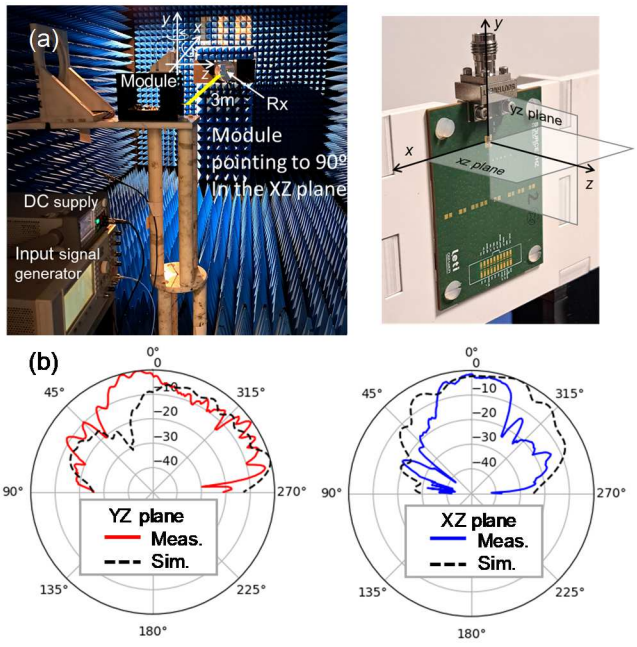

Fig. 6. (a) In-chamber measurement set-up, and (b) normalized experimental radiation diagram of the source module at 282 GHz in the vertical polarization.

Table I. Sub-THz source and oscillators state of the art

Specifications	**This work**	[5] JSSC 2012	[6] ISSC 2012	[2] JSSC 2011	[7] MWTL 2015	[8] ISSC 2014	[3] RFIC 2016	[9] ISSC 2014
Architecture	**Doubler+TPO**	Diff-TPO	VCO+Tripler	TPO	TPO	TPO	TPO	TPO
Number of elements	**1**	2	4x4	1	1	4x4	4	1
Integrable/scalable	**Yes**	Yes	Yes	No	Yes	Yes	No	Yes
Integrated antenna	**Yes**	Yes	Yes	No	No	Yes	No	No
Frequency (GHz)	**280**	288	285	482	285	338	299	290
Output power per element (dBm)	**-1*/-1.1****	-1.5*/-4.1**	-19.2**	-7.9*	-9*	-12.9**	0.9*	-14*
Peak EIRP at broadside (dBm)	**-4**	-4.1	9.4	NA	NA	17.1	NA	NA
P_{DC} (mW)	**75**	275	890	61	52	1540	235	106
Phase noise (dBc/Hz) at 1 MHz offset	**-110**	-87	-92	-76	-105	-93	-79	-80
Frequency TR (%)	**4.2**	1.4	3.2	NA	10.9	2.1	1.7	8
Total Efficiency (%)	**1**	0.25	0.02	0.22	0.24	0.05	0.51	0.03
FOM^{+} (dBc/Hz)	**-200**	-172	-172	-172	-197	-172	-169	-169
Technology	**45nm CMOS**	65nm CMOS	45nm CMOS	65nm CMOS	BiCMOS 55	65nm CMOS	65nm CMOS	90nmSiGe

* On chip power ** Radiated output power

$$FOM^{+} = PhN(\Delta f) - 20\,Log\left(\frac{f_{osc}}{\Delta f}\right) + 10\log\left(\frac{P_{DC}}{1\,mW}\right)$$

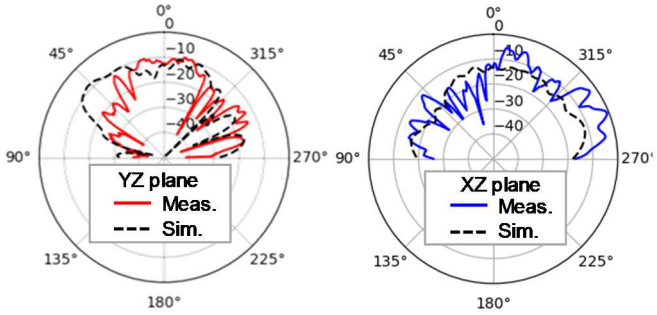

Fig. 7. Normalized experimental radiation diagram of the source module at 282 GHz in the horizontal polarization direction.

V. Conclusion

This paper presents a compact, lens-free 0.28 THz source fabricated in 45 nm CMOS PDSOI technology from Global Foundries. The circuit performances are compared to similar sources and oscillators in Table 1. To the author knowledge, a record value of -1 dBm at 280 GHz for 1 % DC-to-RF efficiency is measured on wafer for a single element, which is the double of the highest recorded efficiency in CMOS node, for an integrable (external bias-tee free) circuit. For the radiated power with on chip antenna, it is the very first lens-free sub-THz source radiating in the front side, recording the highest reported total radiated power of -1.1 dBm for a single oscillating element. The compact source consumes 75 mW of DC power resulting in 1% DC-to-THz efficiency. The source, including the on-chip antenna, occupies 0.4x0.9 mm^2 and is compliant with an array arrangement that would allow to increase the radiated power. The large locking range and the excellent phase noise performance enable high-quality frequency modulated continuous wave (FMCW) signal generation, a critical requirement for radar and sensing applications. Overall, the proposed sub-THz source is, to the best of the authors knowledge, the first CMOS integrated source able to fulfill the requirements of sub-THz signal generation for both imaging and radar applications in a low-cost, compact and lens-free implementation, showing one of the best DC-to-RF efficiencies to date.

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