A 0.38-THz Scalable 2-D Beam-Steering Radiator Array Based on High-Efficiency Push-Push Oscillators

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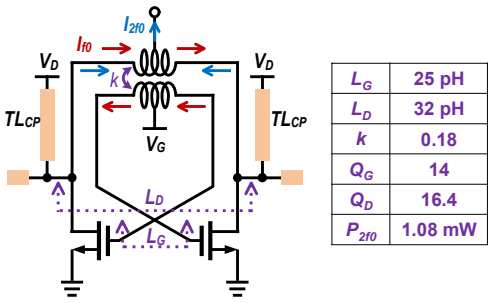
***Abstract*—A 0.38-THz radiator array features scalability and two-dimensional (2-D) beam steerability. A high efficiency is primarily achieved by designing an array of coupled-inductor-based push-push oscillators (CIB-PPOs) and extracting its strong second-order harmonics as the THz output. Enhancing the isolation between the gate and drain terminals of the transistors at the second-order harmonic frequency to effectively reducing signal leakage losses further improves the efficiency. At the system level, potential mode ambiguity is suppressed, and phase shifting is realized by tuning the self-oscillation frequency of each CIB-PPO via their gate biasing voltages. For validation, a 4×4 array with on-chip antennas were implemented in a 65-nm CMOS process. The fabricated prototype measures a frequency range of 366 to 386.4 GHz (5.4%), with a maximum radiated power of 0.45 dBm and a competitive peak DC-to-RF efficiency of 0.15%. The beam-steering ranges are 43° and 16° in the E-plane and H-plane, respectively.**

Keywords*—Beamsteering, coupled inductor, DC-to-RF efficiency, output power, push-push oscillator, radiator array, terahertz (THz).

I. Introduction

The terahertz (THz) and sub-THz spectrum are promising for enabling wireless communications with unprecedented data rates and facilitating high-resolution imaging and sensing applications. In many of these use cases, a beam-steerable signal source with adequate output power is required. However, as the operating frequency approaches or even surpasses the maximum oscillation frequency (f_{max}) of transistors, achieving reliable signal generation becomes increasingly challenging, let alone attaining a practical and usable level of output power.

In recent years, significant advancements in THz radiator chip design have been driven by innovations in device optimization [1], circuit topologies [2]-[4], and system integration [5]-[7], leading to rapid progress. In [2], a method utilizing fundamental oscillation followed by frequency doubling achieves a signal source with 0.37% efficiency at 312 GHz. However, this approach faces challenges for scaling up the array size, which in turn limits the output power and the equivalent isotropically radiated power (EIRP). As an alternative, harmonic oscillators have been explored to enable scalability, potentially enhancing EIRP [3]. In [4], an array operating at 340 GHz simultaneously achieves scalability and beam steerability, though these capabilities are both confined to a single dimension. Two-dimensional (2-D) array expansion and beam steering have been realized by coupled oscillator arrays and their high-order harmonics are served as the output [5]-[7]. However, this approach typically yields efficiency levels below 0.05%.



L_G	25 pH
L_D	32 pH
k	0.18
Q_G	14
Q_D	16.4
P_{2f0}	1.08 mW

Fig. 1. Schematic of the proposed coupled-inductors-based push-push oscillator (CIB-PPO).

In this paper, a coupled-inductor-based push-push oscillator (CIB-PPO) is proposed, enabling fundamental oscillation at 190 GHz and highly efficient second-order harmonic generation at 380 GHz. Furthermore, a coherent 4×4 array of CIB-PPOs is demonstrated, showcasing both scalability and 2-D beam steerability based on the mechanism in [8]. The radiator, prototyped using a 65-nm CMOS process, achieves a radiated power up to 0.45 dBm and a peak DC-to-RF efficiency of 0.15%.

II. Coupled-Inductor-Based Push-Push Oscillator

Evidently, the realization of a THz radiator array that simultaneously offers scalability, 2-D beam steerability, and high efficiency remains a significant challenge. In essence, this is largely because the increasing constraints—particularly the additional parasitics—introduced by coherently coupling multiple oscillators and enabling phase shifting impose an upper limit on the fundamental oscillation frequency. As a result, high-order harmonic extraction becomes necessary, which inherently exhibits a reduced efficiency.

To address this issue, a coupled-inductor-based push-push oscillator (CIB-PPO) is proposed to enhance the fundamental oscillation frequency, thereby reducing the required harmonic order for efficiency improvement. As depicted in Fig. 1, the proposed CIB-PPO is mainly composed of a pair of transistors providing necessary loop gain to sustain oscillation, and a coupled inductor pair. The coupled inductors function as a feedback network, determining the fundamental oscillation frequency (f_0). Meanwhile, the second-harmonic currents (i_{2f0}) generated

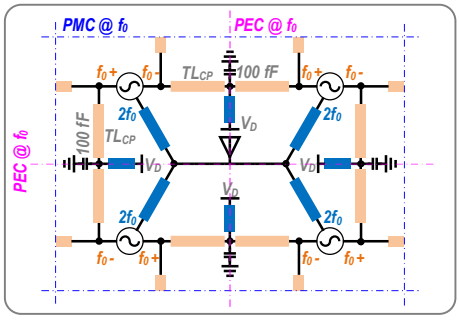


Fig. 2. Radiator element consisting of 4 coupled oscillators and an on-chip dual-fed loop antenna.

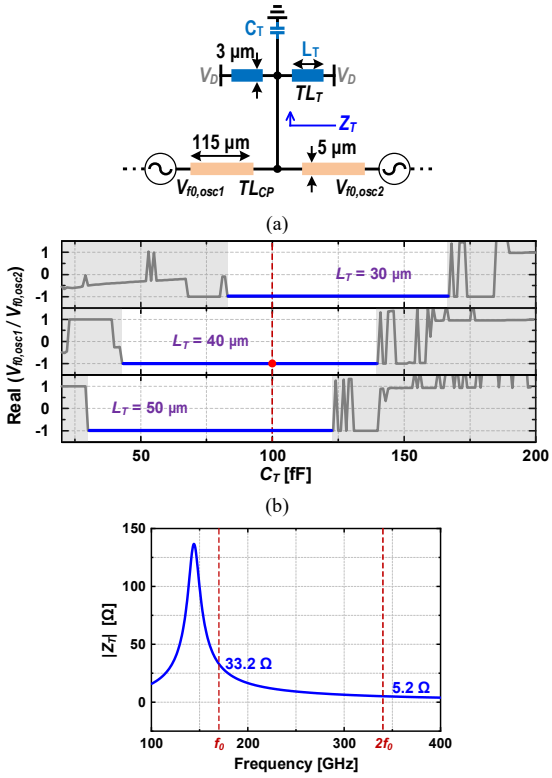


Fig. 3. (a) Mode ambiguity suppression in coupled oscillators by connecting TL_T and C_T between each two neighboring TL_{CP}. (b) Demonstration of mode stability. A ratio $V_{f0,osc}$ /$V_{f0,osc2}$ of -1 indicates an odd-mode operation. (c) Simulated impedance (Z_T) contributed by TL_T and C_T.

by the two transistors are constructively combined and extracted from the center-tap node.

In addition to utilizing the strong second-order harmonic as the output, the DC-to-RF efficiency is further optimized by the following measures. First, the feedback network plays a critical role in isolating the gate terminals from the drain terminals at the second-order harmonic frequency ($2f_0$), effectively minimizing leakage losses. Second, the out-of-phase operation for the transistor pair is realized through cross-coupling, with the use of L_G. As such, the long transmission lines typically required in conventional solutions [4] are eliminated and thus their associated high loss can be avoided. Third, to maximize the output power at $2f_0$, the inductor values L_G and L_D are optimally designed to be

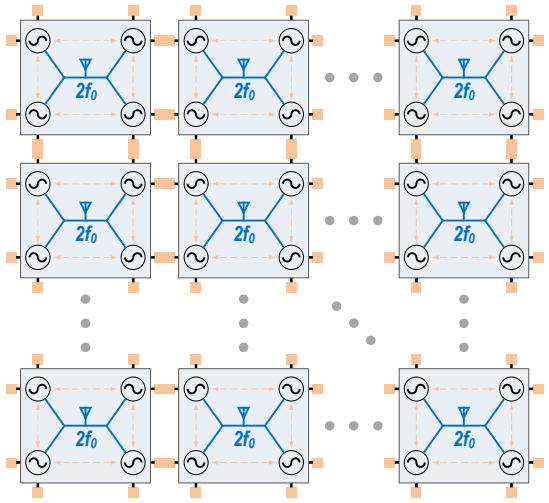


Fig. 4. System architecture of the proposed scalable and 2-D beam-steerable radiator array.

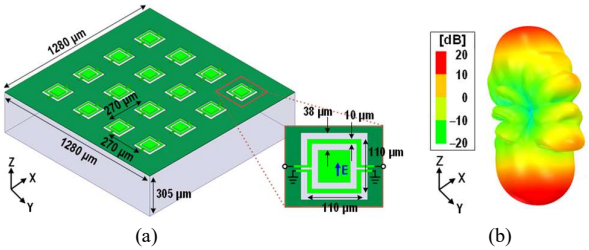


Fig. 5. On-chip 4×4 loop antenna array. (a) 3-D structure. (b) Simulated 3-D radiation pattern.

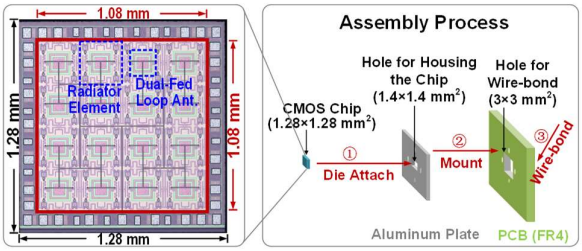
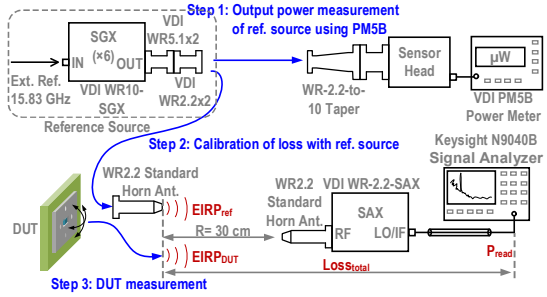


Fig. 6. Chip micrograph and assembly process.

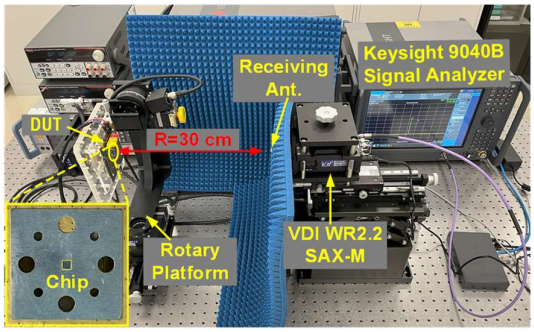
25 and 32 pH, respectively, with achievable quality factors of 14 and 16.4. Their coupling coefficient k is 0.18. Fourth, the optimal load impedance at $2f_0$ is identified by load-pull simulation and then realized by an impedance matching network between the oscillator and the antenna.

III. Array Construction and Mode-Ambiguity Suppression

As shown in Fig. 2, four CIB-PPOs are coupled together at f_0 using transmission lines (TL_{CP}), and their output power at $2f_0$ is combined before being fed to an on-chip antenna. Within this radiator element, the boundary between each two neighboring oscillators is ideally designed to function as a perfect electric conductor (PEC) to facilitate odd-mode operation at f_0. However, coupling between oscillators can potentially occur in even mode, leading to mode ambiguity. To mitigate this issue, a shunt transmission line (TL_T) and a



(a)



(b)

Fig. 7. (a) Setup for radiation pattern and EIRP measurement. (b) Photograph of in-house testing.

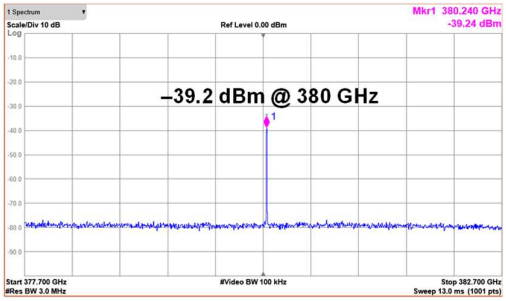
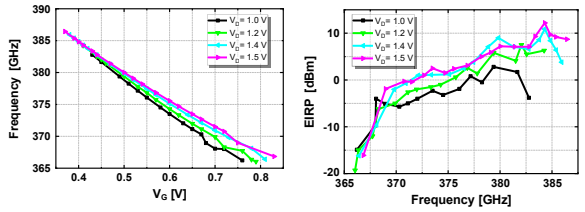


Fig. 8. Measured output spectrum at 380 GHz.

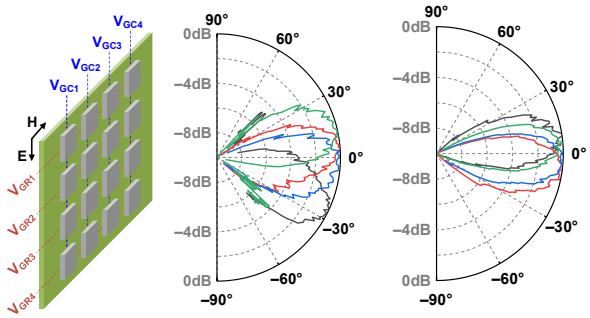
capacitor (C_T) are added between each pair of neighboring TL_{CP}, effectively suppressing the undesired even mode, as shown in Fig. 3(a). To evaluate the oscillation mode, the voltage ratio $V_{f0,osc1}/V_{f0,osc2}$ is simulated using SpectreRF. As depicted in Fig. 3(b), by optimizing the length of a shunt transmission line (TL_T) to 40 μm and its parallel capacitor (C_T) to 100 fF, odd-mode operation is reliably achieved. Furthermore, the simulated impedance (Z_T) contributed by TL_T and C_T is shown in Fig. 3(c). At f_0, a moderate $|Z_T|$ of 33.2 Ω helps suppress even-mode oscillation, which would require a nearly open circuit. Conversely, at $2f_0$, $|Z_T|$ is as low as 5.2 Ω, creating a reflective termination that recycles harmonic power and thus minimizes power loss. Notably, the DC power can be supplied through the shunt transmission lines.

With such an element featuring connectivity in all four directions around, a scalable radiator architecture can be constructed, as illustrated in Fig. 4. The short transmission lines connecting adjacent elements realizes a perfect magnetic conductor (PMC) boundary and an array-level



(a) (b)

Fig. 9. (a) Measured output frequency under various gate bias V_G. (b) Measured EIRP at different frequencies.



(a) (b) (c)

Fig. 10. 2-D beam steering. (a) Configuration of gate biasing voltages. (b) beam steering in the E-plane: 43° from –28° to 15°). (c) beam steering in the H-plane: 16° from –7° to 9°.

even-mode operation at f_0. For validation, a 4×4 array is designed and implemented. Accordingly, a 4×4 dual-fed loop antenna array is integrated on chip, as shown in Fig. 5(a). With a 305-μm thick substrate, the simulated 3-D radiation pattern is plotted in Fig. 5(b). The directivity and radiation efficiency achieved are 13.5 dB and 38%, respectively.

The radiation beam of the array can be steered by intentionally adjusting the self-oscillation frequency of each oscillator to create variable phase shifts [8]. Fortunately, due to the sufficiently strong couplings between adjacent elements, frequency synchronization across the entire array is maintained.

IV. Experimental Results

The 4×4 radiator array chip was fabricated in a 65-nm CMOS process, occupying a core area of 1.08 mm× 1.08 mm. The chip was assembled with a hollowed aluminum plate and a printed circuit board (PCB) for testing purposes, as illustrated in Fig. 6.

For measuring the EIRP and the radiation patterns, the device under test (DUT) is mounted on a rotary platform. The radiated signal is received by a horn antenna and down-converted using a VDI spectrum analyzer extender (VDI WR2.2SAX) before being analyzed by a signal analyzer (Keysight N9040B), as depicted in Fig. 7(a). The distance between the DUT and the horn antenna is set to 30 cm to fulfill the far-field condition. Free-space propagation and down-conversion losses are pre-calibrated using a reference source and a power meter (VDI Erikson PM5B). A photograph of the in-house testing setup is presented in Fig. 7(b).

The output spectrum at 380 GHz is shown in Fig. 8. By adjusting all the gate bias V_G together, a frequency tuning range of 366 to 386.4 GHz (5.4%) is achieved under various

TABLE I. COMPARISON WITH RECENT WORKS

Ref.	TCAS-I'22 [2]	JSSC'22 [3]	CICC'24 [4]	JSSC'15 [5]	JSSC'19 [6]	JSSC'22 [7]	This Work
Freq. [GHz] (Harmonic Order)	312 (×2)	450 (×2)	345.8 (×2)	338 (×4)	344 (×4)	416 (×6)	**384.3 (×2)**
Beam Steering [°]	NA	NA	90/0	45/50	128/53	60/60	**43/16**
P_{rad} [dBm]	-3.8	–3.2	–4.2	–0.9	–6.9	–3	**0.45**
DC-to-RF Efficiency [%]	0.37	0.14	0.27	0.053	0.046	0.034	**0.15**
EIRP [dBm]	14.5 (w/ Lens)	29.1 (w/ Lens)	30.5 (w/ Cassegrain Ant.)	17.1	4.9	14	**12.2**
Tuning Range [%]	4.8	4.6	4.5	2.1	15.1	1.7	**5.4**
Phase Noise [dBc/Hz@ Offset]	NA	–76.4 @1MHz	–85.2@ 1MHz	–93 @1MHz	–93 @10MHz	–88 @1MHz	**–85.1@ 1MHz**
P_{dc} [mW]	114	347	140	1540	450	1450	**747**
Antenna Type	Monopole Ant.+ Si Lens	Slot Ant.	Loop Ant.+ Cassegrain	Patch Ant.	Patch Ant.	Patch Ant.	**Loop Ant.**
Array Size	1×2	4×4	2×7	4×4	2×2	4×4	**4×4**
Technology	40nm CMOS	65nm CMOS	65nm CMOS	65nm CMOS	130nm SiGe	65nm CMOS	**65nm CMOS**
Area [mm^2]	0.32 (Core)	1.56	1.59	3.9	1.2	4.1	**1.64**

supply voltages, as shown in Fig. 9(a). The measured EIRP, depicted in Fig. 9(b), indicates a peak value of 12.2 dBm at 384.3 GHz when powered by a 1.5-V supply. From the measured radiation patterns, the directivity is determined to be 11.75 dB, resulting in a radiated power of 0.45 dBm. Considering the DC power consumption of 747 mW, the DC-to-RF efficiency is estimated to be 0.15%.

Beam steering in the E-plane and H-plane is tested by sequentially sweeping the gate biasing voltages, either row by row (V_{GR1} to V_{R4}) or column by column (V_{GC1} to V_{GC4}), as illustrated in Fig. 10(a). To minimize frequency variation during beam steering, the gate biasing voltages are configured to resemble an arithmetic sequence while maintaining a relatively constant average value. As shown in Fig. 10(b) and (c), beam steering angles of 43° in the E-plane and 16° in the H-plane are measured at 380 GHz.

Table I summarizes the performance of this work and compares it with several recently published THz sources operating at similar frequencies. The radiator array in this work achieves the highest output power of 0.45 dBm and the highest DC-to-RF efficiency of 0.15% among the listed 2-D beam-steerable radiators.

V. CONCLUSION

This paper proposes a 4×4 2-D beam-steerable and scalable radiator array at 380 GHz. With the CIB PPOs and the mode-ambiguity suppression method proposed, the prototype achieves a frequency range of 366 to 386.4 GHz, and 2-D beam-steering ranges of 43° in the E-plane and 16° in the H-plane, with a radiated power up to 0.45 dBm and a peak DC-to-RF efficiency of 0.15%, which is the highest among the listed 2-D beam-steerable radiators.

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