Demonstration of Nanoscale Cryogenic Ferroelectric Independent-Double-Gate FinFET for High-Density Storage and Neuromorphic Computing

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***Abstract* — In this paper, for the first time, we demonstrate a novel device – ferroelectric independent-double-gate FinFET (FeIGFinFET). Both independent-gate FinFET characteristics and ferroelectric memory properties are experimentally demonstrated on the same device. With back-gate biasing, FeIGFinFET achieves significantly reduced static leakage compared to its conventional common-gate counterpart. We have also demonstrated that the FeIGFinFET stores independent states at its two gates, doubling the storage density. Independent potentiation and depression characteristics for the front- and back-sides at both room temperature and 77K also highlight the potential of FeIGFinFET for neuromorphic computing. At the array level, FeIGFinFET can achieve significantly improved program-inhibit operation, as shown with mixed-mode TCAD simulation.**

Keywords—Ferroelectric, FinFETs, Double-gate FETs, Nonvolatile memory, Neuromorphic computing

I. Introduction

As artificial intelligence and edge computing continue to advance, the everlasting demand for on-chip high-density memory, high-performance, and low-power computation calls for novel materials, devices, and architecture (**Fig. 1**) [1]. Hafnium-based ferroelectric (FE) material, $Hf_{0.5}Zr_{0.5}O_2$ (HZO) in particular, has been viewed as a candidate for future memory, thanks to its nanoscale-CMOS compatibility, low write latency, and low program voltage. Devices such as FE FETs or FE FinFETs have been widely developed at room temperature (R.T.) [2][3] or cryogenic temperatures (Cryo T.) [4]. Future servers may operate at 77K for reduced power consumption, and FE memory is an excellent candidate with the low write voltage. In this paper, we propose and experimentally demonstrate a novel FE-independent double-gate FinFET (FeIGFinFET) structure with a FE gate stack and independent storage and operation at separate front- and back-gates, essentially doubling the storage density. FeIGFinFET may also be applied to cross-bar computing-in-memory (CIM) architecture with two gate sides that can be viewed as two separate synaptic elements during current summation for a non-von-Neumann computing architecture. In this paper, we demonstrate FeIGFinFET with (1) a new gate separation process for device fabrication; (2) independent storage at both front-gate (FG) and back-gates (BG) at R.T. and Cryo T.; (3) the ability to achieve independent potentiation and depression operation for neuromorphic applications; (4) static leakage suppression via direct BG biasing; (5) novel CIM array architecture for high-density neural networks.

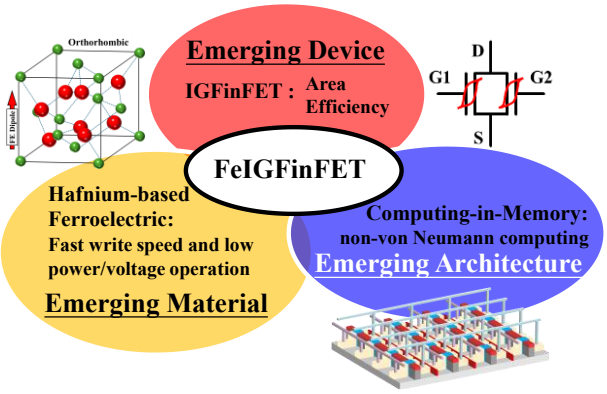

Fig. 1. (a) FeIGFinFET: A novel device combining emerging hafnium-based FE materials, novel device structure for high-density storage, and new CIM circuit architecture for non von-Neumann computation.

II. Fabrication and Characterization

A. FeIGFinFET Fabrication Process

Fig. 2 presents the process flow for FeIGFinFETs. To enhance the crystallinity of HZO, a thin (1.5nm) ZrO_2 layer is deposited prior to HZO (5nm or 10nm) to enhance FE crystal formation [5]. The two-step annealing processes (rapid thermal anneal (RTA) at 700°C and microwave anneal (MWA)) are performed to promote good crystal quality and FE properties in the HZO layer based on FE capacitor experiments that were done separately. MWA limits the thermal budget after source/drain implantation for a sharper junction. To separate FG and BG, we use chemical

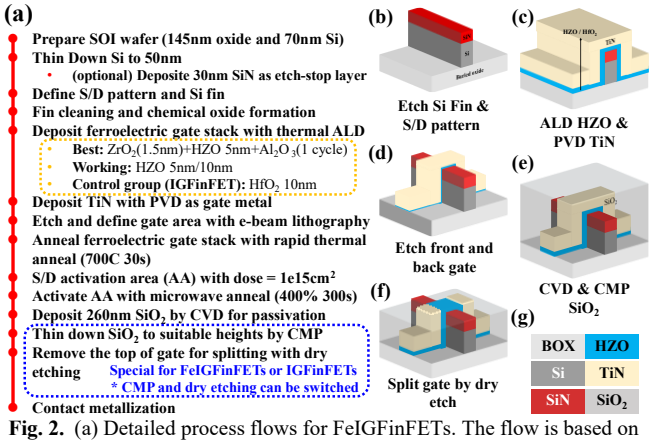

Fig. 2. (a) Detailed process flows for FeIGFinFETs. The flow is based on regular FE FinFET process flow [6] with modifications. Several gate stacks options are listed. With the help of the ZrO_2 seed layer, FeIGFinFET can achieve better ferroelectricity. Gate splitting with CMP and dry etch are added to make IGFinFETs or FeIGFinFETs. (b)-(g) Main process steps and corresponding drawn materials.

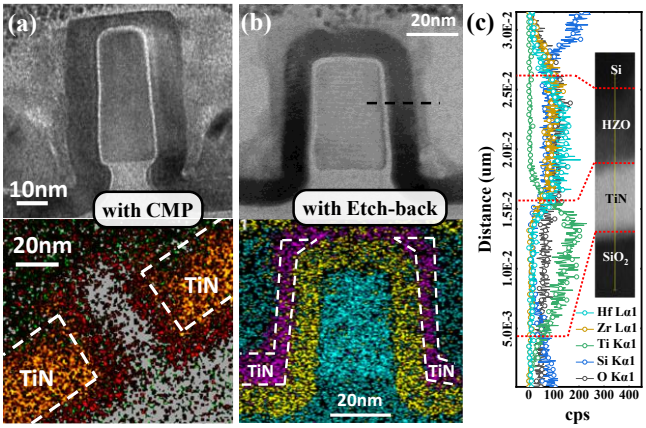

Fig. 3. TEM and EDX mapping results showing successful gate (TiN) splitting using (a) chemical mechanical polishing (CMP) with W_{layout} = 25nm and (b) dry etching with W_{layout} = 35nm. (c) EDX line-scan from the Si channel (top) all the way to the SiO_2 passivation layer (bottom).

mechanical polishing (CMP) followed by dry etching, rather than a single CMP process, to split the gates. This allows the fabrication of both independent-gate (IG) FinFETs and regular (common-gate, CG) FinFETs on the same wafer, as the dry etching step can be blocked by an additional photomask. In **Fig. 3(a)(b)**, cross-sectional transmission electron microscope (TEM) and energy-dispersive X-ray spectroscopy (EDX) images of the FeIGFinFETs with different separation methods are shown. Clear separation of the TiN gate (highlighted with white dashed lines) is shown. **Fig. 3(c)** shows the EDX line scan across the FE gate stack from **Fig. 3(b)** (along the dashed line), indicating the successful deposition of HZO. We have also fabricated control IGFinFET devices without a FE gate stack by following the same process flow but replacing HZO with regular high-k HfO_2.

B. Electrical verification of IGFinFET

Electrical characterization results indicate successful gate splitting. **Fig. 4(a)** shows clear IG operation for both n- and p-type IGFinFETs. The different biases applied to the BG can easily control the threshold voltage (V_T) of the device while operating in IG mode (**Fig. 4(b)**). A higher slope (body factor) is shown for devices with thinner fin structures due to a larger electric field across the fully depleted fin. BG is very effective in suppressing static leakage current. On the other hand, the sub-threshold swing is very large when the BG channel is

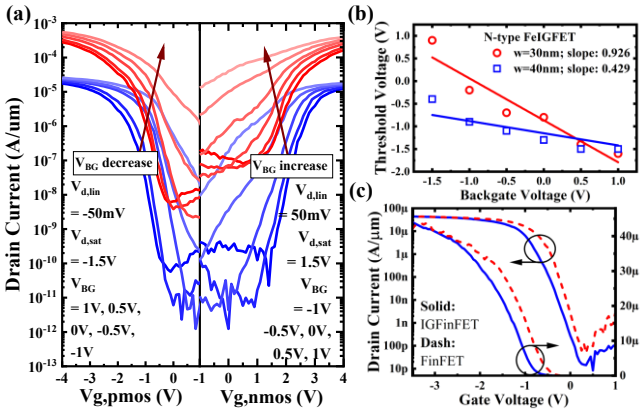

Fig. 4. (a) Transfer I_D-V_G characteristic of n-type and p-type IGFinFETs highlighting BG tuning effects. (b) V_T dependence on BG voltage for different fin widths for IGFinFETs. Thinner fins exhibit greater sensitivity to BG voltage. (c) IGFinFET operated in CG mode and regular FinFET without gate separation etch show similar I_D-V_G.

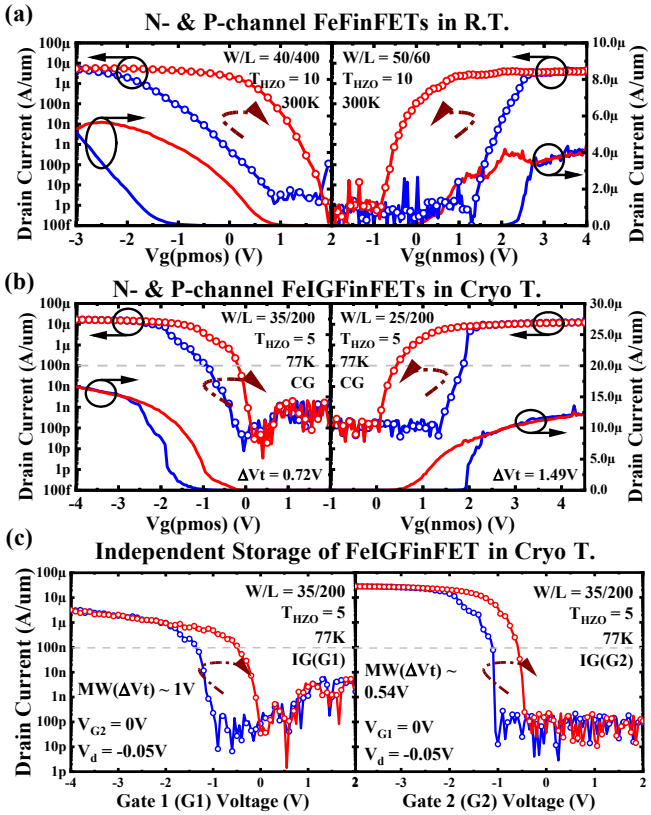

Fig. 5. I_D-V_G characteristic of (a) FE FinFET memory at R.T. and (b) FeIGFinFET in CG mode at Cryo T. with FE hysteresis in both n-type and p-type devices. (c) Both G1 and G2 in FeIGFinFET exhibit FE hysteresis in the same device, with slightly asymmetric I-V due to process variation. Large memory window (MW) with step-like sweep shows the successful fabrication of FE FinFETs with nanoscale HZO gate stack. Note that for all the sub-figures, blue is for forward sweep and red is for reverse sweep. The unit for device width (W), length (L) and HZO thickness (T_{HZO})is in nano-meters (nm)

inverted, as expected. Meanwhile, when operating IGFinFETs in CG mode by sweeping the two gates together electrically, its I_D-V_G is similar to regular FinFET on the same wafer, with metal gates physically connected and surrounding the fin (**Fig. 4(c)**), except for the V_T shift due to device variation. During IG measurements, we confirmed successful operation with gate 1 (G1) or gate 2 (G2) as either FG or BG.

III. Independent Storage on FeIGFinFET

A. Data Storage in FeIGFinFET

With the independent-gate structure, FeIGFinFETs can perform memory storage operations in both CG and IG modes. First of all, we measured double-sweep I_D-V_G in FE FinFETs (without gate splitting) to confirm proper FE FET operation for both n- and p-channel devices (**Fig. 5(a)**). For FeIGFinFETs, **Fig. 5(b)** shows double-sweep I_D-V_G in CG-mode in both n- and p-channel devices, with expected counterclockwise hysteresis direction for n-channel devices and clockwise hysteresis direction for p-channel devices. When operating the device in IG mode, as shown in **Fig. 5(c)**, FE hysteresis is observed by setting either G1 or G2 as the FG, while keeping the other gate (BG) grounded. This demonstrates that both G1 and G2 can store FE states. By operating in IG mode, FeIGFinFETs double the number of stored states in a single device, thereby enhance area

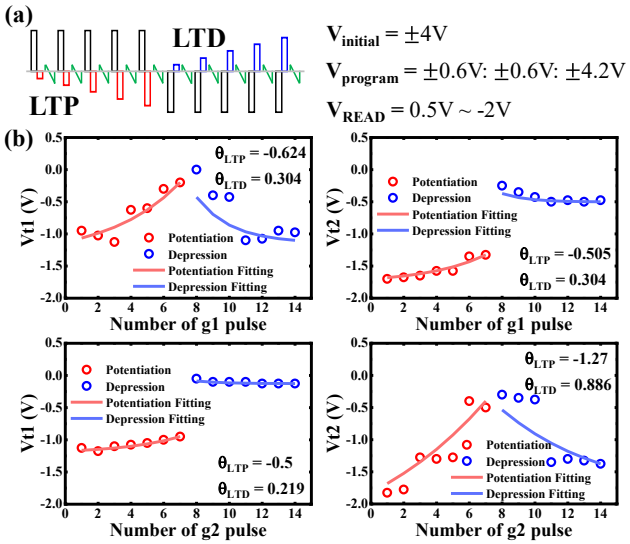

Fig. 6. LTP and LTD measurement conditions and measurement results with $Vt_{LTP/LTD}$ fitting curves. Pulse voltage range from ±0.6V to ±4.2V in steps of ±0.6V. V_T results show a near-linear response when the pulse is applied to the same-side gate, while nearly no change when the pulse is applied to the opposite-side gate.

efficiency. For example, if 2 bits can be stored on one side of the gate, 4 bits can be stored in the entire FeIGFinFET device.

B. Neuromorphic Potentiation and Depression Operation with FeIGFinFET

To investigate the potential of FeIGFinFETs for neuromorphic computing, we have characterized their potentiation/depression behavior and extracted their non-linearity factors. Equations (1) through (4) describe device V_T as a function of pulse number (P) with expressions similar to [7][8], but replacing the conductance of resistive memory devices with threshold voltage for the FeIGFinFET. $\theta_{LTP/LTD}$ are the nonlinearity ratio for potentiation and depression, which are extracted by fitting V_T vs. P to measured data. Consecutive increasing pulse voltages are applied to one gate while the other gate remains grounded. **Fig. 6(a)** illustrates the pulse setting during measurement.

$$Vt_{LTP} = \beta_{LTP}\left(1 - e^{-\frac{P}{\alpha_{LTP}}}\right) + Vt_{min} \quad (1)$$

$$Vt_{LTD} = -\beta_{LTD}\left(1 - e^{-\frac{P-Pmax}{\alpha_{LTD}}}\right) + Vt_{max} \quad (2)$$

$$\beta_{LTP/LTD} = \frac{Vt_{max} - Vt_{min}}{1 - exp\left(-\frac{P_{max}}{\alpha_{LTP/LTD}}\right)} \quad (3)$$

$$\alpha_{LTP/LTD} = \theta_{LTP/LTD} \times P_{max} \quad (4)$$

When applying program pulses to one gate, the V_T of the same-side gate increases almost linearly with the number of pulses, while the V_T of the opposite-side gate (measured by sweeping the other gate) remains essentially unchanged. This is confirmed repeatedly by treating either gate as the front gate (**Fig. 6(b)**). The results shown here are similar for Cryo T. and R.T. The reason for the very little impact of stored FE polarization on the V_T on the other gate is that the electric field near the same-side gate is much larger than the opposite-side gate, as can be seen from the very asymmetric energy band diagram (**Fig. 7(a)**). Therefore, we may independently store a FE state without affecting the read-out on the other side.

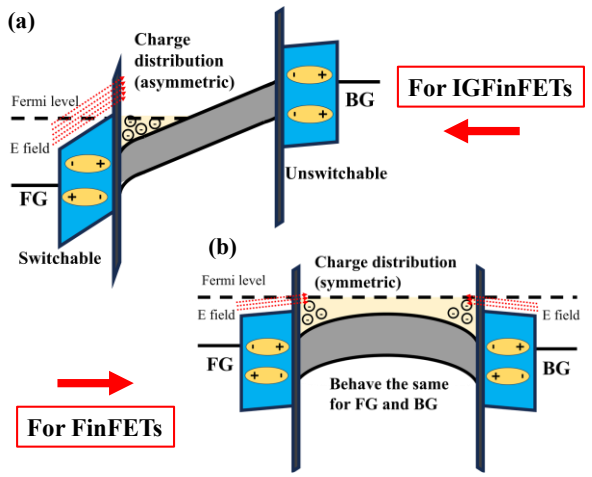

Fig. 7. Band diagram for n-FeIGFinFET under (a) IG mode with bias at FG only (BG grounded) and (b) CG mode with bias at both FG and BG. The non-symmetric electric field distribution paves the way for independent storage for FeIGFinFET. Notice also that with BG bias applied, carrier concentration at the BG side further decreases, eliminating the leakage path near the BG.

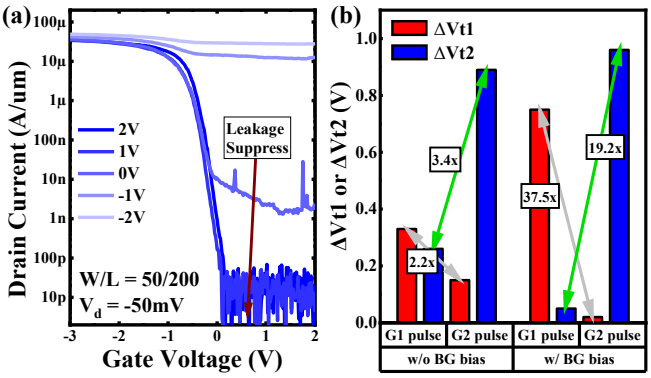

Fig. 8. The effects of BG biasing in p-FeIGFinFET. (a) Transfer characteristics with different BG biases. The "OFF" state leakage is greatly suppressed with positive BG bias, while the "ON" state current remains essentially unchanged. (b) Measured V_T shifts summarized. With the help of BG biasing (+1V), the difference between same-side and opposite-side V_T shifts is enlarged.

BG biasing is also essential for leakage suppression, as illustrated in **Fig. 8(a)**. Take pFET for example, the off-state leakage is dramatically suppressed with positive BG biasing, as the leakage near the back gate side is suppressed. Carrier concentration at the back side is significantly reduced with BG biasing (**Fig. 7**). With BG biasing, the phenomenon of V_T shifting by program/erase pulse application is much more pronounced (**Fig. 8(b)**), thereby enhancing the independent storage capability of FeIGFinFETs.

IV. Special Applications of FeIGFinFET

A. Program-Inhibit Mode Memory Operation

To explore the design of FeIGFinFETs array, program-inhibit simulation of a 2*2 crossbar array is performed with Sentaurus Device 3D TCAD. The high resistance state (HRS) and low resistance state (LRS) indicate the storage state of the selected device. In **Fig. 9(a)**, a program pulse has been sent in to change the state of the selected cell from 12.5s to 13.5s. The results show a larger current ratio of programmed to non-programmed cells for FeIGFinFETs in IG mode than in CG mode, thanks to the BG biasing in IG mode to suppress unwanted leakage current for the inhibited devices and

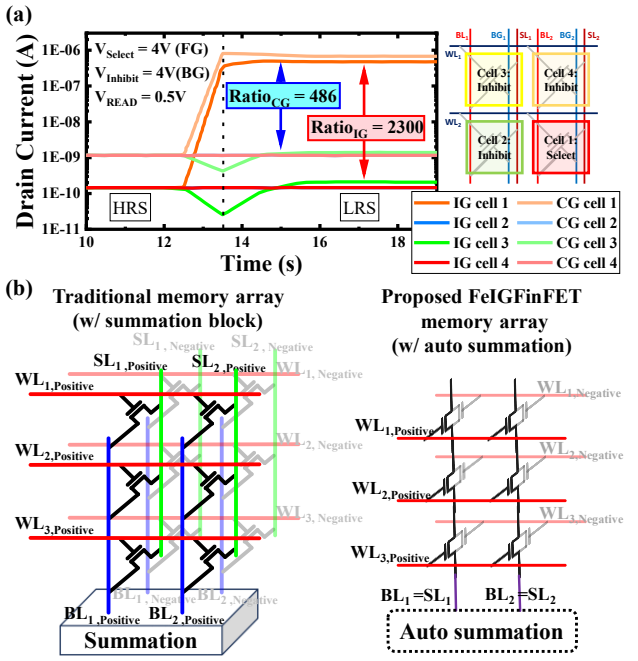

Fig. 9. (a) Mixed-mode TCAD simulation of program-inhibit mode FeIGFinFET memory array operation. A larger current ratio between selected and program-inhibited cells is achieved with IG operation mode than CG mode due to leakage suppression. (b) Proposed FeIGFinFET architecture for weighted sum operation, with positive/negative weights respectively stored on two gate sides of a single device.

increase the I_{on}/I_{off} ratio for the selected devices during data write operation. Note that the initial states for all the devices are set as HRS, and cell 2 and cell 4 have identical results because of the same voltage difference between nodes.

B. Neural Network (NN) Computing Architecture

Since FeIGFinFETs have the ability to store FE states independently, it can be approximated as two transistors with a shared source/drain, effectively. State summation can, therefore, be achieved naturally. By leveraging this property, a new CIM architecture for FeIGFinFETs is proposed, which performs weighted-sum operations, as illustrated in **Fig. 9(b)**. For conventional NN architecture (shown on the left-hand side), positive and negative weights must be stored on two separate memory devices to represent one signed weight component. When it comes to FeIGFinFETs, two weights can be stored on the same device with minimal interference, not only doubling integration density under the same chip size but also achieve the auto summation thanks to the unique IG structure.

V. Conclusion

FeIGFinFETs are demonstrated with a novel fabrication process that facilitates the integration of both IG and CG devices on a single chip. Measurements taken at R.T. and Cryo T. indicate that the two gate sides can be independently programmed and read. Successful potentiation and depression operation further highlights the potential of FeIGFinFETs for neuromorphic computing. The implementation of BG biasing effectively reduces leakage current. Furthermore, a novel CIM architecture for a FeIGFinFET weighted-sum neural network is proposed, which allows the storage of two weights within a single device. Table 1 benchmarks the different fabrication methods and function achievements for IGFinFETs. In this work we have performed the most complete examination, and the storage of independent information on the front- and back-gates have been experimentally shown for the first time.

Table 1. Benchmarking for IGFinFET technologies [9][10][11][12]

		This work	EDL 2021 [9]	ISCAS 2019 [10]	VLSI 2005 [11]	EDL 2004 [12]
Fabrication process		CMP + Dry etch with selective etch-back	Simulation only	Simulation only	Direct etching	Direct CMP
Device spec	Width/ Length	W: 20nm~50nm L: 50nm~200nm	W: 25nm L: 100nm	W: 6 or 12nm L: 30nm	W: 80nm L: 40um	W: 25~75nm L: 2um
	Fin height	50nm	40nm	--	150nm	230nm
	Oxide thickness	(FE) 10nm HZO + 1.5nm ZrO_2	(FE) 7nm HZO	(NC) 10nm HZO	(no FE) 2nm SiO_2	(no FE) 10nm SiO_2
Characterization temperature		4K to 300K	300K	300K	300K	300K
Application		CIM, Neuromorphic array	PIM	--	Mixer	--

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