Static and Statistical Modeling of LTPS TFTs for Robust Analog Design: Verified Through Amplifier and Comparator Measurements

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***Abstract*—Targeting large-area analog sensing applications, a compact modeling framework is proposed for low-temperature polycrystalline silicon (LTPS) thin-film transistors (TFTs). The model captures both static and statistical characteristics. Five key parameters (K, V_{th}, SS, θ, λ) are extracted per device by fitting measured I_{DS}-V_{DS} curves. Statistical analysis is conducted from both technology-corner and mismatch perspectives. Devices are clustered into fast, typical, and slow technology corners; combined corners are then formed by pairing N-type and P-type classifications, and their distribution across 15cm substrate is analyzed. Mismatch is characterized by analyzing the spatial correlation of TFTs, from which local and global variation coefficients are derived. Circuit-level validation is performed using a folded-cascode operational transconductance amplifier (OTA) and a dynamic comparator, both fabricated in the same LTPS process. Measurements from 45 OTAs and 7 comparators confirm the accuracy and robustness of the model.**

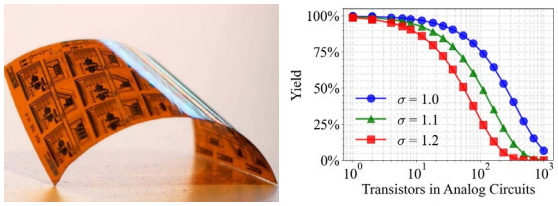
Keywords—Flexible Electronics, Thin-film Transistor, Low Temperature Polycrystalline Silicon, Transistor Model.

I. Introduction

The growing demand for wearable devices and the Internet of Things (IoT) has driven ongoing innovation in integrated circuits (ICs). Most existing ICs are silicon-based, primarily owing to the maturity of silicon fabrication processes [1]. However, the rigidity of silicon chips causes discomfort on the skin, and their high cost per unit area limits scalability. Certain applications, such as multi-electrode recording [2] and ultrasound imaging [3], require flexible large-area sensor arrays to achieve wide-area monitoring and broad fields of view. These requirements pose significant challenges for the development of conformal sensing systems.

Thin-film transistors (TFTs), as key components of flexible electronics, have attracted increasing attention for addressing the limitations of rigid, high-cost silicon circuits. Their advantages—including low fabrication cost, lightweight, conformability, and mechanical flexibility—make them well-suited for large-area, wearable systems [4][5][6]. An example of this is a flexible TFT die [7], as shown in Fig. 1(a). Among various TFT technologies, low-temperature polycrystalline silicon (LTPS) offers higher carrier mobility (50–100 cm²/V·s) compared to amorphous silicon (~1 cm²/V·s) and oxide semiconductors such as IGZO (~10 cm²/V·s) [8][8], thereby enabling higher performance and greater circuit integration. Consequently, LTPS has been increasingly adopted in sensing circuits for emerging flexible applications [9][10][11][12].

Despite its advantages, LTPS suffers from considerable device variation, primarily due to the diverse and complicated grain distribution in polycrystalline silicon films [13]. In analog signal processing circuits, such variation causes device mismatch, which in turn leads to offset in amplifiers and comparators, as well as nonlinearity and inaccuracy in data converters [14]. The following pessimistic case illustrates the mismatch impact on yield: a transistor with a parameter x is functional only when x lies within a window of ±3 units, corresponding to a 3σ range when $\sigma = 1$. A circuit is considered to fail if any transistor's parameter x falls outside the 3σ range. As the standard deviation σ increases, or as more transistors are integrated in an analog module, the probability of failure—and hence yield loss—increases rapidly, as shown in Fig. 1(b). Moreover, since TFTs are typically spread over large areas, spatial variation across the substrate introduces additional uncertainty. These challenges highlight the need for accurate static modeling and statistical variation characterization of LTPS TFTs.



(a) (b)

Fig. 1. (a) Photograph of a flexible TFT die [7]. (b) Estimated yield as a function of transistor variation and circuit size.

To enable robust analog circuit design under these challenges, this work presents a comprehensive characterization of LTPS TFTs through static and statistical modeling. Key parameters are extracted by fitting current–voltage (I–V) characteristics, and clustering is applied to identify technology corners and analyze their distribution across a 15cm wafer. The spatial correlation of transistor mismatch is quantified, from which local and global variation parameters are derived. The proposed models are validated by comparing simulation results with measurements of amplifiers and comparators fabricated across multiple wafers.

The remainder of this paper is organized as follows. Section II presents the static and statistical modeling framework. Section III describes the parameter extraction and variation analysis. Section IV provides both measurement and simulation results from fabricated analog blocks. Finally, Section V concludes the paper.

II. Static and Statistical Model

A. TFT Static Model

Various static models have been developed for TFTs to address different trade-offs, including model complexity, physical accuracy, and compatibility with circuit simulators [15][16]. One of the simplest approaches adapts the quadratic I–V expression from crystalline silicon devices. However, this formulation does not accurately capture subthreshold behavior, and often suffers from convergence issues. More advanced physical models, derived from charge-based or surface-

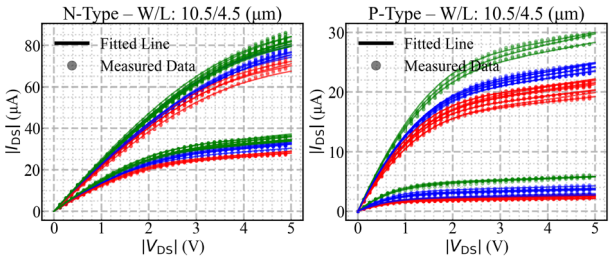


Fig. 2. Measured and fitted I_{DS}–V_{DS} curves at $|V_{GS}|$ = 3.3 V and 5 V. Colors indicate clustered corners: fast(green), typical(blue), slow(red).

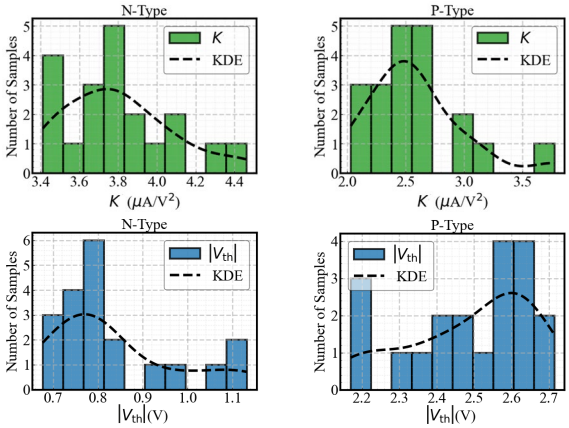


Fig. 3. Histograms and kernel density estimations (KDE) of K and $|V_{th}|$.

potential theories, generally offer improved accuracy. Nevertheless, their idealized assumptions can lead to discrepancies with experimental data, and their equations typically require more than ten fitting parameters, demanding large datasets and significant fitting effort [17].

This work adapts the compact model proposed in [18], which achieves sufficient accuracy with six parameters (K, V_{th}, SS, θ, λ, γ). The static I–V characteristics are described by:

$$I_{DS} = \frac{\mu_0 C_{ox}}{2}\frac{W}{L}\frac{1}{1+\theta V_{GSTe}}\left(V_{GSTe}^{2+\gamma} - V_{GDTe}^{2+\gamma}\right)(1+\lambda V_{DS}) \quad (1)$$

where μ_0 is the carrier mobility, C_{ox} is the gate insulator capacitance, W/L is the channel width-to-length ratio, γ is the mobility enhancement factor, θ is the velocity saturation coefficient, and λ is the channel length modulation parameter. The product $K = \mu_0 C_{ox}$ is known as the current factor. The effective gate-source and gate-drain voltages, V_{GSTe} and V_{GDTe}, are defined by an asymptotic interpolation function to model subthreshold behavior:

$$V_{GXTe} = 2\,SS\,log_{10}\left(1 + 10\hat{}\left(\frac{V_G - V_X - V_{th}}{2SS}\right)\right) \quad (2)$$

where X represents the source or drain terminal, and SS is the subthreshold slope.

B. TFT Statistical Model

The process of mismatch generation is analyzed in [14] using spatial Fourier analysis. The standard deviations of K and V_{th} can be expressed as:

$$\sigma^2\left(\frac{\Delta K}{K}\right) = \frac{A_K^2}{WL} + S_K^2 D^2 \quad (3)$$

$$\sigma^2(\Delta V_{th}) = \frac{A_{V_{th}}^2}{WL} + S_{V_{th}}^2 D^2 \quad (4)$$

where A_K, $A_{V_{th}}$, S_K and $S_{V_{th}}$ are process-dependent constants, and D is the spacing between transistors. The coefficients A_K and $A_{V_{th}}$ characterize local variation, which is dependent on transistor size and particularly critical in pixel-level circuits.

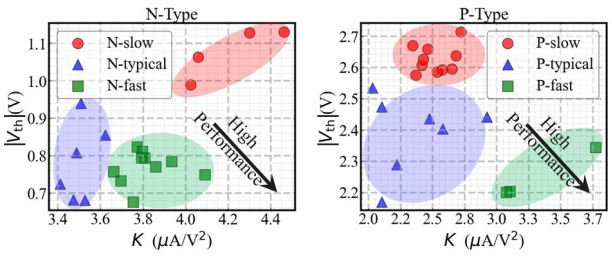


Fig. 4. Distribution of technology corners in the K–V_{th} space.

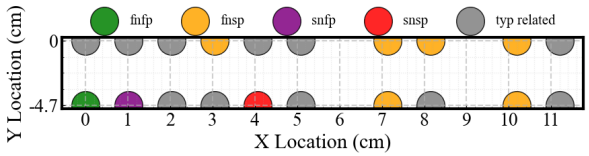


Fig. 5. Distribution of combined N/P technology corners on the plate.

In contrast, S_K and $S_{V_{th}}$ reflect global variation, which becomes increasingly significant as the circuit area scales up.

III. Device Characterization

To characterize static and statistical behavior, both N-type and P-type TFTs with a W/L ratio of 10.5 μm/4.5 μm were fabricated using a commercial LTPS process. The devices were arranged in a two-row array with a vertical spacing of 4.7 cm. Each row contains 12 samples spaced 1.02 cm apart along the x-axis, and each sample consists of one N-TFT and one P-TFT placed adjacently. Samples located at x = 6.12 cm and 9.18 cm show significant deviation from the rest and were excluded from subsequent analysis.

A. TFT Static Characterization

Based on the static model described in Section II, five key parameters (K, V_{th}, SS, θ, λ) are extracted by fitting the measured I_{DS}–V_{DS} curves for each device using the damped least-squares (DLS) method. Extraction is performed at $|V_{GS}|$ = 3.3 V and 5 V, which are typical bias conditions for LTPS TFTs in analog applications operating under a 10 V supply [19]. The mobility enhancement factor γ is excluded from fitting, as the enhancement in IGZO due to trap-state filling is typically not present in LTPS, where mobility is limited by grain-boundary [20]. As shown in Fig. 2, the fitting results exhibit good agreement with measurement data, with an average determination coefficient R^2 of 0.998. The extracted K and V_{th} parameters are summarized as histograms in Fig. 3. Their typical values are determined to be 3.8 μA/V^2 and 0.8 V for N-TFTs, and 2.5 μA/V^2 and –2.6 V for P-TFTs, respectively, with corresponding carrier mobilities of 112 cm^2/V·s (N-type) and 74 cm^2/V·s (P-type).

B. TFT Statistical Characterization

While device variation is limited in mature technologies, it can be very significant for emerging ones such as LTPS TFTs. To ensure functional reliability and improve yield, worst-case scenarios and statistical variations must be considered early in the design process, typically through corner and Monte Carlo simulations. Corner simulation captures performance extremes using representative parameter sets from pre-defined technology corners, while Monte Carlo simulation evaluates statistical impact based on parameter distributions.

To characterize performance variation extremes, a Gaussian mixture model (GMM) is employed to cluster 20 transistors of each type into three technology corners—fast,

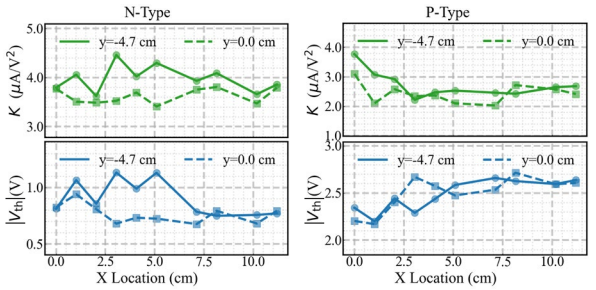


Fig. 6. Extracted K and $|V_{th}|$ values across different sample positions.

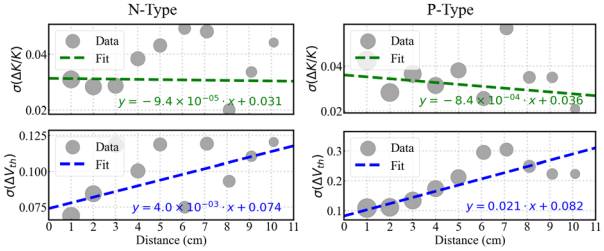


Fig. 7. Standard deviation of $\Delta K/K$ and ΔV_{th} versus device spacing, with marker size indicating data count.

typical, and slow—based on their I_{DS} values. The clustering results are visualized in Fig. 4, using extracted K and V_{th} values. P-TFTs exhibit clearer clustering than N-TFTs, as also reflected in Fig. 2. The corner parameters are obtained by calculating the centroid of each cluster in the K–V_{th} space. Devices with higher K and lower V_{th} exhibit stronger driving capability and thus higher performance. The resulting corner distribution follows the expected performance trend.

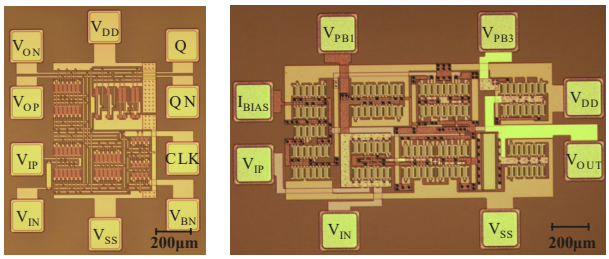
Based on device locations, the technology corners identified through clustering are mapped across the substrate to reveal their spatial distribution. Furthermore, N-TFT and P-TFT corners are combined to define mismatch corners such as fast-N/slow-P (fnsp), slow-N/fast-P (snfp), as illustrated in Fig. 5. Among them, the fnsp corner appears most frequently, indicating that special attention should be paid to this corner in circuit design to ensure robustness.

To examine the spatial correlation of transistor mismatch, the extracted K and V_{th} values are plotted along the x-axis by device positions, as shown in Fig. 6. While both parameters exhibit significant overall variation, adjacent samples show relatively small differences.

To quantify how device variation relates to spacing, a distance matrix is constructed by calculating the pairwise distances between all transistors to all the rest. For each pair, relative variations $\Delta K/K$ and ΔV_{th} are computed as a function of distance. The corresponding standard deviations, $\sigma(\Delta K/K)$ and $\sigma(\Delta V_{th})$, are evaluated at each distance and plotted in Fig. 7, with marker size indicating the data count. Linear regression is applied to extract spatial trends. As distance approaches zero, the extrapolated local standard variation for devices sized 10.5 µm/ 4.5 µm is approximately 3.1% in $\sigma(\Delta K/K)$ and 74 mV in $\sigma(\Delta V_{th})$ for N-TFTs, and 3.6% and 82 mV, respectively, for P-TFTs. No clear global trend is observed in $\sigma(\Delta K/K)$, while $\sigma(\Delta V_{th})$ increases with distance, at rates of approximately 4 mV/cm for N-TFTs and 21 mV/cm for P-TFTs. These results suggest that global variation becomes significant only at centimeter-scale circuits, whereas local variation remains dominant at smaller scales.

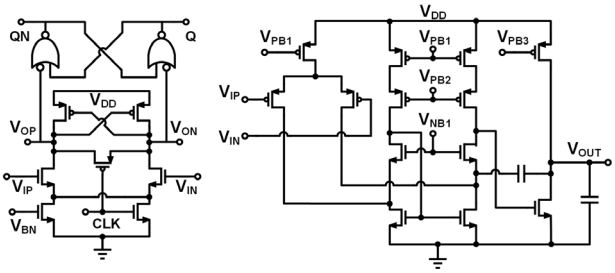
IV. Circuit-Level Validation

To validate the static and statistical models at the circuit level, a corresponding Verilog-A transistor model was



(a) (b)

Fig. 8. Circuit micrographs of (a) the comparator and (b) the OTA.



(a) (b)

Fig. 9. Circuit schematics of (a) the comparator and (b) the OTA.

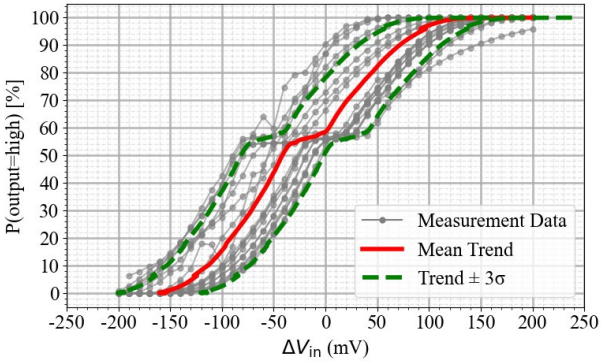


Fig. 10. Comparator output probability vs. input differential voltage.

developed using the technology corner parameters. Gaussian variations were applied to K and V_{th} in Monte Carlo simulations, based on the extracted statistical parameters $\sigma(\Delta K/K)$ and $\sigma(\Delta V_{th})$. With this model, two representative analog blocks—a dynamic comparator and a folded-cascode OTA—were designed and fabricated using the same LTPS process. Their chip micrographs and circuit schematics are shown in Fig. 8 and Fig. 9, respectively. I_{BIAS} in Fig. 8(b) generates the on-chip V_{PB2} and V_{NB1} used in Fig. 9(b).

A statistical approach was used to characterize the dynamic comparator, as its nonlinear operation significantly changes transistor operating points during comparison. The input-referred offset is defined as the differential input $\Delta V_{in}=V_{IP}-V_{IN}$ that results in a 50% probability of a high output. The comparator was measured using a 10 V supply, a 3 V common-mode input, and a 100 kHz clock. To extract output probability, ΔV_{in} was applied as a staircase ramp signal sweeping from –200 mV to +200 mV in 10 mV steps. Each step was held for 0.5 s to allow 1,000 comparison cycles for probability computation, as well as data logging. Seven samples were measured, with three repeats each.

Fig. 10 shows the extracted output probability versus input differential voltage across all measurements. The mean trend reveals a systematic offset of approximately –40 mV, caused by asymmetric loading in the differential branches. Most curves fall within the ±3σ envelope, where σ was obtained from 100 Monte Carlo simulations. The wider distribution in

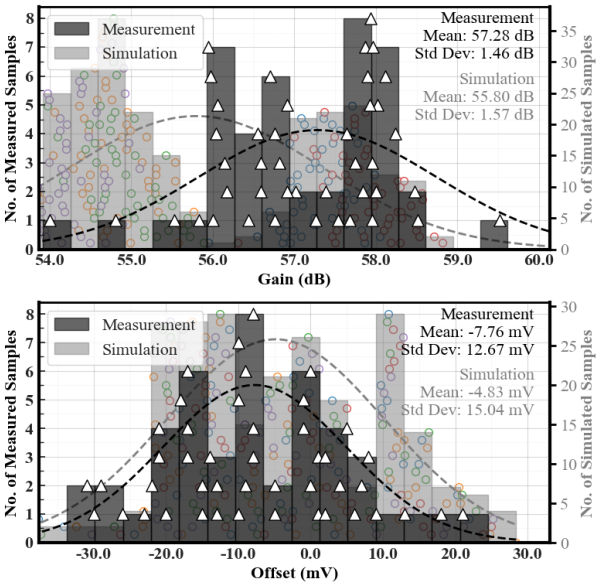


Fig. 11. Histogram of measured and simulated OTA DC gain and offset.

measurements may result from load capacitance variation in the preamplifier stage.

The folded-cascode OTA was characterized for DC gain and offset under a 12 V supply. Fig. 11 summarizes measured and simulated results for both metrics, based on 45 samples and 50 Monte Carlo simulations per technology corner. Triangular markers are measured data, while circular points are from simulation, with their color indicating the combined technology corners: fnfp (red), fnsp (blue), typical (green), snfp (purple), and snsp (yellow).

DC gain was measured by applying a 1 mV differential AC input and recording the output amplitude. The measured gain has a mean of 57 dB with a standard deviation of 1.5 dB. Simulated gain values were obtained using global variation coefficients across all technology corners, as the OTAs are distributed across multiple wafers and locations within each wafer. Most measured data fall into the fnsp corner (blue), highlighting this corner's significance in design. The larger spread in measured gain may result from wafer-to-wafer variations, which are not included in the model.

Offset was derived by configuring the OTA in a unity-gain feedback loop and measuring the voltage difference between V_{IP} and V_{IN}. The measured offset shows a standard deviation of 12.7 mV, while simulation predicts 15 mV using a local variation setup applied to all corners. Local variation was used here, as offset is primarily determined by mismatch within the circuit itself. The small discrepancy between measurement and simulation may be due to the dummy input transistors used in the layout.

V. Conclusion

This work presents a compact and accurate modelling framework for LTPS TFTs, capturing both static characteristics and statistical variations. Technology corners and variation parameters are extracted through fitting, clustering, and spatial correlation analysis. The model is validated against measurements from 45 OTAs and 7 comparators, demonstrating a strong agreement. These results confirm the model's applicability for robust analog design in large-area sensing systems based on LTPS technology.

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References

[1] Q. Lin et al., "Wearable multiple modality bio-signal recording and processing on chip: A review," *IEEE Sens. J*, vol. 21, no. 2, pp. 1108–1123, Jan. 2021.

[2] M. E. J. Obien et al., "Revealing neuronal function through microelectrode array recordings," *Front. Neurosci.*, vol. 8, Art. 423, Jan. 2015.

[3] M. Dandekar, K. Myny and W. Dehaene, "An all LTPS-TFT-based charge-integrating amplifier for sensor-array readout circuit on flexible substrate," *IEEE Open J. Solid-State Circuits Soc.*, vol. 2, pp. 208–216, 2022.

[4] M. Zulqarnain and E. Cantatore, "Analog and mixed signal circuit design techniques in flexible unipolar a-IGZO TFT technology: Challenges and recent trends," *IEEE Open J. Circuits Syst.*, vol. 2, pp. 743–756, 2021.

[5] E. Genco et al., "An EMG Interface Comprising a Flexible a-IGZO Active Electrode Matrix and a 65-nm CMOS IC," *IEEE J. Solid-State Circuits*, vol. 58, no. 11, pp. 3138–3149, Nov. 2023.

[6] M. Fattori et al., "Advanced Sensing Systems Exploiting the Integration of Flexible and Large-Area TFTs with Si-CMOS Technology," in *Proc. IEEE Custom Integr. Circuits Conf. (CICC)*, Denver, CO, USA, Apr. 2024, pp. 1-8

[7] N. P. Papadopoulos et al., "Toward Temperature Tracking With Unipolar Metal-Oxide Thin-Film SAR C-2C ADC on Plastic," *IEEE J. Solid-State Circuits*, vol. 53, no. 8, pp. 2263-2272, Aug. 2018.

[8] T.-C. Chang et al., "Flexible low-temperature polycrystalline silicon thin-film transistors," *Mater. Today Adv.*, vol. 5, Art. 100040, Mar. 2020.

[9] D. Kong et al., "New Capacitive Active-Pixel Sensor Based on LTPS-TFT Backplane Technology for Fingerprint Recognition," in *SID Symp. Dig. Tech. Papers*, vol. 52, pp. 1074–1077, 2021.

[10] A. Rahaman, H. Jeong and J. Jang, "A High-Gain CMOS Operational Amplifier Using Low-Temperature Poly-Si Oxide TFTs," *IEEE Trans. Electron Devices*, vol. 67, no. 2, pp. 524-528, Feb. 2020.

[11] S. M. Sadati Faramarzi et al., "Thin-Film Transistor-Based Sensor Interface Circuits Enabling Distributed Local In-Module Solar Cell Temperature Monitoring," *IEEE J. Solid-State Circuits*, vol. 59, no. 1, pp. 307–315, Jan. 2024.

[12] H. Zhang et al., "A Fully LTPS-TFT-Based Bidirectional Biomedical Interface Circuit for Large-Area Healthcare Applications," *IEEE J. Flex. Electron*, vol. 3, no. 12, pp. 526–532, Dec. 2024.

[13] Y.-H. Tai et al., "A Statistical Model for Simulating the Effect of LTPS TFT Device Variation for SOP Applications," *J. Display Technol.*, vol. 3, no. 4, pp. 426–433, Dec. 2007.

[14] M. J. M. Pelgrom, A. C. J. Duinmaijer and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, Oct. 1989.

[15] N. Lu et al., "A Review for Compact Model of Thin-Film Transistors (TFTs)," *Micromachines*, vol. 9, Art. 599, Nov. 2018.

[16] L. Li et al., "Generalized Rapid TFT Modeling (GRTM) Framework for Agile Device Modeling With Thin-Film Transistors," *IEEE J. Flex. Electron.*, vol. 3, no. 5, pp. 190–196, May 2024.

[17] O. Marinov et al., "Organic Thin-Film Transistors: Part I—Compact DC Modeling," *IEEE Trans. Electron Devices*, vol. 56, no. 12, pp. 2952–2961, Dec. 2009.

[18] F. De Roose et al., "Dual-gate self-aligned a-InGaZnO transistor model for flexible circuit applications," in *Design, Autom. & Test Eur. Conf. & Exhib. (DATE)*, Florence, Italy, Mar. 2019, pp. 25–29.

[19] F. De Roose et al., "Multimodal Intelligent Display Backplane Blocks," in *SID Symp. Dig. Tech. Papers*, vol. 55, pp. 1691–1694, 2024.

[20] K. Jang et al., "Improvement of electrical performance in P-channel LTPS thin-film transistor with a-Si:H surface passivation," *Mater.*, vol. 12, no. 1, Art. 161, Jan. 2019.