A 200MS/s, 77dB-DR Two-Stage SAR ADC with Asynchronous Pipelining and Reference Snubbers

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***Abstract*—This paper presents a low-noise ADC for low-power, low-latency signal acquisition chains. It features asynchronous pipelining to improve backend precision while minimizing the conversion latency to 8ns, independent of sample rate. Domain-crossing reference snubbers address settling and ringing limitations of the precision references, for the sub-ADCs and the floating-inverter residue amplifier. Implemented in 40nm CMOS, the proposed design achieves a 71.1dB peak SNDR and 77dB DR at 200MS/s, consuming 5.8mW. It advances the speed of state-of-art low-noise SAR ADCs by 2.5× and delivers a best-in-class noise-level and DR with a 179.4dB $FoM_{S,DR}$.**

***Index Terms*—signal chain, low-noise, latency, asynchronous pipeline, SAR ADC, SAR reference, residue amplifier.**

I. Introduction

The growth of pipelined SAR ADCs resulted in a wide array of fully dynamic, low-power ADCs [1]–[5]. Nonetheless, the impact of this progress on system-level efficiency has become relatively limited. Signal pre-processing in the system's analog front-end (AFE) heavily dominates the overall system power, mainly because of the required linear, high gain before the ADC [6], as Fig. 1 shows. Therefore, low-noise ADCs are key for the next generation of signal acquisition chains. For the same performance, less AFE gain is required because the signals of interest received at a low-noise ADC can be smaller. In addition, the high dynamic range (DR) makes the ADC robust to saturation from interfering or wandering signals, simplifying the AFE more. Thus, low-noise/high-DR ADCs offer a critical relaxation of signal pre-processing resources, and will significantly improve system-level efficiency.

However, achieving such low-noise performance using SAR-based ADCs is not trivial when targeting a high sample rate. Pushing for fast bit trials and smaller residue voltages does not only involve tighter noise and metastability design constraints: reference settling and ringing issues become problematic, causing additional precision degradation. Consequently, these targets force the SAR ADC beyond the speed and power efficiency limits of its technology.

To stretch these limits, pipelining can be employed, but from a system-level perspective this is not always desired. Low latency and frequency scalability are critical specifications for modern applications requiring short round-trip delays or rapid feedback [7]. In contrast, pipelining spreads out conversion time over multiple clock cycles, essentially sacrificing system latency for ADC performance. This leads to an undesirable trade-off between the achievable sample rates and latency, potentially restricting the application at system-level.

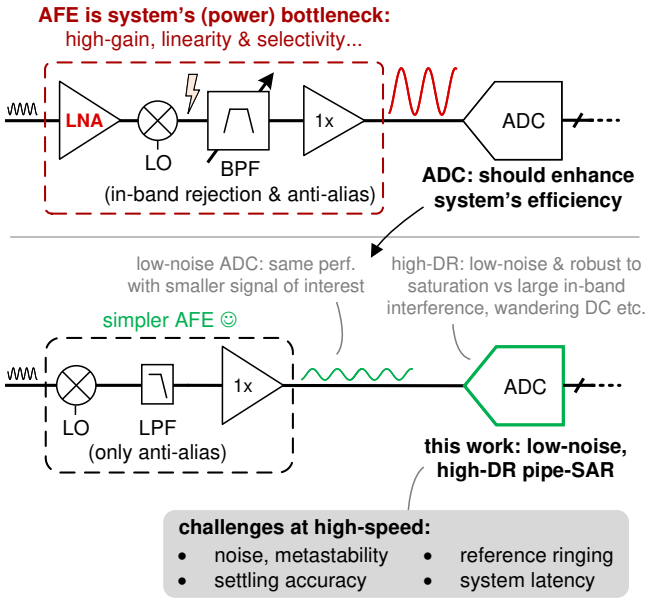

Fig. 1. Signal pre-processing in the AFE dominates system efficiency of receiver (or sensor) chains. Low-noise/high-DR ADCs can ease this AFE bottleneck, but pose design challenges at high speeds.

To address the above needs and challenges, this work presents a two-stage SAR ADC with asynchronous pipelining, "snubber"-based reference stabilization and a fast floating-inverter residue amplifier (RA). The 40nm CMOS prototype ADC achieves <110μV_{RMS} input-referred noise and 77dB DR at 200MS/s, improving the state-of-the-art by >4dB in DR and 2.5× in sample rate, while consuming only 5.8mW. In addition, the prototype ADC minimizes its latency to 8ns at *any* sample rate up to 200MS/s, uniquely supporting the next-generation of low-power signal acquisition chains, both at higher speeds and with low latency.

II. ADC Architecture

Fig 2. shows the 14b ADC architecture, featuring a first stage 7b SAR ADC and 16×-gain RA, followed by a backend 8b SAR ADC with 1b overrange and 0.25× reference scaling. For high speed, both sub-ADCs start their conversion with a separate, fast MSB comparator, eliminating the signal transfer delay due to bottom-plate sampling. A redundant bit trial is inserted in each sub-ADC to allow incomplete CDAC settling. For example, the timers of the first CDAC (1.8pF)

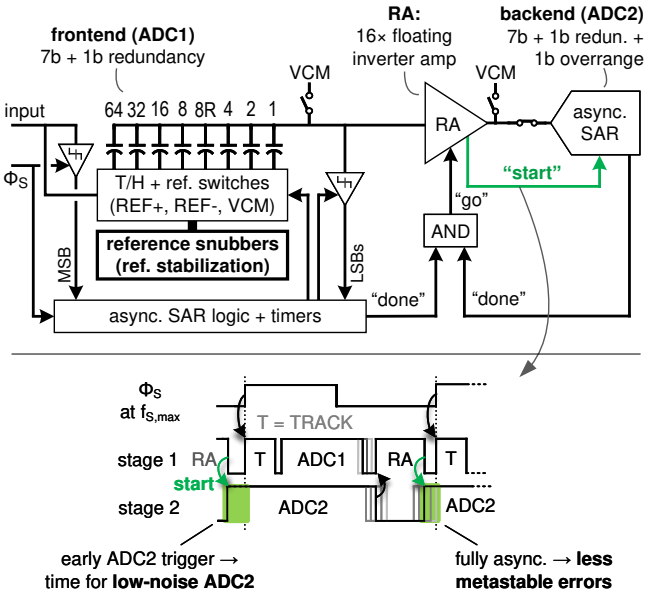

Fig. 2. Overview and simplified timing of the proposed two-stage SAR ADC.

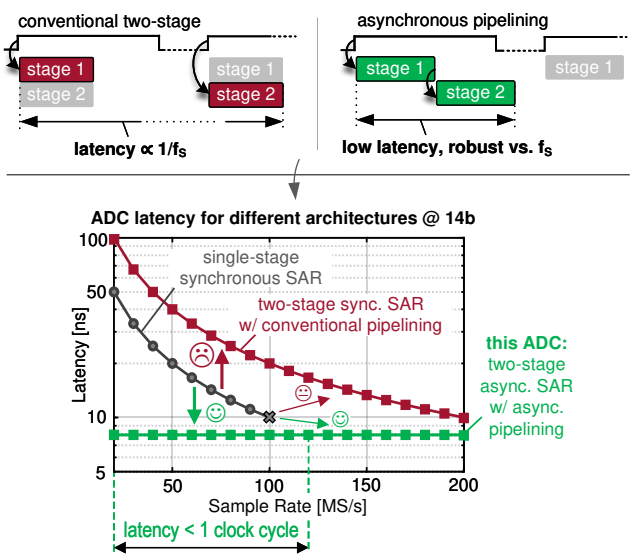

Fig. 3. Comparison between conventional (synchronous) pipelining and asynchronous pipelining from a latency and sample rate perspective.

safely allocate less than 3 DAC time-constants during most bit trials, saving almost 55% settling time. Dynamic logic in the asynchronous state machines further lowers the critical path delay, resulting in a 200ps bit trial time on average in the first stage, including DAC settling and logic delay.

A. Asynchronous Pipelining

With the above techniques, a conventional two-stage SAR still faces speed and precision limitations. Extra timing margin covers for the conversion time uncertainty of asynchronous sub-ADCs, but commonly leads to excessive idle time after the RA. Moreover, the backend ADC struggles to accommodate the low-noise, low-amplitude comparisons and the declining redundant error correction range towards the final bits.

Conventionally, the start of the backend ADC synchronizes to the next sampling pulse. In contrast, the backend ADC in this design asynchronously starts as soon as the RA finishes, as shown in Fig. 2 (bottom). This asynchronous pipelining typically aims to reduce clock power and realizes an adaptive sample rate [8], [9]. However in this ADC, this approach is leveraged to overcome the aforementioned limitations. The immediate conversion start of the backend ADC eliminates all idle time. The backend ADC uses the early start to increase its decision time, reducing the noise of the final comparisons to $<20\mu V_{RMS}$, input-referred. Furthermore, the probability of backend metastability errors is greatly reduced, because the available time margin of a metastable decision is increased by 2×. Altogether, it avoids the need for a high-speed, power-hungry comparator or a multi-bit/cycle architecture.

B. Low Latency and Frequency Scalability Aspects

Asynchronous pipelining eliminates the need for an external clock triggering the backend and breaks the latency trade-off of conventional pipelining, offering significant additional benefits for frequency scalability (Fig. 3). In this ADC it realizes a low latency of 8ns, robust against changes in sample rate. The latency is even less than a single clock cycle when running at <120MS/s, supporting low-power event-driven applications. Moreover, the backend ADC and the first stage are not simultaneously active at reduced sample rates, making the ADC less susceptible to internal crosstalk.

III. Circuit Design and Implementation Details

A. RC Snubber Reference Stabilization

Unsettled SAR references prevent full-precision residue handover in multi-stage SARs, strongly limiting performance at high sample rates. Stabilization techniques based on bit-wise charge neutralization exist, but these techniques only account for the signal-dependent charge drawn from the references for conversion. However, as Fig. 4 (left) shows, low-noise CDACs need large switches for high settling speed, resulting in another, additional charge injection on the references.

A key observation is that this additional charge must return via two separated domains. Standard decoupling creates unpredictable return path currents (via split grounds, on-chip parasitic supply grid inductance, any possible bondwires etc.). This results in ineffective damping, or even aggravates ringing, especially limiting high-speed, low-noise SAR ADCs.

In this ADC, domain-crossing reference snubbers passively suppress this additional reference ringing (Fig. 4, right). Capacitors C_{SNUB} act as local charge reservoirs at the CDAC. A small series resistor R_{SNUB} provides damping and prevents unwanted high-frequency crosstalk, acting as a relatively high impedance to any "noise" originating from VDD. 1pF capacitors with a $\sim 30\Omega$ series resistor are locally placed across the switch driver supplies (VDD/VSS) and references (VREF+/-) in both sub-ADCs. Simulations show that the proposed RC snubbers minimize reference ringing to $<150\mu V_{pp}$ in the first stage and are very robust to uncertainty of on-chip parasitic inductance (Fig. 4, bottom).

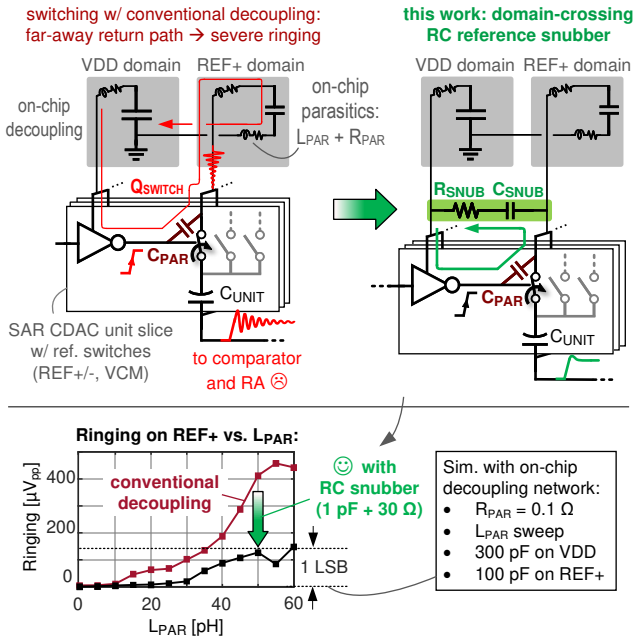

Fig. 4. Proposed RC snubbers for reference ringing due to feedthrough charge of low-noise SAR CDAC switching, and simulated ringing amplitude.

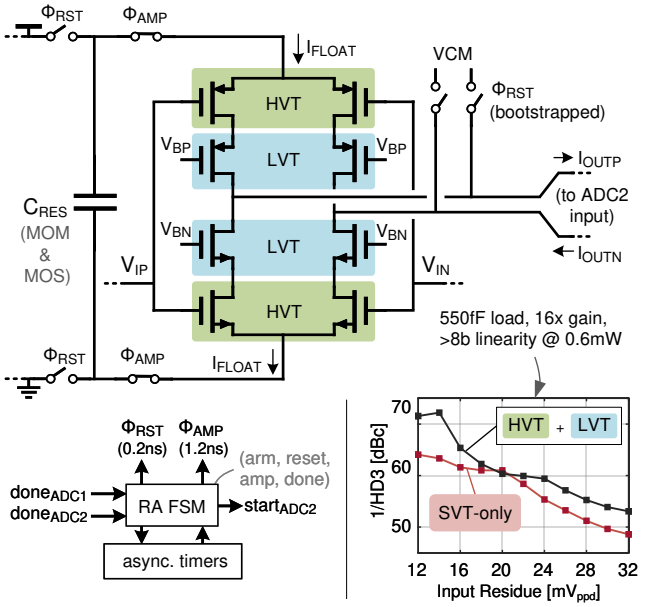

Fig. 5. FIA-based RA with asynchronous logic, and simulated linearity up to max. input residue voltage ($32mV_{ppd}$ for 1b interstage overrange).

B. Residue Amplifier

Dynamic RAs without feedback loop are very sensitive to unsettled residue voltages. The proposed reference snubbers result in a rapidly stabilized residue, enabling the application of an open-loop floating-inverter amplifier (FIA) [9], [10]. Open-loop FIAs are power-efficient and can be robust using PVT-tracking timers. The floating supply guarantees resilience to supply noise and forces that I_{OUTN} = I_{OUTP}, avoiding common-mode feedback. The RA in this work is further optimized for speed and linearity (Fig. 5). C_{RES} is sized 60pF to limit supply quenching, boosting amplification speed. Secondly, the reset switches are bootstrapped to shorten reset time and to reduce parasitic non-linearity. Lastly, it combines high-threshold (HVT) and low-threshold (LVT) transistors for higher linearity. The RA contributes <50μV_{RMS} input-referred noise and achieves 16×-gain in 1.2ns with >8b linearity on a 550fF load, for only 0.6mW including timers and logic.

IV. Measurement Results

The prototype SAR ADC is implemented in a 40nm CMOS process (Fig. 8) and consumes 5.8mW at 200MS/s. The measured performance is shown in Fig. 6 and Fig. 7. The SNDR/SFDR are at 71.7dB/81.1dB for a 7.5MHz input and 66.1dB/77.6dB for a near-Nyquist frequency input with one-time foreground weight calibration (off-chip). At low f_{IN}, the peak SNDR is limited by the remaining INL, and at high f_{IN} by the external ADC input driver. At 200MS/s, the measured input amplitude sweep shows an exceptionally high DR of 77dB, equivalent to only 110μV_{RMS} input-referred noise, enabled by the precision-enhanced backend ADC, rapidly stable references and noise-efficient RA. The proposed architecture also shows a stable SNDR across a wide sample

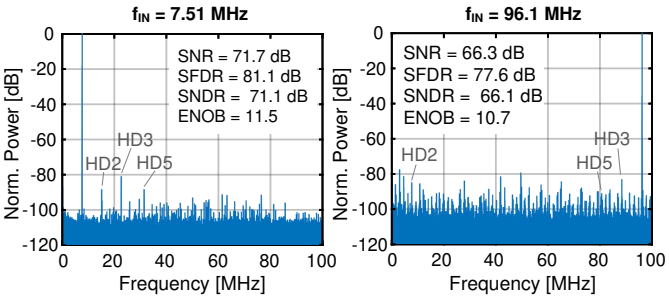

Fig. 6. Measured FFTs for low and high input frequencies: 2^{16}pts at 200MS/s.

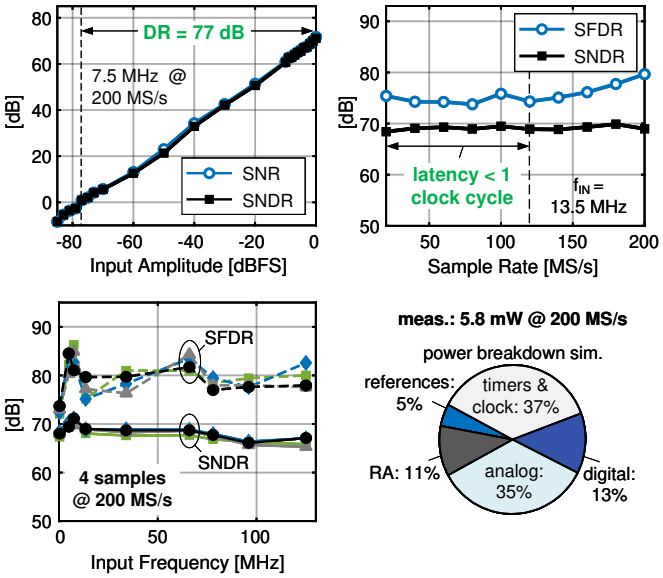

Fig. 7. Measured performance. Top: versus input amplitude and sample rate. Bottom: 4 samples versus input frequency, and power breakdown.

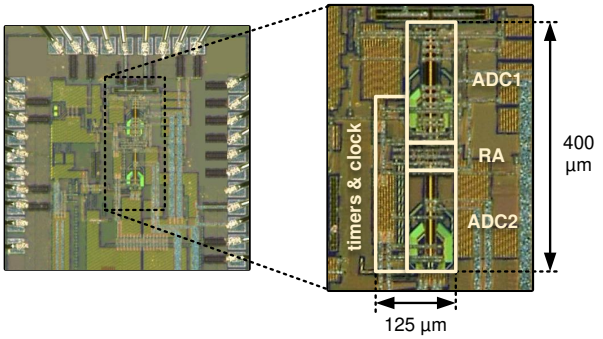

Fig. 8. Chip micrograph.

TABLE I
SUMMARY AND COMPARISON WITH RELEVANT PIPELINED-SARS

	This Work	VLSI'19 [4]	CICC'22 [3]	CICC'20 [5]	ISSCC'24 [1]	VLSI'24 [2]
Architecture	2-stg. SAR async-pipe	2-stage SAR	3-stage SAR	2-stage SAR	2-stage SAR	2-stage SAR
Technology	40nm	40nm	40nm	16nm	22nm	22nm
Resolution [bit]	14	12	13	14	14	13
f_{SAMPLE} [MS/s]	200	200	625	100	200	475
Power [mW]	5.8	3.9	7.05	2.5	2	9.93
Supply [V]	1.1	0.9	1.15	1.2, 0.75	0.9	1
Area [mm^2]	0.044	0.026	0.022	0.102	0.019	0.038
SNDR LF/HF [dB]	71.1/66.1	61.1/62.1	63.8/62.4	N.A./72.6	70.9/70.7	71.5/65.9
FoM_S LF/HF [dB]	173.5/ 168.5	165.2/ 166.2	170.3/ 168.9	N.A./ 175.6	177.9/ 177.7	175.3/ 169.7
DR [dB]	**77**	N.A.	67	70*	72.8	72.1
Tot. Noise [uVrms]	**109.9**	N.A.	363.2*	268.3*	145.8*	175.6*
FoM_S DR [dB]	**179.4**	N.A.	173.5	173	179.8	175.9
Robust Latency#	✓	x	x	x	x	x
Av. Latency$^\Delta$ [ns]	**8**	55*	26*	110*	55*	23*

Total noise is input referred, FoM_S $X = X + 10\log(0.5f_{SAMPLE}/\text{Power})$
*Based on reported data or estimated from figures
#Versus sample rate, $^\Delta$Between 10% and 100% of max. sample rate

rate, and its robust 8ns latency resulted in an observed conversion time *shorter* than one clock cycle up to 120MS/s.

Table I summarizes the performance and shows that the proposed design achieves a superior DR, noise-level and latency compared to other pipelined-SARs at similar speed or resolution. Compared to more SAR ADCs, this work also stands out with at least +4.2dB DR or 2.5× speed, despite its mature technology (Fig. 9). This work demonstrates a 179.4dB $FoM_{S,DR}$ at 200MS/s, greatly advancing the state-of-the-art for low-noise ADCs with DR $\geq$12b, as shown in Fig. 10.

V. CONCLUSION

This work presents a two-stage SAR ADC addressing a need for low-noise, high-DR ADCs in high-performance signal acquisition applications. The ADC specially leverages asynchronous pipelining for noise and latency minimization, and proposes reference snubbers to enable rapid settling and an open-loop FIA RA with tight precision constraints. Achieving 77dB DR at 200MS/s, 179.4dB $FoM_{S,DR}$, and 8ns latency, it offers a best-in-class combination of noise, speed and energy efficiency, paving the way for the next generation of low-power, low-latency signal acquisition chains.

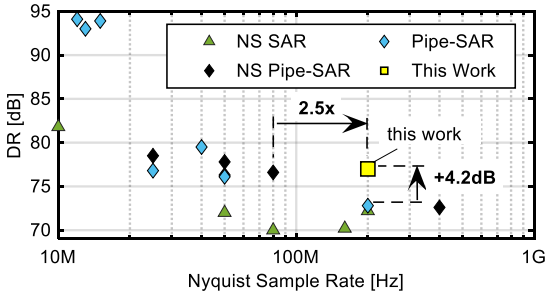

Fig. 9. Comparison with reported DR of SAR-based ADCs $\geq$10MS/s in [11].

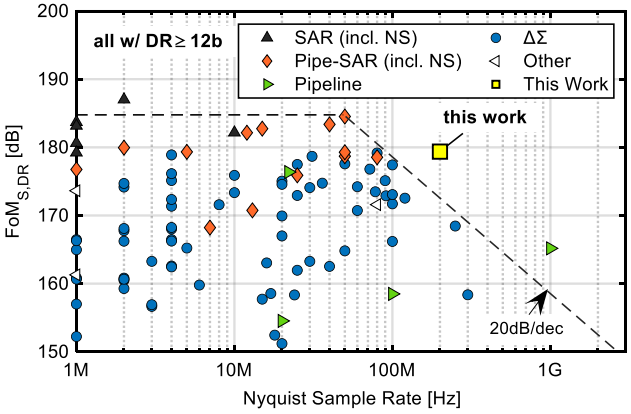

Fig. 10. Comparison with state-of-the-art low-noise ADCs in [11].

ACKNOWLEDGMENT

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