An Accurate Load Balance Single-inductor Bipolar-output Converter Achieving 0.2% Output Common-mode Voltage Variation and 95.2% Peak Efficiency

Li-Jen Huang*, Yu-Tse Shih*, Jie-Lin Wu*, Tay Jye Ni*, Ke-Horng Chen*, Ying-Hsi Lin†, Shian-Ru Lin†, Tsung-Yen Tsai†
Email: lijenhuang.ee13@nycu.edu.tw ytshih0111.ee13@nycu.edu.tw jerrylalla32159@gmail.com khchen@nycu.edu.tw yslin@realtek.com srlin@realtek.com tytsai@realtek.com
*Department of Electrical and Computer Engineering, National Chiao Tung University, Hsinchu, Taiwan,
†Realtek Semiconductor Corp, Hsinchu, Taiwan

***Abstract*—This paper presents an Accurate Load Balance (ALB) Single-Inductor Bipolar-Output (SIBO) converter tailored for micro-LED applications. By generating opposite-slope output currents, the proposed ALB-SIBO significantly suppresses the output common-mode voltage ripple to below 0.2%, aided by a hybrid analog/digital compensator. The converter achieves a peak efficiency of 95.2%. A gate-driven auto-calibration zero current detector (ZCD) is introduced to minimize reverse inductor current during discontinuous conduction mode (DCM), reducing it from −560 mA to under 1 mA. This calibration is selectively activated only during DCM to maximize efficiency. Under dynamic load conditions, the converter demonstrates robust transient performance: an undershoot of just 84 mV with a 7 µs recovery time for a +800 mA/µs load step, and an overshoot of 68 mV with a 9 µs recovery time for a −800 mA/µs load release.**

Keywords—SIBO converter, hybrid converter, load balance, common-mode voltage, high efficiency, high output power, micro led, zero current detector.

I. Introduction

Micro LEDs (µLEDs) are increasingly favored for automotive displays due to their compact size, high efficiency, and exceptional brightness, typically requiring a forward voltage of 3.6V. To effectively drive these µLEDs, especially in automotive environments, DC-DC converters with bipolar outputs are essential. In [1], a SIBO converter is used with constant current (CC) control to power µLEDs. While CC drivers can tolerate variations in V_LED, they suffer from slow response times, making them less suitable for automotive applications where frequent LED switching is required. In contrast, [2] introduces a SIBO converter using constant voltage (CV) control, which offers faster response. However, CV drivers are highly sensitive to V_{LED} fluctuations, potentially leading to visible flicker—an issue unacceptable in automotive lighting. Therefore, a SIBO converter with low output ripple and quiet, stable power supply voltages is essential to eliminate flickering and ensure reliable, high-quality lighting performance in automotive applications.

Fig. 2(a) illustrates the SIBO buck-boost converter architecture presented in [6], along with its associated challenges. While the SIBO converter enables simultaneous regulation of both V_{op} and V_{on} using a single inductor, it suffers from significant common-mode voltage (V_{cm}) ripple. This issue arises because the converter operates across three phases, with V_{op} and V_{on} being charged and discharged in similar slope patterns but in different phases, resulting in pronounced V_{cm} fluctuation. Additionally, the separate charging periods for V_{op} and V_{on} can lead to degraded load transient response. Another critical challenge is the zero current detection (ZCD) circuit, particularly when the SIBO converter is used to drive LED panels that often operate under light load conditions. Under such scenarios, the accuracy and latency of the ZCD circuit become crucial. A large delay in ZCD leads to inefficient switching, increased V_{cm} ripple, and reduced power efficiency. After phase Φ_3, reverse inductor current may continue to discharge V_{on}, causing an undesirable voltage drop. Thus, a low-latency ZCD circuit is essential for improving both efficiency and V_{cm} stability in SIBO converters under light-load operation.

Fig. 2(b) illustrates the simultaneous energy transfer topologies from [3]–[4], which aim to reduce output ripple and minimize output capacitance by simultaneously energizing both V_{op} and V_{on} during phases Φ_1 and Φ_2. Ideally, µLEDs draw current symmetrically from V_{op} to V_{on}, where I_{op} equals I_{on}, resulting in a load mismatch current I_{mis} (= I_{op} − I_{on}) of zero. However, in practical scenarios, power losses and load imbalances can cause I_{op} to slightly deviate from I_{on}. When I_{op} exceeds I_{on} and no additional load-balancing phase Φ_p is included—as in [3]–[4]—V_{op} may fall short of its target value, resulting in insufficient voltage across the LEDs. Conversely, inserting Φ_p to regulate V_{op} can amplify the common-mode voltage variation (ΔV_{cm}), since V_{op} and V_{on} follow similar slope trends during Φ_p, increasing V_{cm} ripple. To address this, the proposed Accurate Load Balance (ALB) SIBO converter introduces an adaptive load balancing mechanism that regulates both outputs accurately while continuously suppressing ΔV_{cm}. Unlike previous approaches, it does so without requiring an extra balancing phase, even when $I_{mis} \neq 0$, thereby achieving precise regulation and low ripple performance.

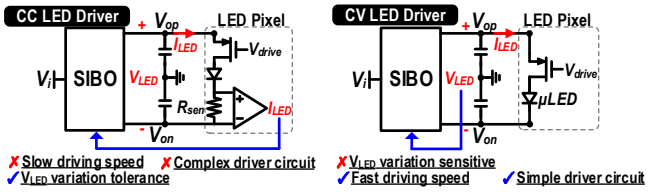


Fig. 1. CC and CV LED driver pros and cons.

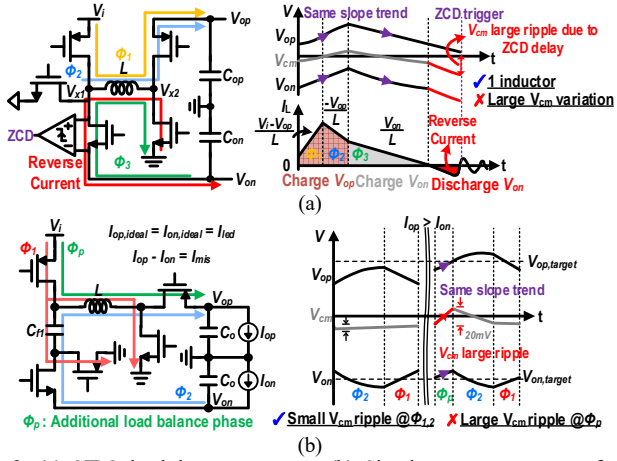


Fig. 2. (a) SIBO buck-boost converter. (b) Simultaneous energy-transferring SIBO converter.

This paper is organized as follows. Section II presents the architecture and operating principles of the proposed ALB-SIBO converter, featuring an analog/digital (A/D) assisted compensator and a gate-driven auto-calibration zero current detector (GDZCD). Section III details the circuit implementations of both the A/D-assisted compensator and the GDZCD. Measurement results from the fabricated test chip, along with a performance comparison against prior works, are provided in Section IV. Finally, Section V concludes the paper.

II. Proposed ALB-SIBO Converter

A. Overall Architecture of ALB-SIBO Converter.

To solve the above mentioned problem, this paper proposes an ALB-SIBO converter in Fig. 3, consisting of 7 switches, one inductor, two flying capacitors, and operates in two phases. By reducing the number of operating phases, the ALB-SIBO converter significantly reduces the switching loss and V_{cm} ripple compared to [3]-[4]. Since both V_{op} and V_{on} are energized simultaneously, the SIBO converter provides quiet supply voltages to μLEDs without the need for large output capacitors. In addition, this paper introduces an A/D assisted compensator to address load imbalance issues. The A/D assisted compensator is composed of M1, M2, an analog controller, and a digital controller, which will source current I_x to V_{x2} or sink current I_y from V_{x1} to ensure proper load balance without additional phases. To prevent reverse inductor current, the ALB-SIBO converter also includes the proposed GDZCD, which will promptly turn off the power switch G_3 for higher efficiency and lower V_{cm} ripple.

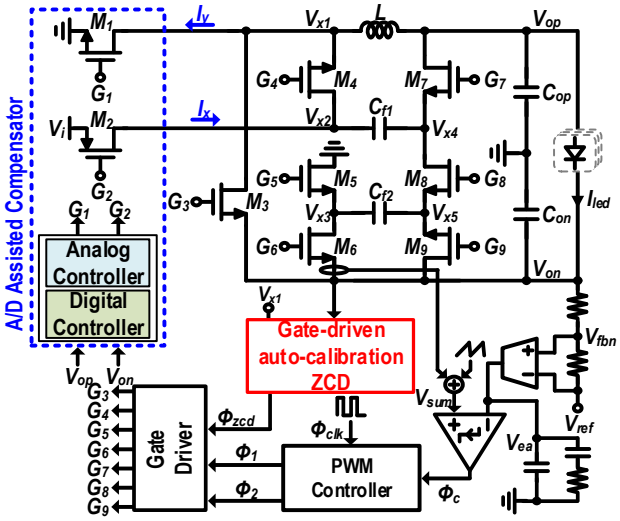


Fig. 3. Overall architecture of ALB-SIBO converter.

B. Digital Operation of the ALB-SIBO

Fig. 4 illustrates the digital operation of the proposed ALB-SIBO converter. During the Φ_1 phase, power switches M_4, M_6, and M_8 are activated by the digital controller, connecting the three passive components in series. In this phase, the inductor (L) and flying capacitor C_{f2} are energized, while C_{f1} is de-energized. This configuration allows the inductor current to simultaneously charge V_{op} and discharge V_{on}. In the Φ_2 phase, switches M_2, M_3, M_5, M_7, and M_9 are turned on, reconfiguring the passive components into a parallel structure. Here, L and C_{f2} are de-energized, and C_{f1} is energized. In this mode, in addition to the inductor delivering energy to both V_{op} and V_{on}, additional current paths through capacitors C_1 and C_2 are formed, helping to reduce inductor current and associated conduction losses. Unlike prior works [3]–[4] that require an additional balancing phase Φ_p to handle output mismatches, the ALB-SIBO maintains low ΔV_{cm} by ensuring that V_{op} and V_{on} follow opposite slope trends in both Φ_1 and Φ_2 phases, as shown in Fig. 4(b). This opposite behavior inherently suppresses V_{cm} ripple without the need for extra switching phases. As a result, the ALB-SIBO tolerates larger load mismatches while maintaining reduced inductor current, achieving lower switching and conduction losses. Moreover, by employing two flying capacitors instead of an extra inductor, the converter reduces the number of high-voltage components and minimizes DC resistance (DCR), improving overall efficiency.

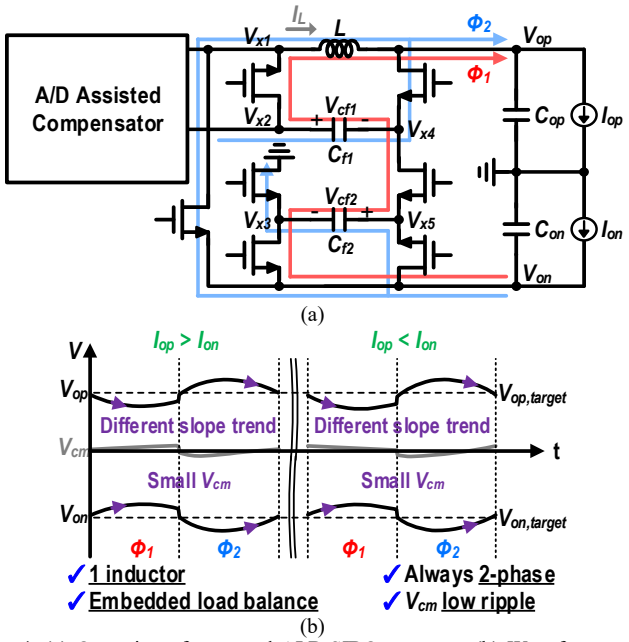


Fig. 4. (a) Operation of proposed ALB-SIBO converter (b) Waveforms and advantages of ALB-SIBO converter.

III. Circuit Implementation

A. Proposed Analog/Digital (A/D) Assisted Compensator

The A/D Assisted Compensator is composed of M_1, M_2, an Analog Controller, and a Digital Controller, which will source current I_x to V_{x2} or sink current I_y from V_{x1} by controlling G_1 and G_2. As shown in Fig. 5, the Analog Controller includes a shared high swing input stage to amplify the difference between level-shifted signals $V_{gnd,ls}$ and $V_{cm,ls}$. The outputs V_{p2} and V_{n2} of the input stage are propagated to Driving Stage I and II to drive G_1 and G_2 respectively.

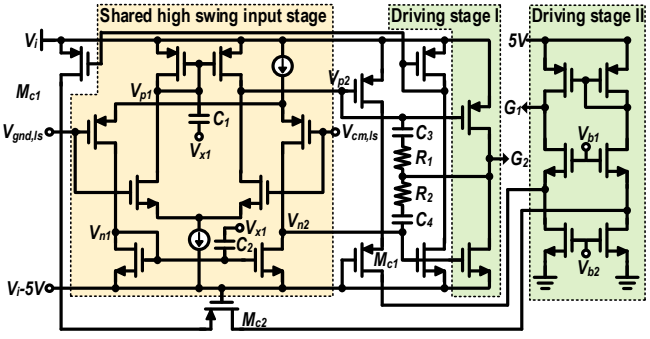
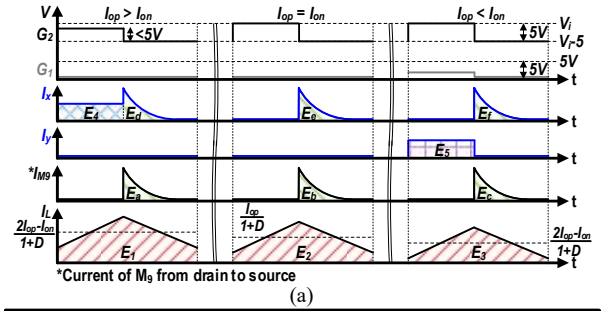
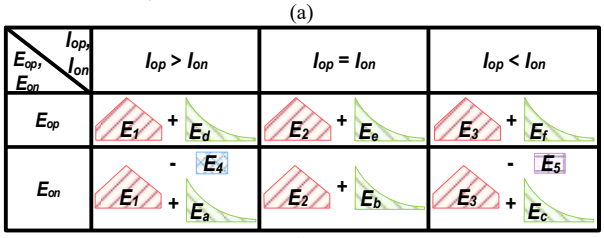


Fig. 5. Circuit implementation of analog controller.

With mismatch load, analog and digital controllers cooperate to lower V_{cm} ripple. The operation waveform and energy transferred to outputs are shown in Fig. 6(a) and (b). When I_{op} is larger than I_{on}, M_2 is turned on by the analog controller and M_1 is turned off in Φ_1. The energy delivered to V_{op} is equal to E_1+E_d while to V_{on} is equal to E_1-E_4+E_a since I_x is injected. When I_{op} is equal to I_{on}, digital controller dominates and turns off M_1 and M_2 in Φ_1. In this scenario, energy transferred to V_{op} and V_{on} are equal to E_2+E_e and E_2+E_b respectively. When I_{op} is smaller than I_{on}, E_{op} and E_{on} will be equal to E_3+E_f and E_3+E_5+E_c respectively due to I_y. In each condition, M_1 is turned off and M_2 is fully turned on in Φ_2.



(a)



(b)

Fig. 6. (a) A/D assisted operation and (b) energy transferred to outputs with A/D assisted compensator.

B. *Proposed gate-driven auto-calibration zero current detector (GDZCD)*

In light load condition, the inductor current may fall below 0. If the power path cannot be disconnected in time, the circuit will face reverse inductor current issue, resulting in worse light load efficiency and overshoot voltage on switching node V_{x1}, causing overstress on M_3. Conventional ZCD [5] calibrates the source-body voltage (V_{sb}) of mosfets. However, due to the parasitic BJT, V_{sb} will change when the converter is operated in CCM, and an additional time is required to calibrate back to the desired value when the converter changes from CCM operation to DCM operation.

To address these problems, this paper proposes the GDZCD which calibrates the gate voltage of M_2 (V_{cali}), as shown in Fig. 7. M_1-M_5 form the continuous comparator compares V_{on} and V_{x1}. With a higher value of V_{cali}, the comparator can operate faster. Pre-amplifier is composed of two sets of common-gate amplifier with interleaved inputs. The outputs of pre-amplifier (V_{pre1} and V_{pre2}) are sent to the clocked comparator and wait for comparison. The outputs of clocked comparator are preset to logically high. When ZCD signal is asserted, the power switch M_3 in ALB-SIBO converter is turned off and the one shot generator enables the clocked comparator for a predetermined time. If zero current is detected lately, UP will be asserted, the up/down (U/D) counter is enabled when EN = 1, and the 5-bit signal G[4:0] is incremented. In contrast, UP will be de-asserted and G[4:0] is decremented. By this operation, U/D counter only works when the ALB-SIBO converter operates in DCM mode. The voltage generator will generate 32 levels related to V_b, and V_{cali} will be determined by G[4:0]; the larger the value of G[4:0], the higher the voltage of V_{cali}. With gate voltage calibration, the ZCD signal can be triggered in time to avoid reverse inductor current.

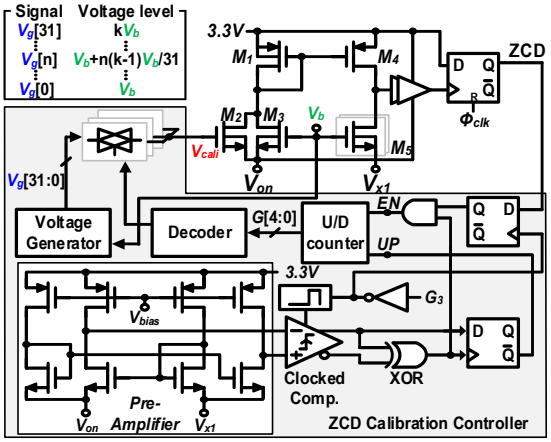


Fig. 7. Circuit implementation of gate-driven auto- calibration ZCD.

IV. Experimental Results

The proposed ALB-SIBO converter is fabricated in 0.15 µm CMOS process with silicon area of 1.7 mm*1.4 mm in Fig. 8. To test the functionality of A/D assisted compensator, the load of 1.8 A is applied at Von side with I_{mis} of 50mA added at V_{op} as shown in Fig. 9(a). If the A/D assisted compensator isn't activated, V_{op} will lack energy and deviate from 1.8 V with ΔV_{cm} of -22 mV. If the A/D assisted compensator is activated, the V_{op} is close to 1.8 V with ΔV_{cm} of -2.6 mV. Besides, the average inductor current ($I_{L,avg}$) is upshifted from 1.22 A to 1.27 A. When the loads of 1.8 A and 1.85 A are applied at V_{op} and V_{on} respectively as shown in Fig. 9(b), ΔV_{cm} is downshifted from 25mV to -3.3 mV while $I_{L,avg}$ is reduced from 1.24 A to 1.19 A due to the A/D assisted compensator.

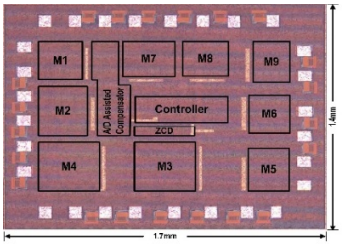
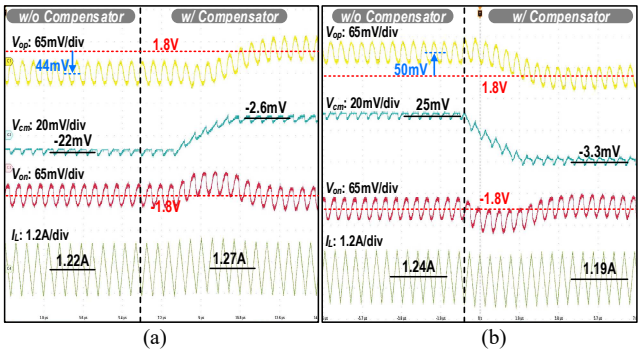


Fig. 8. Chip micrograph.

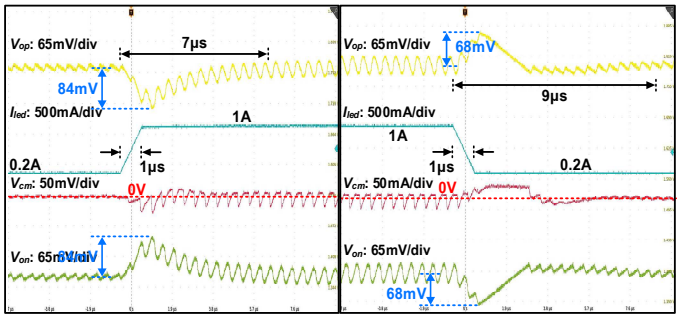


(a) (b)

Fig. 9. Measured outputs w/ and w/o A/D assisted compensator (a) when I_{op}>I_{on}(I_{op} = 1.85 A, I_{on} = 1.8 A) and (b) when I_{op}<I_{on} (I_{op} = 1.8 A, I_{on} = 1.85 A).

The heavy load transient with the load step of 800 mA/µs is shown in Fig. 10(a). The undershoot voltage of V_{op} and V_{on} is 84 mV with the recovery time of 7 µs compared to 82 mV and 60 µs with load step of 270 mA/µs in [4]. Although

the transient event occurs, ΔV_{cm} is still remained around 0V. Furthermore, the overshoot voltage of V_{op} and V_{on} is both 68 mV with the load step of -800mA/μs and the recovery time is 9 μs as shown in Fig. 10 (b).The output ripple of V_{op} and V_{on} at I_{led}=300 mA are 15 mV and 16 mV, respectively. $I_{L,avg}$ at DCM condition is equal to (D+D')*I_{led}/(2D+D'), where D is the duty cycle when I_L is in the rising slope and D' is the time when I_L is in the falling slope with respect to T_{clk}.



(a) (b)

Fig. 10. (a) Measured heavy load transient waveforms (I_{op} = I_{on} = I_{led}). (b) Measured light load transient waveforms (I_{op} = I_{on} = I_{led}).

The calibration of GDZCD is shown in Fig. 11, and the reverse current is low to sub-1 mA. The procedure starts by setting G[4:0]=0 and the reverse inductor current is -560 mA. The GDZCD Calibration Controller gradually up-counts until its value becomes 26. The controller stabilizes the 5-bit signal between 25 and 26 to minimize reverse current to sub-1 mA.

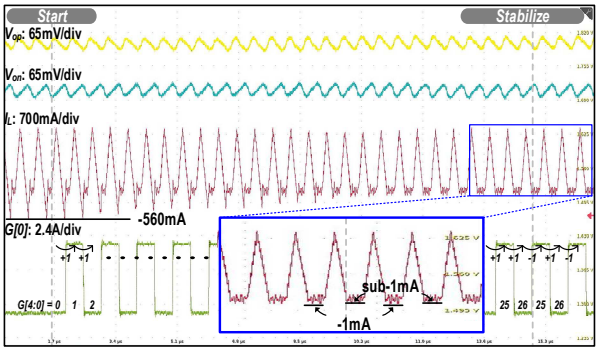
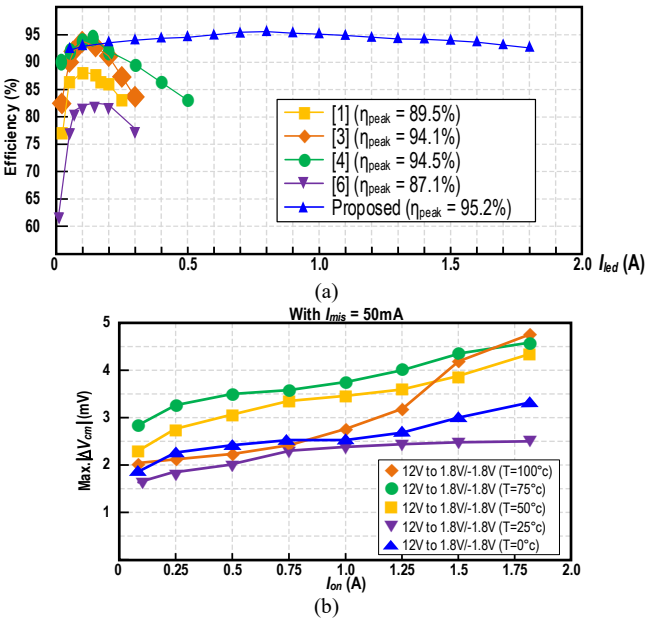


Fig. 11. Measured GDZCD calibration procedure when I_{op} = I_{on} = I_{led} = 500 mA.

The proposed ALB-SIBO converter achieves a peak efficiency of 95.2% at I_{led}=800mA, as shown in Fig. 12(a), representing a 0.7% improvement over [4] at I_{led}=120 mA. Fig. 12(b) presents the maximum $|\Delta V_{cm}|$ across varying temperatures with I_{mis} = 50 mA, where the worst-case value is 4.8 mV at 100 °C and I_{led}=1.8 A. Table I compares the proposed converter with prior works, highlighting its superior performance: the lowest $|\Delta V_{cm}|$ of 4.8 mV and highest efficiency of 95.2% at an output power of 6.48 W.

V. Conclusion

The proposed ALB-SIBO converter achieves 95.2% peak efficiency and 6.48W maximum output power. With the help of A/D Assisted Compensator, $|\Delta V_{cm}|$ is suppressed to 4.8 mV in the full range of I_{led} when encountering mismatch load between V_{op} and V_{on}. Thanks to the GDZCD, the reverse conduction current during DCM is suppressed to be sub-1 mA.



(a)

(b)

Fig. 12. (a) Measured efficiencies of prior arts and ALB-SIBO. (b) Measured maximum $|\Delta V_{cm}|$ of proposed ALB-SIBO.

Table I. Performance comparison with previously published works.

	This work	[1] STOD13A	[3] ISSCC2020	[4] ISSCC 2024	[6] VLSI 2010
CMOS Tech.	0.15μm	*N.A.	0.5μm	0.18μm	0.5μm
Topology	ALB	Multi-Inductor	SET	Hybrid	SIBBIF
Typical V_i [V]	12	3.7	3.7	3.7	3.7
V_{op}/V_{on} [V]	1.8/-1.8	4.6/-4.9	4.6/-4.9	4.6/-4.9	4.6/-5.4
Frequency [MHz]	2	1.5	1.4	1.5	1.25
Max. I_{led} [A]	1.8	0.25	0.3	0.5	0.3
Inductor	0.47μH	4.7μH*2	10μH	2.2μH	4.7μH
Flying Capacitor	1μF*2	*N.A.	*N.A.	4.7μF*2	4.7μF
Output Capacitor	4.7μF*2	10μF*2	10μF*2	10μF*2	10μF*2
Peak Efficiency	95.2%	**89.5%	94.1%	94.5%	87.1%
Area [mm²]	2.38	N.A.	1.46	1.19	5.75
Max. Output Power	6.48W	2.375W	2.85W	4.75W	3W
Max. $\|\Delta V_{cm}\|$	4.8mV	150mV	150mV	150mV	400mV
Output ripple on V_{op}/V_{on} @ I_{led}	15mV/16mV @ 300mA	**21mV/28mV @ 250mA	24.5mV/28mV @ 300mA	18mV/18mV @ 300mA	50mV/60mV @ 300mA
Undershoot / Recovery time @ load step	88mV / 7μs @ 800mA/μs	N.A.	***292mV / 37μs @ 270mA/20μs	***82mV / 60μs @ 270mA/μs	***150mV / 38μs @ 300mA/5μs
Overshoot / Recovery time @ load step	68mV / 10μs @ -800mA/μs	N.A.	***430mV / 60μs @ -270mA/20μs	***78mV / 80μs @ -270mA/μs	***100mV / 45μs @ -300mA/5μs

* Not reported in the paper** Obtained from Figure *** Estimated from the paper

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