# A +/-25 V Charge Pump With Switchable Polarity in 3.3 V CMOS Technology

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***Abstract*—In this paper a scalable multiple-stage charge pump with switchable polarity constructed from low-voltage MOS transistors is demonstrated. A distinguished feature of the proposed circuit is a cross-switch integrated in each pumping unit, which configures the polarity of the respective pumping stage depending on the polarity of the preceding stage, thus implementing a daisy-chained control scheme. Such approach allows connecting any amount of stages in series, enabling a straightforward scalability of the circuit.**

**A prototype switchable charge pump comprising 18 stages is implemented with 3.3 V MOSFET devices in 90 nm SOI-CMOS technology. The measured circuit generates output voltages exceeding +/–25 V from a single 1.9 V supply source while consuming a current of 450 $\mu$A. The proposed charge pump can be used as a driver for switchable systems requiring high actuating voltages for high-ohmic inputs.**

***Index Terms*—Bipolar, charge pump, high voltage, stacking, switch, voltage generation.**

## I. Introduction

Charge pumps are widely used in switchable systems requiring static bipolar actuation voltages for bringing and sustaining actuating elements in a desired state. Examples of the systems include non-volatile flash memory [1], MOSFET-based RF switches [2], MEMS ohmic and capacitive switches [3] etc. A typical configuration of such a system includes a positive and a negative charge pump circuit followed by level shifters that multiplex charge pump voltages into control nodes of the actuators [4] (for example, gates of MOSFETs in a RF switch) as depicted in Fig. 1(a).

Designing a high-voltage level shifter with low-voltage MOS devices is anything but a trivial task, as it is associated with a number of challenges (in this work "high voltage" is defined as a level that exceeds at least three times the maximum voltage rating of a single MOSFET device available in fabrication technology). A number of solutions for designing high-voltage level shifters, and particularly their output stages, are reported in literature [5], [6].

A circuit with three stacked MOSFETs presented in [5] targets pulsed mode of operation and cannot handle static signals. A design approach for scaling up the stack size to any arbitrary number of devices and operation with static voltages is proposed in [6], however it needs multiple reference voltage levels between the rails, requiring large voltage dividers. Many level-translating circuits reported in literature are based on high-voltage transistors available in the used technology [7],

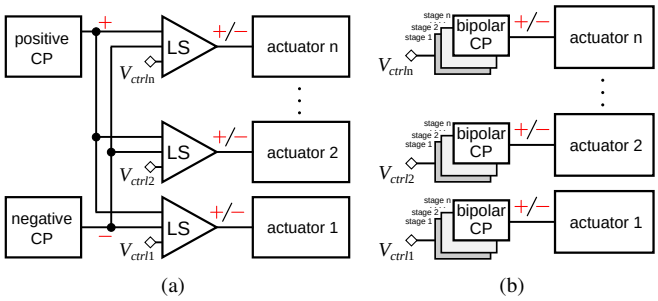


Fig. 1. (a) – Actuators controlled by bipolar voltages via level shifters (LS), (b) – Actuators controlled directly by individual charge pumps (CP) with switchable polarity.

however standard CMOS processes do not typically comprise such high-voltage devices. None of the above-mentioned structures offer an efficient solution if three or more stacked MOSFETs are needed to achieve the required voltage handling of the level shifter circuit. Moreover, the reported solutions cannot be scaled in a straightforward way.

In this work, we propose a concept and circuit implementation of a *scalable charge pump with switched polarity*, which can be directly coupled to the control terminal of an actuator, thus eliminating the need for a high-voltage level shifter as portrayed in Fig. 1(b). Switched-polarity charge pumps have been previously reported in literature [1], [8], [9]. However, in all cases switch based on single high-voltage MOSFET is used to swap the pumping branch polarity, requiring high-voltage transistors which are aimed to be avoided in this work.

## II. Charge Pump Implementation

A circuit diagram of the proposed charge pump is demonstrated in Fig. 2. It consists of $n$ switched-polarity voltage doublers $X_{pump1}$ through $X_{pumpn}$ coupled in series and driven by a differential rectangular signal generated by a ring oscillator $X_{ringo}$ followed by a driver circuit $X_{driver}$. The voltage doubler contains a charge transfer cell constructed from two cross-coupled transistor pairs $M_{n21}$–$M_{n22}$ and $M_{p21}$–$M_{p22}$ and capacitors $C_{21}$, $C_{22}$ [10]. When the square wave signal is applied to $f_p$ and $f_n$ the charge transfer cell generates a positive voltage between the nodes $v_p$ and $v_n$, wherein the potential at $v_p$ is always higher than at $v_n$.

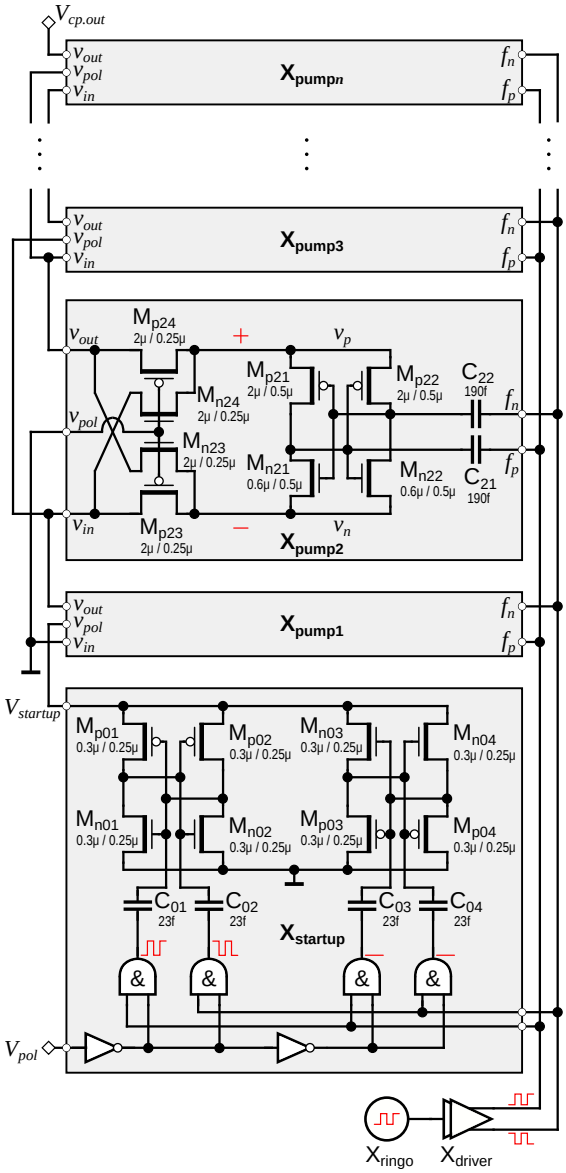


Fig. 2. Schematic diagram of the charge pump with switchable polarity.

The polarity of the output voltage $v_{out} - v_{in}$ from the doubler is configured by a cross-switch circuit made of $M_{n23}$, $M_{n24}$, $M_{p23}$, $M_{p24}$, which routs the nodes $v_p$ and $v_n$ to the respective terminals $v_{out}$ or $v_{in}$. The cross-switch is controlled by a single node $v_{pol}$. Normally-OFF transistors are utilized in the presented design. Therefore, in order to guarantee proper conduction of the cross-switch in any initial state of the charge pump a bipolar voltage is applied to $v_{pol}$ from the preceding stage $X_{pump}$.

When the circuit is configured to pump negative voltage, the $v_{pol}$ is forced to the level $v_p - v_n$ above the $v_{in}$, thus bringing the $M_{n23}$ and $M_{n24}$ to the ON state. The opposite occurs for the positive polarity of the circuit, meaning, the potential of node $v_{pol}$ is pulled to more negative than of node $v_{in}$, opening up the pair $M_{p23}$ and $M_{p24}$ and establishing the conductive path between the nodes $v_p - v_{out}$ and $v_n - v_{in}$. Since the

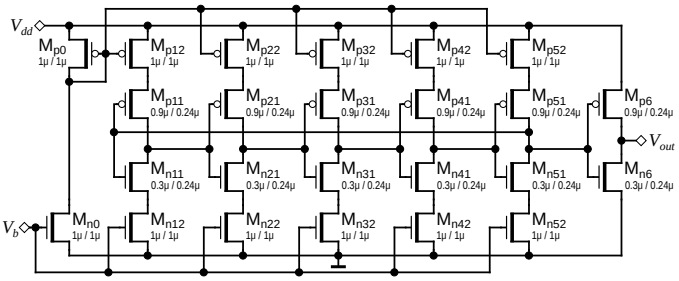


Fig. 3. Schematic diagram of the tunable current-starved ring oscillator $X_{ringo}$.

terminal $v_{in}$ of the first pumping stage is grounded and $v_{pol}$ node of the said stage needs to be biased by either positive or negative voltage, a start-up charge pump cell $X_{startup}$ is designed to trigger a chain reaction in the daisy chain and sequentially flip the pumping stages into the desired polarity. As shown in Fig. 2, the startup circuit block comprises two single-stage pumping units – the positive unit ($M_{n01}$, $M_{n02}$, $M_{p01}$, $M_{p02}$, $C_{01}$, $C_{02}$) and the negative unit ($M_{n03}$, $M_{n04}$, $M_{p03}$, $M_{p04}$, $C_{03}$, $C_{04}$), – either one being activated at a time depending on the digital polarity control signal $V_{pol}$, delivering either positive or negative voltage at $V_{startup}$.

The bodies of all NMOS and PMOS devices are connected to the lowest and highest potentials within the own cell, namely to the nodes $v_n$ and $v_p$ in the main pumping stages and to $V_{startup}$ and ground in the startup unit.

Note that the transistors in the cross switch are exposed to the DC voltage which is double the pumped voltage of a single charge pump stage. This implies that the voltage generated by a single plumping stage shall not exceed half of the maximum voltage rating of utilized MOSFET devices.

## III. Hardware Demonstrator

A prototype of the proposed charge pump has been designed and fabriacted in a 90 nm SOI-CMOS technology.

The charge pump core has been implemented in exact accordance to the schematic diagram in Fig. 2. The number of switched-polarity voltage doublers $X_{pump}$ is $n = 18$. Since the DC voltage at the last pumping stage $X_{pumpn}$ can theoretically reach the level of $\pm nV_{dd}$, where $V_{dd}$ is the magnitude of the driving rectangular signal at nodes $f_n$ and $f_p$, the capacitors $C_{21}$ and $C_{22}$ are implemented as metal-oxide-metal (MOM) structures in the BEOL stack, capable of handling DC voltages above 40 V. Due to the relatively low specific capacitance of these structures, they occupy most of the layout area of the pumping stage (approximately 95 %).

A single MOSFET in the technology is rated for the maximum voltage of 3.3 V. Since the transistors $M_{n23}$, $M_{n24}$, $M_{p23}$, $M_{p24}$ of the cross-switch are exposed to double the pumped voltage of a single stage, the output voltage of the doubler shall not exceed $0.5 \cdot 3.3$ V, namely:

$$|v_{out} - v_{in}| = v_p - v_n < 1.65\,\mathrm{V} \tag{1}$$

This requirement is addressed by limiting the supply voltage $V_{dd}$ of the CMOS inverter-based driver, which outputs the

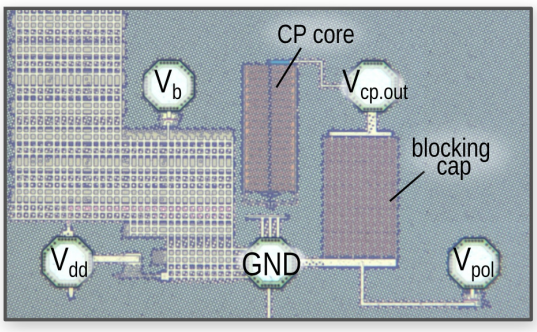


Fig. 4. Photograph of the fabricated IC ($900\times500\,\mu m^2$).

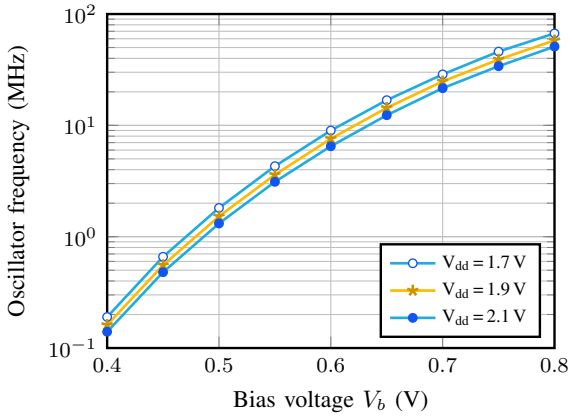


Fig. 5. Ring oscillator frequency as a function of bias and supply voltages at room temperature.

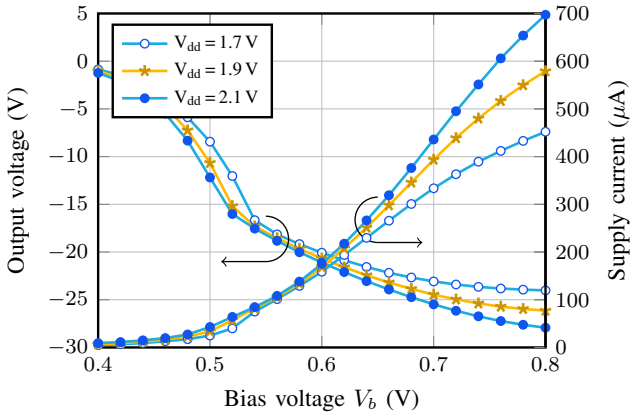


Fig. 6. Measured output voltage and supply current of the unloaded charge pump configured to generate negative output ($V_{pol} = 0$ V).

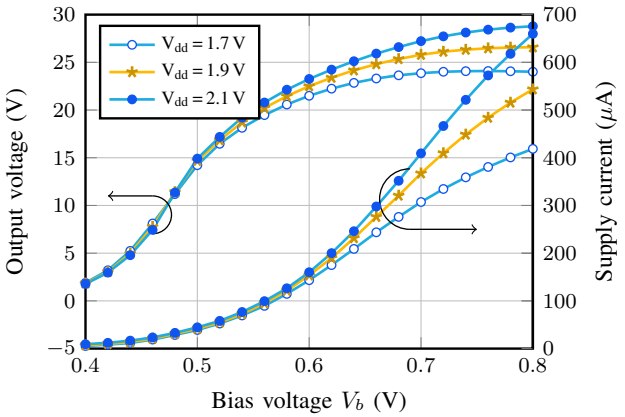


Fig. 7. Measured output voltage and supply current of the unloaded charge pump configured to generate positive output ($V_{pol} = V_{dd}$).

rectangular pulses with the peak voltage of $V_{dd}$. While the theoretical limit for $V_{dd}$ could be 1.65 V, practically, due to charge sharing in the internal nodes of the pumping stages the maximum supply voltage was set to 2.1 V, which according to simulation, allowed to fulfill the requirement set by (1).

A current-starved ring oscillator [11] with the wide frequency tuning range between 0.1 MHz and 100 MHz is used to generate the drive signal for the charge pump. The schematic diagram is demonstrated in Fig. 3.

## IV. Measurement Results

A photograph of the fabricated die is demonstrated in Fig. 4. The largest portion of the charge pump core is occupied by the MOM capacitors. Yet another 9.5 pF MOM capacitor is connected between the output node $V_{cp.out}$ and ground to suppress the ripple and switching noise of the circuit.

The measured oscillator frequency response for various bias and supply voltages is shown in Fig. 5. With the help of these curves the values of bias voltage $V_b$ and supply voltage $V_{dd}$ in the measured characteristics can be traced back to the drive signal frequency.

The measured negative output voltage of the unloaded charge pump (open-circuited output) is presented in Fig. 6, reaching the level of –28 V at the peak bias conditions. The positive voltage response of the circuit demonstrates similar behavior and is shown in Fig. 7.

The short-circuited output currents in both positive and negative states of the charge pump are plotted in Fig. 8. A notable difference in the driving strength capabilities between the positive and negative outputs is explained by the influence of handle silicon wafer (acting as a back-gate) on the conductivity of MOSFET channel – indeed, at high positive pumped voltages ($V_b$ of 0.55 V and above, corresponding to $V_{cp.out} > 20$ V) the body to back-gate voltage substantially shifts up the threshold voltage of the transistors in the $X_{pump}$ cells, visibly limiting the charge-pump output current.

Table I provides a comparison of the presented high-stacked switchable charge pump with state-of-art switchable bipolar charge-pumps of the similar class. The circuit reported in this work demonstrates compatible power dissipation with notably higher number of pumping stages constructed solely with low-voltage MOSFETs, differentiating itself from the other concepts, specifically [1] and [9].

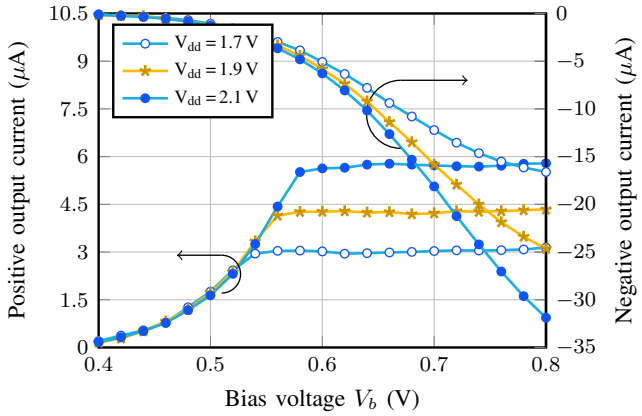


Fig. 8. Measured short-circuited output current of the charge pump.

TABLE I
COMPARISON TABLE OF SWITCHED POLARITY CHARGE PUMPS

| **Parameter** | **This work** | **[9]** | **[1]** | **[12]** |
|---|---|---|---|---|
| CMOS node (nm) | 90 | 180 | 130 | 250 |
| Supply voltage (V) | 1.9 | 1.8 | 1.5 | 2.5 |
| Number of pumping stages | 18 | 7 | 5 | 6 |
| Output voltage (V) | ±25 | ±11 | ±9 | ±12* |
| Power dissipation in unloaded conditions (mW) | 0.85 | 2.1–2.3 | n.a. | 2.4–3.9 |

* – separate positive and negative outputs, not switchable.

## V. CONCLUSION

In this work a high-voltage, switchable polarity charge-pump designed with low-voltage transistors is presented. Among the main benefits of the proposed concept is an ease of circuit scalability in terms of stacking of the charge pump stages, which is enabled by the daisy-chained control mechanism between the pumping units. Among the limiting factors for the number of stacked pumping stages are influence of the handle wafer on the channel conductance of the MOSFETs (back-gate biasing effect) in stack and the breakdown voltage ratings for the pumping capacitors.

The hardware prototype designed in 90 nm SOI CMOS process comprising 18 stacked pumping stages generating ±25 V from a 1.9 V supply prove the proposed concept. The presented charge pump can find a use as a driver for transducers requiring high-voltage, low-power actuating signals.

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