

A 0.65-pJ/b, 11-Gb/s/pin Transmitter Employing Edge-Controlled Crosstalk Cancellation For Near-Complete Suppression of Crosstalk-Induced Jitter

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Abstract—This paper presents an 11-Gb/s/pin, 5-channel transmitter (TX) incorporating an edge-controlled crosstalk cancellation (EC-XTC) scheme that achieves nearly 100% reduction in crosstalk-induced jitter (CIJ). In the proposed EC-XTC architecture, an edge controller boosts the initial transition slope of the channel output by modulating the voltage level of a 1-UI pulse, which subsequently controls a feedforward XTC driver. CIJ is effectively minimized through the joint optimization of the XTC driver strength and the boosting level of the edge controller. Fabricated using a 28-nm CMOS process, the prototype TX maintains a horizontal eye opening of 0.506 UI at the center victim channel output at a bit error rate (BER) of 10^{-9} , both in the absence and presence of adjacent aggressor channels, demonstrating a CIJ reduction ratio approaching 100%. The TX core, including the five channel drivers and EC-XTC circuitry, achieves an energy efficiency of 0.65 pJ/b at 11 Gb/s/pin.

Keywords—Crosstalk (XT), crosstalk-induced jitter (CIJ), high-density interconnects, transmitter (TX).

I. INTRODUCTION

Advances in recent packaging technologies, such as 2.5D heterogeneous integration and 3D integrated circuits, have enabled high-throughput communication between processors and high-bandwidth memory (HBM) [1]. To meet the data bandwidth demands of the next-generation HPC/AI era, interconnect channels should become denser, and the data rate must be increased. However, this trend results in severe crosstalk (XT) noise issues, as multi-channel signals transition at higher frequencies and increasingly couple with one another. To address this, transmitters (TXs) with FIR-based crosstalk cancellation (XTC) schemes [2], [3], as well as the TX with a feedforward equalizer (FFE)-combined XTC scheme [4], have been proposed. These prior XTC schemes employed feedforward XTC drivers and utilized aggressor data information to cancel far-end crosstalk (FEXT), as shown in Fig. 1(a). However, the achieved crosstalk-induced jitter (CIJ) reduction was limited to 70–80%.

In this work, a 5-channel TX employing an edge-controlled XTC (EC-XTC) scheme is proposed. To further suppress CIJ, an edge controller enhances the initial transition slope of the victim channel output, effectively eliminating CIJ caused by FEXT through the XTC driver control. By jointly optimizing the boosted pulse level generated by the edge controller and the strength of the XTC driver, the horizontal eye margin is closely restored to its original value observed in the absence of FEXT.

II. PROPOSED CROSSTALK CANCELLATION SCHEME

A. Overall TX Architecture

Fig. 2 shows the overall TX architecture employing the proposed EC-XTC scheme, which includes 5-channel TX,

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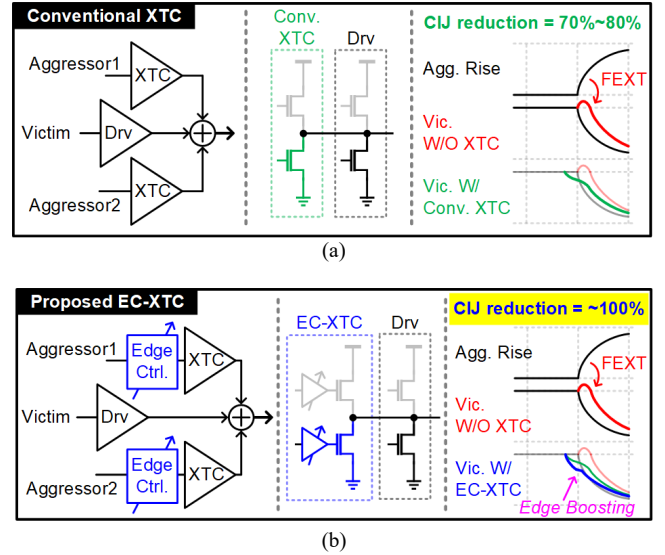


Fig. 1. (a) Conventional XTC scheme and (b) proposed EC-XTC scheme.

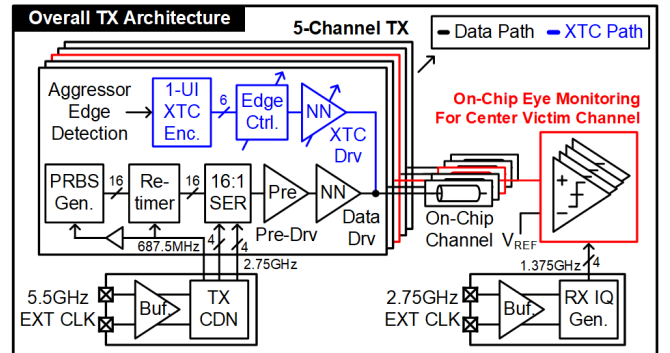
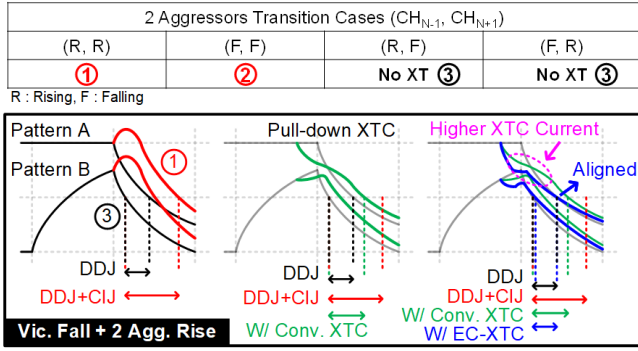
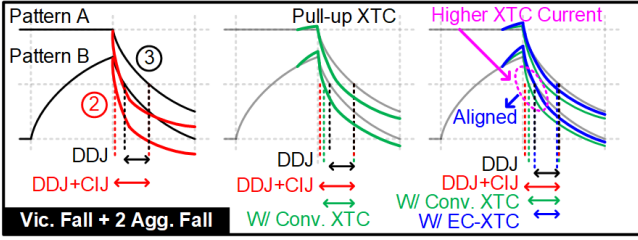


Fig. 2. Overall TX architecture with proposed EC-XTC scheme.

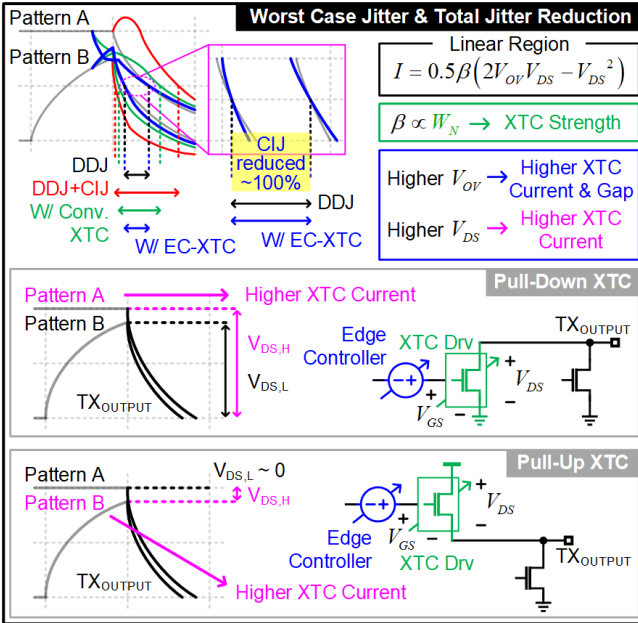
on-chip channels, and a single-channel receiver (RX) for on-chip eye monitoring of the center victim channel output. Each TX consists of a data path with an XTC path and a clock path that generates quadrature clock signals. On the data path, a 16-bit parallel PRBS data pattern is generated and retimed before 16:1 serialization. After serialization, the pre-driver boosts the edge level of the data to drive the N-over-N (NN) main driver. Transition-detected 1-UI pulses are generated for the pre-driver to boost the edge level. Finally, the main driver transmits the data to the on-chip channel. On the XTC path, a 1-UI XTC encoder generates pulse signals to activate the edge controller and XTC driver, using transition-detected 1-UI pulses from the two adjacent aggressors. The edge controller adjusts the boosting level of pre-driven XTC pulse, while the XTC driver controls the pull-up/down strength of the XTC pulse, which will be described in detail in the following section.



(a)



(b)



(c)

Fig. 3. Operation principle of the proposed EC-XTC scheme: CIJ reduction of conventional XTC and EC-XTC with falling victim case when (a) aggressors are rising and (b) falling. (c) Total jitter generation and reduction by EC-XTC scheme.

B. Operation of Edge-Controlled Crosstalk Cancellation

Fig. 3 illustrates the operation principle of the proposed EC-XTC scheme with an analysis of the worst-case jitter generation. The worst data-dependent jitter (DDJ) occurs between these transitions: a long sequence of ones ending with a falling edge (11...110), called *Pattern A*, and a long sequence of zeros with a single ‘1’ in the middle (00...010), called *Pattern B*. With these two patterns, the worst-case jitter is generated when the adjacent aggressors rise for *Pattern A* and fall for *Pattern B*. Similarly, the other worst-case jitter is generated when the adjacent aggressors fall and rise with the victim channel’s data patterns of (00...001) and (11...101), respectively.

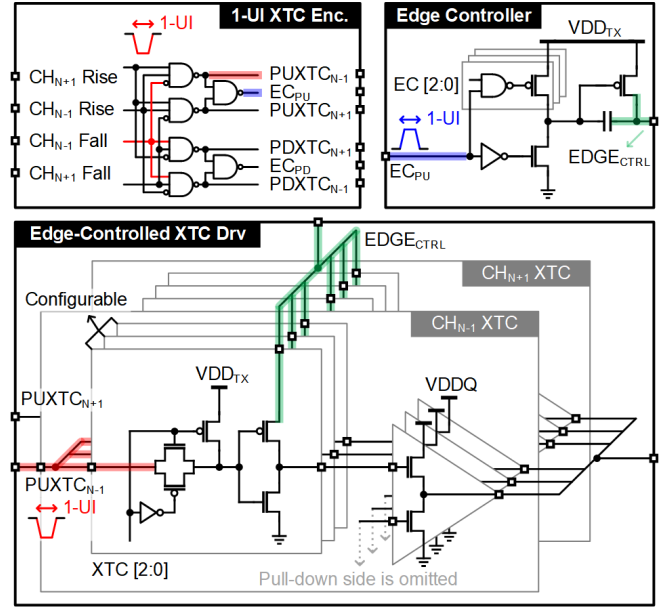


Fig. 4. Schematic of proposed EC-XTC circuitry.

Fig. 3(a) shows the CIJ reduction of conventional XTC and the proposed EC-XTC against the worst jitter when the victim falls with two aggressors rising. Here, the worst jitter is generated by the DDJ of *Pattern B* and the CIJ added to *Pattern A*. Conventional XTC can only partially reduce the CIJ added to *Pattern A*, so some jitter remains. In contrast, the proposed EC-XTC boosts the initial slope of the pull-down XTC more for *Pattern A* than for *Pattern B*, allowing nearly complete CIJ cancellation and leaving only the DDJ. Fig. 3(b) shows a similar case but with two falling aggressors. In this case, the DDJ of *Pattern A* and the CIJ given to *Pattern B* contribute to the worst jitter. Again, conventional XTC offers limited CIJ reduction for *Pattern B*. However, the proposed EC-XTC improves the pull-up transition of *Pattern B* more effectively than for *Pattern A*, owing to its ability to adapt based on the varying V_{DS} of the XTC driver, which carries information about signal transition.

Fig. 3(c) provides a full comparison between conventional XTC and EC-XTC in terms of total CIJ generation. The peak-to-peak CIJ is mainly caused by *Pattern A* with rising aggressors and *Pattern B* with falling aggressors. Conventional XTC fails to cancel this jitter completely because the compensated falling edge of the victim signal is not sharp enough. The proposed EC-XTC, however, sharpens this edge, allowing it to cross the two patterns with no XT at the RX decision threshold (V_{REF}), achieving close to 100% CIJ reduction. For instance, as seen in Fig. 3(a), when aggressors are rising while the victim is falling, a pull-down XTC is needed. For *Pattern A*, the pull-down XTC driver operates with a full V_{DS} of V_{DDQ} , generating a strong current. For *Pattern B*, the V_{DS} is lower, leading to a weaker current. Since the XTC driver works in the linear region, a higher V_{DS} produces a higher XTC current. Additionally, a higher overdrive voltage (V_{OV}) increases both the current and the difference between high and low V_{DS} cases. This XTC strength can be linearly tuned by adjusting the width of the XTC driver. A similar analysis applies to the case in Fig. 3(b) and to other scenarios, such as rising victim with falling or rising aggressors, leading to the same conclusion as in Fig. 3(a).

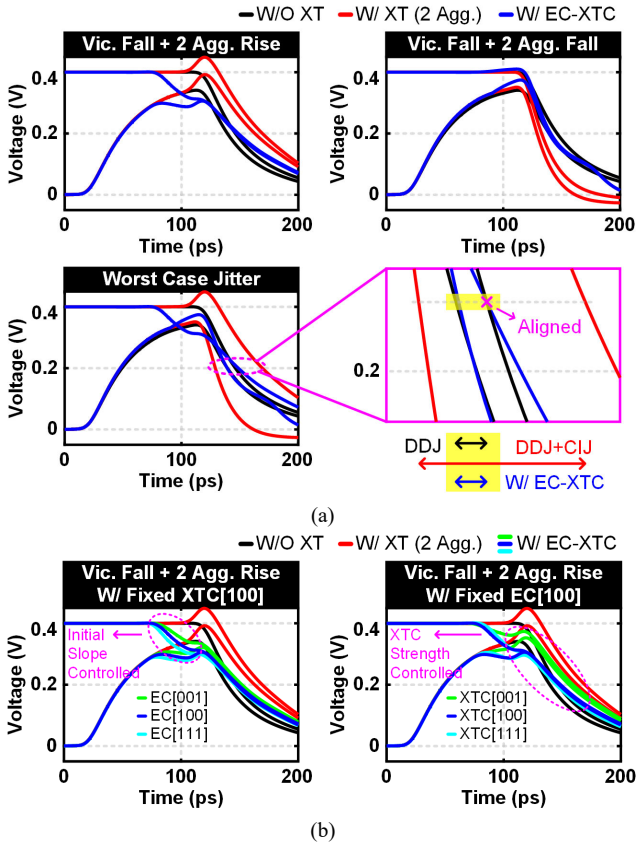


Fig. 5. Post-layout simulated waveforms of an on-chip victim channel output at 11 Gb/s per pin: (a) Worst jitter case of falling victim with rising aggressors, falling aggressors, and total jitter reduction when the optimal EC-XTC is enabled. (b) Effect of the pulse boosting modulation and an intrinsic XTC strength control.

C. Implementation of Edge-Controlled Crosstalk Cancellation

Fig. 4 shows the schematic of the proposed EC-XTC circuitry. For simplicity, only the pull-up section of the edge controller and XTC drivers is shown. The 1-UI XTC encoder is made up of four 3-input NAND gates (each with input inverters) and two 2-input NAND gates. The encoder outputs on the pull-up side— $PUXTC_{N-1}$ and $PUXTC_{N+1}$ —activate the pull-up XTC drivers for CH_{N-1} and CH_{N+1} , which cancel the FEXT induced by those adjacent channels. Similarly, $PDXTC_{N-1}$ and $PDXTC_{N+1}$ activate the pull-down XTC drivers. Two additional output signals, EC_{PU} and EC_{PD} , serve as base pulses for pulse boosting in the pull-up and pull-down edge controllers, respectively.

The edge controller (EC) circuit boosts the input pulse using capacitive peaking with a pre-charged series capacitor. It includes a 3-bit configurable PMOS for pulse boosting, a series capacitor, and a PMOS/NMOS pair for charging. When the input pulse is low, the PMOS/NMOS pair charges the capacitor. When the input pulse goes high, the PMOS/NMOS pair turns off, and the boosting PMOS releases the charge from the capacitor to create a stronger output pulse. The boost level can be set between 1.1 V to 1.4 V.

Each edge-controlled XTC driver has two parts to cancel the FEXT from CH_{N-1} and CH_{N+1} . The XTC driver includes three segments: an XTC strength control switch, an inverter for the edge-boosted pulse, and a NN main driver. The strength control uses a 3-bit switch to choose how many NN drivers are active, adjusting the overall XTC strength. The inverter passes the edge-boosted pulse when $PUXTC_{N+1}$ or

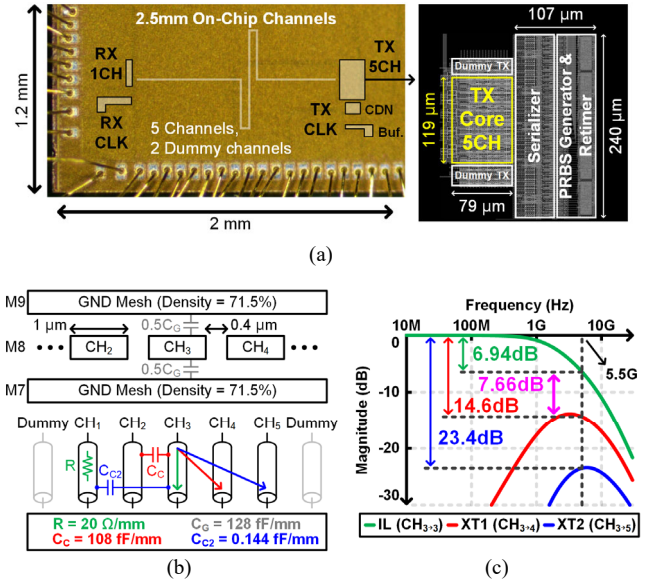


Fig. 6. (a) Prototype chip microphotograph. (b) Structure and (c) post-layout-simulated frequency response of on-chip channels.

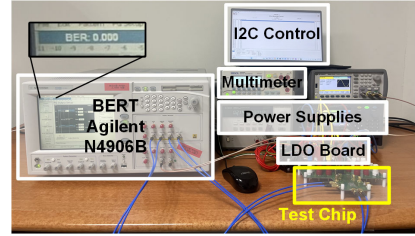


Fig. 7. Measurement setup.

$PUXTC_{N-1}$ is low. Finally, the main driver sends this pulse to cancel out the FEXT, enabling the edge-controlled XTC.

Fig. 5 shows the post-layout simulation results for the on-chip victim channel output at 11 Gb/s per pin. In Fig. 5(a), enabling the optimized EC-XTC fully eliminates the worst-case jitter. Fig. 5(b) highlights how both pulse boosting and intrinsic strength control contribute to XTC behavior. The EC circuit shapes the initial transition slope, while the XTC driver tunes the XTC strength.

III. MEASUREMENT RESULTS

Fig. 6(a) shows the microphotograph of the prototype chip, fabricated using a 28 nm CMOS process. It includes a 5-channel TX implementing the proposed EC-XTC scheme, 2.5-mm on-chip channels, and a single-channel RX for on-chip eye monitoring of the center victim channel output. The total active area of the TX is 0.045 mm^2 , with the TX core circuit occupying an active area of $0.0019 \text{ mm}^2/\text{pin}$. Fig. 6(b) illustrates the on-chip channel structure, including the equivalent resistance and capacitance per unit length. The channels are constructed using M7 and M9 metals as ground meshes (71.5% area density) and M8 as the signal lines. The signal line width and spacing are $1 \mu\text{m}$ and $0.4 \mu\text{m}$, respectively. Fig. 6(c) presents the post-layout simulated frequency response of the on-chip channels. At the Nyquist

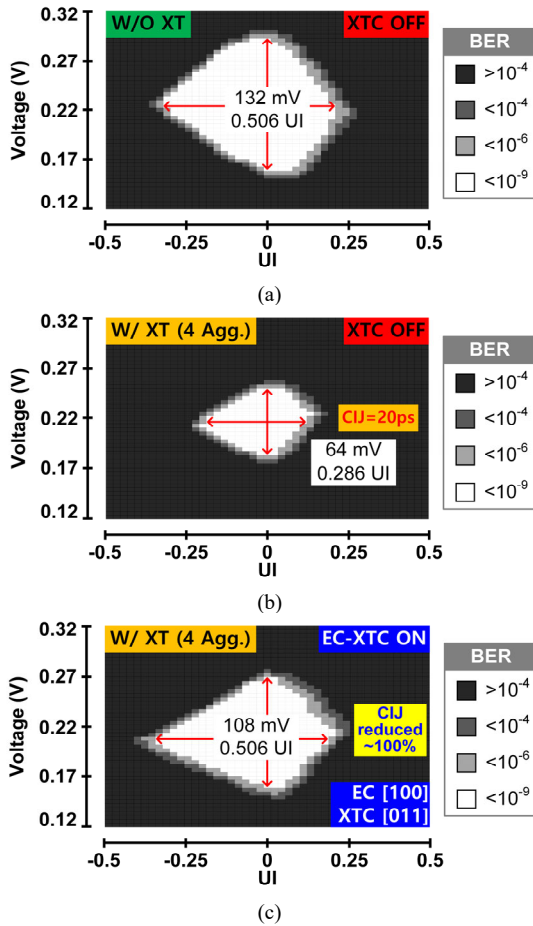


Fig. 8. Measured shmoo plot: (a) No XT, (b) EC-XTC off with four aggressors, and (c) EC-XTC enabled with four aggressors.

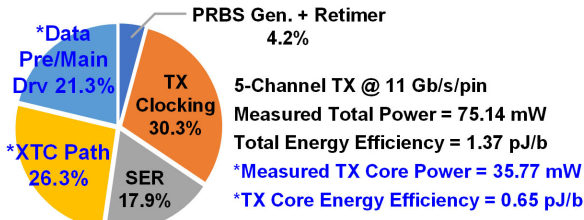


Fig. 9. Measured power consumption with power breakdown.

frequency of 5.5 GHz, the channel loss is 6.94 dB, the first-adjacent FEXT (XT1) is -14.6 dB, and the second-adjacent FEXT (XT2) is -23.4 dB. Given that the signal-to-crosstalk ratio (SCR) for XT1 is 7.66 dB and for XT2 is 16.46 dB, XT1 is identified as the dominant FEXT source, while XT2 is negligible. Fig. 7 shows the measurement setup for the prototype chip operating at 11 Gb/s per pin, using on-chip generated PRBS-7 data.

Fig. 8 shows the measured shmoo plots of the center victim channel output, obtained by sweeping the RX sampling timing and reference voltage (V_{REF}), using a bit error rate (BER) criterion of 10^{-9} . In the absence of aggressors, the horizontal and vertical eye openings are 0.506 UI and 132 mV, respectively, as shown in Fig. 8(a). When all five channels are driven by each TX driver with PRBS-7 data using different seeds, the eye degrades to 0.286 UI and 64 mV, respectively, as shown in Fig. 8(b). With the proposed EC-XTC enabled, the horizontal eye opening is fully recovered to 0.506 UI, demonstrating nearly 100% CIJ reduction, as shown in Fig. 8(c). Fig. 9 shows the power breakdown. The 5-channel TX driver with the EC-XTC

TABLE I.
COMPARISON OF XTC SCHEMES FOR HIGH-DENSITY ON-CHIP CHANNELS

| | ISSCC 2020 [4] | JSSC 2024 [5] | SOVC 2024 [6] | This Work |
|--------------------------------|---|--------------------------------------|-----------------------|--------------------------|
| Technology | 65nm | 28nm | 40nm | 28nm |
| Signaling Type | NRZ (Voltage Mode) | PAM-4 (Capacitive) | NRZ (Current Mode) | NRZ (Voltage Mode) |
| Supply Voltage | 1.2V (TX) | 1.0V (TRX) | 1.0V / 1.2V (TX / RX) | 0.4V / 1.0V (VDDQ / VDD) |
| Data Rate [Gb/s/pin] | 4 | 24 | 20 | 11 |
| XTC Type | FFE-combined XTC | PAM-based XTC | TIA-based XTC | Edge-controlled XTC |
| Channel Length | 6mm | 4mm | 1mm | 2.5mm |
| Channel Pitch | 1 μ m (0.5 μ m) (3-D Staggered) | 2 μ m | 1.5 μ m | 1.4 μ m |
| Channel Width | 0.5 μ m | 1 μ m | 0.5 μ m | 1 μ m |
| Channel loss | 10.2dB | 4.3dB (7.5dB) (W/ Capacitor) | N/A | 6.94dB |
| Signal-to-Crosstalk Ratio | 6.2dB | 13.4dB (10.2dB) (W/ Capacitor) | N/A | 7.66dB |
| CIJ Reduction Ratio | 78% | 64% / 76% / 62% (top / mid / bottom) | 75% (Simulated) | Close to 100% |
| Horizontal Eye [UI] (BER) | 0.4 (< 10^{-9}) | 0.37 / 0.48 / 0.34 (< 10^{-12}) | 0.56 (< 10^{-10}) | 0.506 (< 10^{-9}) |
| Vertical Eye [mV] (BER) | 26 (< 10^{-9}) | 60 / 80 / 60 (< 10^{-12}) | 38 (< 10^{-10}) | 108 (< 10^{-9}) |
| Energy Efficiency [pJ/b] | 1.5 | 0.458 | 0.246 | 1.37 |
| Core Energy Efficiency* [pJ/b] | 1.5 | 0.458 | 0.199 | 0.65 |

* Energy efficiency of only data driver and XTC path.

circuitry consumes 35.77 mW, achieving an energy efficiency of 0.65 pJ/b. Table I compares the performance of this work with prior XTC schemes for high-density on-chip channels [4]–[6], showing that the proposed design achieves the best CIJ reduction with competitive core energy efficiency.

IV. CONCLUSION

This work presents a 5-channel TX operating at 11 Gb/s/pin, featuring a novel EC-XTC scheme for high-density interconnects. The proposed EC-XTC effectively reduces CIJ by nearly 100% through precise control of the XTC driver and the boosted pulse level of the edge controller. These controls modulate both the initial and overall slopes of the victim channel output, significantly improving signal integrity. Measurement results demonstrate full recovery of the horizontal eye margin under worst-case crosstalk conditions, and the prototype achieves a core energy efficiency of 0.65 pJ/b, outperforming prior XTC solutions in CIJ mitigation.

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