A 1.8 GHz 50 µW frequency-locked LO-generator for OOK receivers in 22 nm FDSOI CMOS

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***Abstract*—A low-power ring oscillator based digital frequency locked loop in 22 nm FDSOI CMOS technology is presented. Operating at 1.84 GHz with a 40 MHz reference frequency it consumes in total 50 µW from 0.55 V and 0.8 V supplies. The circuit supports fractional-N operation with a phase noise below −82 dBc/Hz at 10 MHz offset, without visible fractional spurs, and reference spurs below −35 dBc, and it is verified in temperatures up to 80 °C. The intended application is LO generation in OOK wake-up receivers.**

***Index Terms*—CMOS, FDSOI, frequency locked loop, IoT devices, on-off keying, ultra-low power, wake-up receiver**

I. Introduction

In many IoT applications the devices must have an extremely low power consumption, relying on a small battery to supply power for many years, or on energy harvesting with low available power. To minimize power consumption, a device can be in a sleep state consuming close to zero power most of the time, and a wake-up receiver can be used for remote activation. The wake-up receiver, however, must be active at least part of the time during sleep state, and it is therefore required to have ultra-low power consumption. Typically, wake-up signals with on-off keying (OOK) modulation are used, which being a pure amplitude modulation does not require local oscillator (LO) signals with high phase stability for correct reception. To generate such a stable LO-signal would require a phase locked loop (PLL), which is incompatible with the stringent power budget of the wake-up receiver. Using OOK modulation, the signal can be demodulated by a rectifier which is largely insensitive to signal frequency and phase. The demodulation can take place at radio frequency (RF), or at an intermediate frequency (IF). Attractive receiver sensitivity and power consumption can be achieved by frequency down-converting the received RF signal to an uncertain IF (U-IF) before demodulation [1] [2]. Without the frequency locking in the part labeled "This Work", the wake-up receiver in Fig. 1 would have an U-IF architecture.

A drawback, however, is the limited selectivity of such a receiver, since the IF filters must be wide enough to pass all IF signals within the expected frequency range, including IF uncertainty, and as little as 1% uncertainty in a 2 GHz oscillator frequency corresponds to 20 MHz IF uncertainty. In [3] a PLL is used for frequency calibration of an LC-oscillator to reduce the uncertainty. After calibration the LC oscillator is free running with good frequency stability in constant temperature. A ring oscillator (RO) has advantages over an LC-

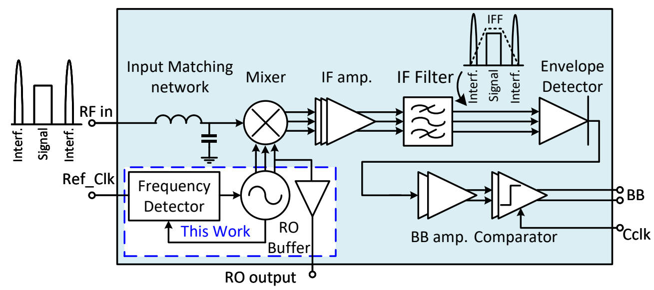


Fig. 1: Wake-up receiver using the proposed frequency locked LO generator.

oscillator in ultra-low power operation, small chip area, and wide relative tuning range, but it is much less frequency stable and hence less suitable for the technique in [3]. In this work we therefore provide an ultra-low power frequency locking of an RO, confining it to a narrow range of a few MHz by operating in closed loop. An IF filter with a narrower bandwidth can then be used to drastically improve the wake-up receiver selectivity, see Fig. 1. Since OOK modulation is used a rather relaxed frequency locked loop (FLL) can be used to stabilize the RO frequency, with a coarse digital phase detection to save power, relying on averaging to obtain sufficient frequency resolution for the frequency control. The implementation of the ultra-low power all-digital FLL is the focus of this work, and the following sections present the design and measurements of a 1.8 GHz FLL based LO generator implemented in 22 nm FD-SOI technology consuming below 50 µW.

II. Circuit design

Fig. 2 shows the block schematic of the frequency locked loop (FLL) circuit. It is designed in a 22 nm FD-SOI process, and to take advantage of that the FLL is largely digital. A three-stage RO is used, where the frequency is digitally controlled by the bias current. The bias current is provided by a digital to analog converter (DAC) using current source cells, with a digitally controlled PMOS switch transistor on top of a PMOS current source transistor, arranged in different tuning banks (sub-DACs). The three RO output signals are sampled at the reference clock rate of 40 MHz, and RF signals are also provided driving a passive mixer to ensure relevant driving capabilities and reported power consumption for the circuit. The sampling uses a CMOS transmission gate and a capacitor, followed by a D-flip-flop taking the binary decision

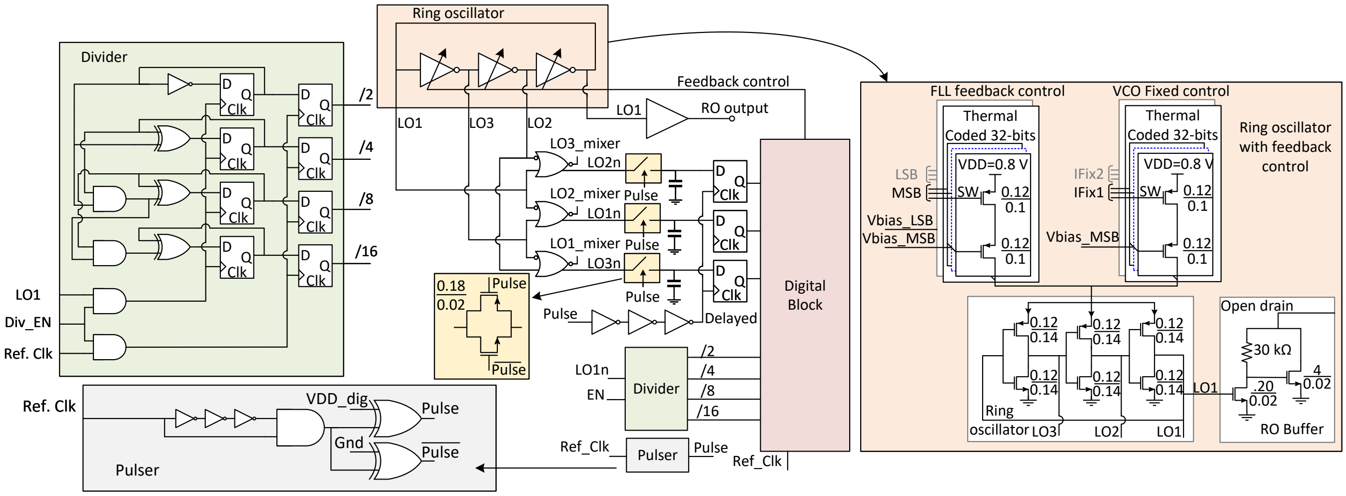


Fig. 2: Schematics of proposed fractional-N digital FLL.

and providing the result to the digital block. Sampling the three-stage RO provides a 3-bit word, which at different phases over an oscillation cycle takes on 6 different values, which we number in order from 1 to 6. In the digital block we then take the difference between the numbers of consecutive samples. The differences provide a measure of the current fractional frequency of the RO, that can be used in the FLL control loop. For instance, if the difference between current and previous sample is equal to 1, the phase has advanced by N+1/6 periods in one reference cycle, and the RO frequency is then equal to an integer multiple (N) of the reference frequency plus 1/6 of the reference frequency, i.e. the fractional frequency is estimated to 1/6. Wrap around needs to be handled, so that when the state advances by one from sample to sample, and then goes from 6 to 1 we do not get a large negative spike of -5. We then add 6 to large negative values in that case, turning the -5 into a 1. As a frequency resolution of 6.7 MHz (reference frequency of 40 MHz divided by 6) is too coarse, we perform averaging of the result before using it to adjust the RO frequency. Averaging 120 consecutive sample-differences improves the resolution 120x, to 56 kHz, which takes 3 µs of averaging to obtain, so the RO update rate can still exceed 300 kHz. To avoid locking to a wrong reference frequency harmonic, a counter clocked by the RO is also part of the circuit. When active, it counts from 0 to 15 over again without stopping, and its output is sampled by 4 flip-flops clocked by the reference frequency. Taking sample differences (but now counter state samples) and averaging the result, can be used to estimate the RO frequency. The unambiguous frequency range of the frequency estimate becomes 16x the reference frequency, i.e. 640 MHz, which is wide enough to avoid false lock. The counter can be selectively activated, using the serial to parallel interface (SPI) that provides all control of the circuit, so it is only active during initial locking and then turned off not to consume power. The RO can then be controlled to a frequency near the desired using the coarser frequency estimates from the counter, after which the higher resolution FLL based on RO sampling can be started. This part could be further automated using a state-machine in the digital part. Relevant to the reported FLL circuit steady-state performance is that such a divider circuit is present in the circuit and that its loading effect is thus included. In the test circuit the RO was tuned manually using the frequency control input IFix1 to set it to a frequency nearby the target before activating the FLL. A 2-stage open drain measurement buffer is also connected to the oscillator, but as buffers driving a mixer are already included in the circuit and in the reported power consumption, and these are the buffers that would be used when integrated with a wakeup receiver, the measurement buffer power consumption is excluded.

III. Measurements

The proposed fractional-N digital FLL is part of a larger chip fabricated in 22 nm FD-SOI technology, where all FLL parts are confined to a chip area of 290 µm x 200 µm, see Fig. 3. The RO takes 15 µm x 45 µm, the digital part takes 80 µm x

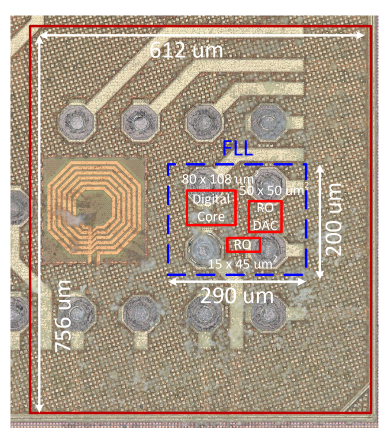
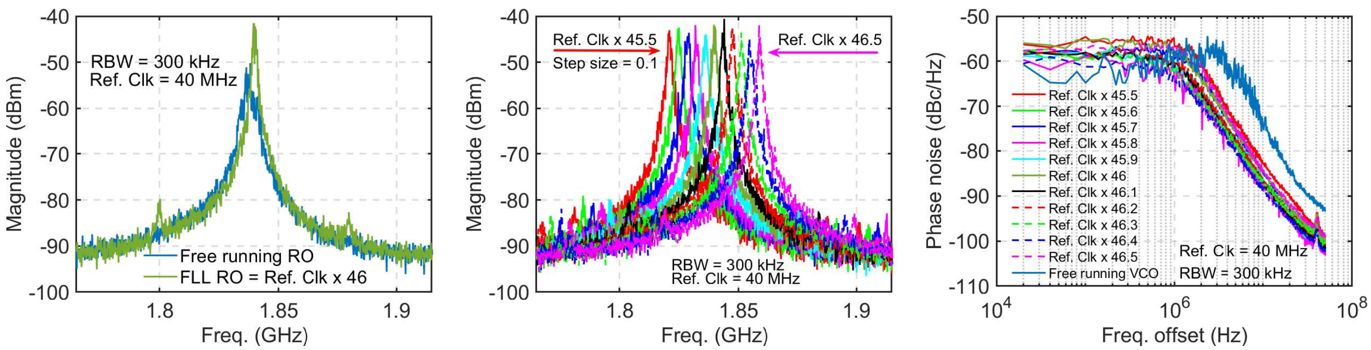


Fig. 3: Die micrograph of the fractional-N digital FLL.



(a) (b) (c)

Fig. 4: Signal spectrum and phase noise when locked and free-running, and when locked using different fractional frequency control words

108 µm, and the current DAC controlling the RO takes 50 µm x 50 µm, in total 0.012 mm^2.

Fig. 4 shows the spectrum and phase noise of the FLL output signal, measured in room temperature (about 25 °C) using a spectrum analyzer. The reference frequency was set to 40 MHz and the coarse tuning setting IFix was set for operation in the 1.85 GHz region and then unchanged. Measurements were performed both when the RO was free running and locked, and as can be seen in Fig. 4a the signal energy is clearly more confined in frequency when locked. The frequency multiplication setting of the circuit was then changed from 45.5 to 46.5 in steps of 0.1. As can be seen in Fig. 4b the circuit can operate over the full fractional range from -0.5 to +0.5. The step size of 0.1, corresponding to 4 MHz, was chosen for figure readability, the circuit has much higher resolution. The reference spurs are about −40 dBc, with worst case at −35 dBc. Fractional spurs cannot be seen above the noise and should thus not impact the performance. The phase noise has an approximately flat level up to 1 MHz offset, corresponding to the oscillator energy being spread over about 2 MHz (double sided), which is then the bandwidth of the IF filter needed in the wake-up receiver, with some margin to ensure that most of the signal energy is inside the filter passband. We can also see that the phase noise at 10 MHz offset is below −82 dBc/Hz for all frequency multiplication factors. In contrast to this, in Fig. 4c we can see that without frequency locking the signal energy is spread over about 8 MHz bandwidth, as the spectrum analyzer shows a phase noise plateau up to 4 MHz offset for the free running oscillator. In Fig. 5 the corresponding power consumption can be seen, plotted versus FLL frequency ratio. The total power consumption is shown, as well as the RO and FLL (mainly digital) part. As can be seen the power consumption is lowest for integer-N operation, i.e. for a frequency ratio equal to 46.0, reaching 50 µW power consumption for a 1.84 GHz frequency locked output signal. For fractional-N operation the power consumption increases, due to the digital part having to perform more non-zero calculations as the fractional frequency departs from zero.

Characterization at elevated temperatures is necessary, since

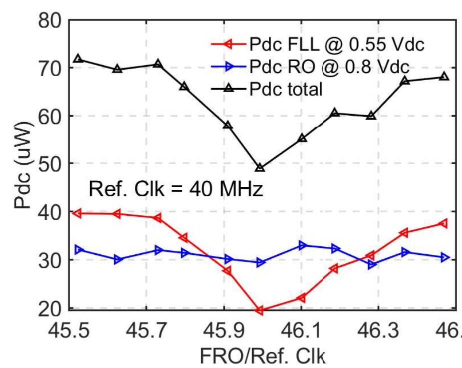


Fig. 5: Power consumption versus frequency ratio, centered at 1.84 GHz, showing a minimum power of 50 µW for integer-N operation.

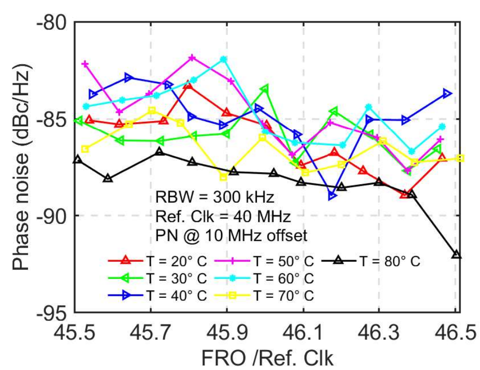
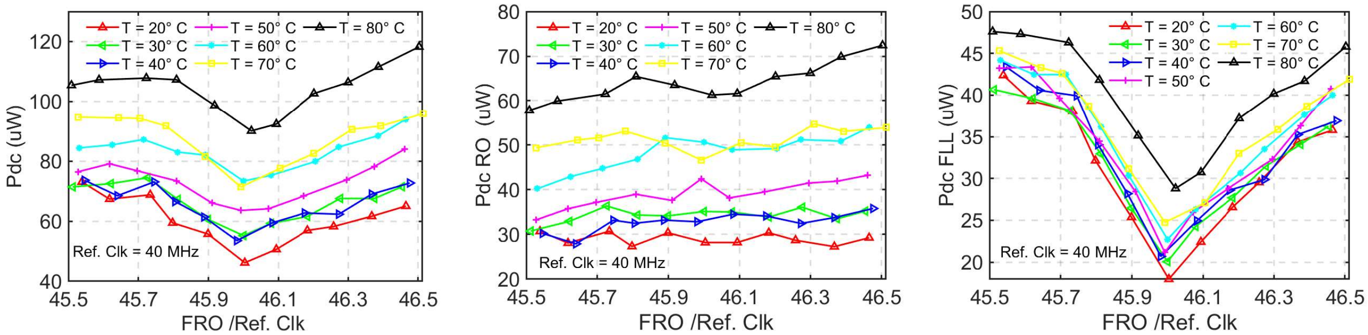


Fig. 6: Phase noise at 10 MHz offset from 20 °C to 80 °C versus frequency ratio, showing a phase noise is below −82 dBc/Hz for all frequency multiplication factors.

the circuit performance is worse at higher temperatures, particularly for the RO. Figs. 6 and 7 present measurements taken in a climate chamber, from 20 °C to 80 °C. In Fig. 6 the phase noise at 10 MHz was measured versus frequency ratio, and as can be seen the worst-case phase noise is rather insensitive to increased temperature, actually going down at the highest temperatures. The power consumption shown in Fig. 7, on the



(a) (b) (c)

Fig. 7: Measurements from 20 °C to 80 °C versus frequency ratio. (a) Total circuit power, (b) RO power, and (c) FLL power (mainly digital part).

other hand, increases with temperature mainly due to the RO, from 46 µW at 20 °C to 90 µW at 80 °C.

IV. Comparison

Table I presents a comparison to published state-of-the-art ultra-low power frequency or phase locked LO generators in the low-GHz frequency range. As can be seen the other works employ phase locking (PLL), providing a more stable output signal with less phase noise. For an OOK wake-up receiver the stability offered by the presented FLL is sufficient, however, and low power consumption is then more important. This work clearly has the lowest reported power consumption of 50 µW. The other works with the two lowest reported power consumption numbers use frequency multiplication to be able to operate the PLL at lower frequency, whereas we operate the RO directly at the output frequency avoiding additional spurs. Our circuit can also operate in fractional-N mode, whereas the other work with the lowest reported power is integer-N, and compared to that we can then obtain a higher output frequency resolution.

TABLE I: Comparison to state of the art

Reference	**This work**	**ISSCC'19 [3]**	**JSSC'19 [4]**	**JSSC'2019 [5]**
Architecture	RO + Digital FLL	PLL + tripler	Digital PLL	RO + PLL + edge comb
Fractional-N	Yes	No	Yes	Yes
Technology	22 nm FDSOI	65 nm	65 nm	40 nm
Supply (V)	0.55 & 0.8	0.5	0.45 & 0.85	0.6
Power (µW)	50[1]-73[2]	166[1]	265[1]	253[1]
Area (mm^2)	0.06[3]	0.25[4]	0.25	0.0166
Fref (MHz)	40	8	10	37.5
Fout (GHz)	1.84[5]	2.4 - 2.5	2.05 - 3.10	2.45 band
PN @ 10 MHz (dBc/Hz)	-82	-94[6]	-124	-95

[1] Power consumption for integer-N operation at room temperature. [2] Power consumption for fractional-N operation at room temperature. [3] Total core area of blocks (DAC,RO,Digital) is 0.012 mm^2. [4] Obscured by FBAR in chip photo, PLL area cannot be accurately estimated. [5] RO has wide range (1.08-1.96GHz),measurements performed about 1.84 GHz. [6] From the extented paper JSSC'21 on the same circuit.

V. Conclusion

This work introduces an ultra-low power frequency-locked local oscillator generator. A three-stage 1.8 GHz ring oscillator is frequency-locked to a 40 MHz reference using an all-digital fractional-N FLL based on sampling the digital state of the ring oscillator. The power consumption including all parts is just 50 µW in room temperature, 66 µW when operating at 1.95 GHz. No frequency multiplication is necessary, avoiding associated spurs. The technique presented offers a very compact chip area and ultra-low power consumption making it suitable for OOK wake-up receivers, where the use of frequency locking can improve both receiver sensitivity and selectivity.

Acknowledgment

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