Bias-Tunable Optical Response of Silicon Nanowire Reconfigurable Phototransistor

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***Abstract*—In this work, the optical characteristics of a silicon nanowire (Si NW)-based reconfigurable phototransistor are investigated for both n-type and p-type operational modes. The presence of sharp Schottky barriers at the source-channel and drain-channel interfaces significantly suppresses off-state leakage current (dark current), enabling high responsivity and photosensitivity. The electronic properties, such as energy band diagrams, electric field distribution, carrier concentration, and transfer characteristics, are analyzed under both dark and illuminated conditions to gain insight into the underlying photo-response mechanisms. Additionally, the transient behavior is evaluated, demonstrating a fast response to the input optical signal. These findings highlight the importance of reconfigurable phototransistors as next-generation photodetectors in CMOS photonic platforms.**

Keywords— Reconfigurable phototransistor, silicon nanowire, Schottky-barrier, ultra-fast response, responsivity, photosensitivity, low dark current.

I. Introduction

Advancements in semiconductor properties and device design have significantly enhanced phototransistor performance, leading to notable improvements in optical behavior parameters such as responsivity, quantum efficiency, response speed, noise characteristics, and spectral range [1] [2]. The evolution of phototransistors has been intrinsically tied to silicon devices, which continue to form the backbone of photodetectors due to their cost-effectiveness and integration capabilities [3] [4]. Despite the advantages, conventional silicon phototransistors face limitations in their narrow spectral response range and quantum efficiency, prompting the exploration of advanced device design and alternative materials to enhance performance [5]. Hence, the photoresponse can be enhanced by pursuing two primary approaches: (1) alternative novel materials and (2) optimization of device design. Recent studies have focused on improving photodetector performance with high-mobility materials like Germanium, InGaAs, GaAs, and emerging 2D materials [6], [7], [8], [9], [10]. These materials offer advantages such as faster response times, higher quantum efficiency, and broader spectral sensitivity, addressing key challenges of traditional silicon-based devices [6]. In addition to material innovations, several studies have investigated architectural modifications to improve phototransistor performance. For instance, incorporating a photonic cavity into the active region has been shown to enhance photoabsorption [11], while the use of junctionless nanowire phototransistors effectively minimizes leakage current in the depletion mode, thereby reducing dark current [12]. Another promising approach involves Schottky barrier phototransistors, where incoming light of appropriate wavelength can modulate the Schottky barrier at the interface and induce internal photoemission under reverse-biased

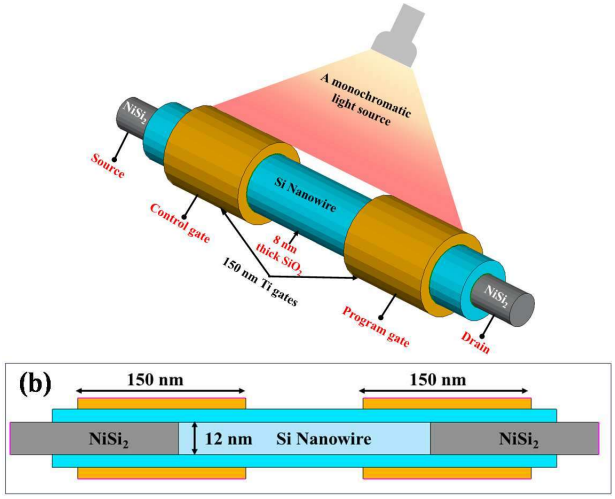

Fig. 1. (a) 3D schematic view of Si NW-based reconfigurable phototransistor with the optical boundary conditions. The inset table shows the parameters of the Si NW length (L_{Si}), diameter (D_{Si}), and $NiSi_2$ workfunction (Φ_{NiSi2}). (b) Cross-sectional view along the channel length, highlighting the overlap of the program and control gates.

conditions, thereby enhancing photosensitivity and the speed of the photoresponse [13].

Although significant improvements in photoresponse are observed in these device designs, the design still could be further improved for compatibility with on-chip CMOS photonics platforms. The reconfigurable field-effect transistors (RFETs) stand out due to their ability to switch operational modes by simply adjusting the terminal bias voltages, offering enhanced versatility for optoelectronic applications with very low dark current [14].

Therefore, the aim of this work is to enhance optical performance by utilizing a silicon nanowire (Si NW)-based reconfigurable field-effect transistor (RFET) [15]. To the best of our knowledge, we have, for the first time, performed a comprehensive analysis of the electronic and transfer characteristics of a reconfigurable phototransistor for both p-type and n-type operations under dark and light conditions. Additionally, the speed of the reconfigurable phototransistor is assessed by determining its rise time and fall time, while key performance metrics are summarized in the figure of merits table.

II. Device Calibration And Simulation Setup

Fig. 1 shows a 3D schematic view of the Si NW-based reconfigurable phototransistor, which is primarily governed by the nature of Schottky barriers at the source-channel and channel-drain interfaces. In the on-state, the current is dominated by tunneling through the Schottky barrier at the source-channel interface, whereas in the off-state, thermionic emission of charge carriers at the barrier junction dictates the

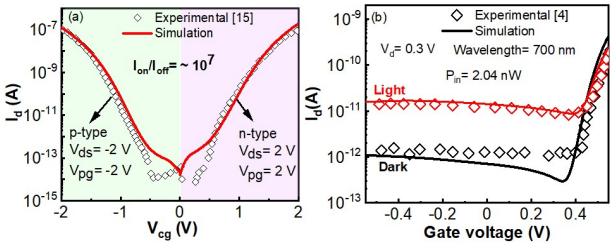

Fig. 2. Calibrated transfer characteristics (I_d): (a) as a function of control gate voltage (V_{cg}) for both p-type and n-type operation with a fixed program gate voltage (V_{pg}) and drain-source voltage (V_{ds}), and (b) as a function of gate voltage for the junctionless Si NW transistor under dark and with input light power (P_{in} = 2.04 nW).

current behavior [14]. This device's dimensions are as follows [15]: The length and diameter of the silicon nanowire are 220 nm and 12 nm, respectively. Nickel silicide ($NiSi_2$) metal is used for the source and drain electrodes, forming Schottky barriers at the source-channel and drain-channel interfaces. The 8 nm SiO_2 layer wrapping the top of the Si NW serves as both the shell and the gate oxide. Titanium (Ti) metal is utilized for both the control and program gates, which extend over the Si-$NiSi_2$ interfaces at both junctions to modulate the Schottky barrier height. To enhance electrostatic control over the Schottky barrier, the Ti gates overlap the $NiSi_2$ region by 90 nm and the silicon nanowire by 60 nm. The analysis is conducted using the *Sentaurus* TCAD platform, incorporating various physical models to achieve accurate calibration of the computational framework [16].

The hydrodynamic model is included to compute carrier transport phenomena, by solving the continuity equation, particularly for short-channel devices [17]. Fermi-Dirac statistics are used for carrier distribution, and the density gradient model accounts for quantum confinement effects. The Phillips Unified mobility model is used for doping concentration, carrier-carrier, and phonon scattering, while the Lombardi model is used for acoustic scattering and surface roughness at Si-SiO_2 interfaces. High field saturation model is implemented to address velocity saturation effects under high electric fields. Barrier non-local tunneling at the Schottky interfaces (source-channel and drain-channel) is incorporated using the Wenzel-Kramers-Brillouin (WKB) approximation tunneling model [18]. For reliable calibration, the effective tunneling masses of electrons (m_e) and holes (m_h) are set to $0.3m_o$ and $0.2m_o$, respectively, where m_o represents the rest mass of an electron. Shockley-Read-Hall (SRH) and Auger recombination models are incorporated to account for carrier recombination. In addition to the electronic models, the in-built optics module is activated to analyze the optical behavior of the reconfigurable phototransistor under varying light conditions. A wavelength-dependent complex refractive index model is utilized to compute the absorbed photon density. The light source is applied from the top of the device, with the illumination window encompassing the nanowire region and its interfaces with the source and drain electrodes. The active area of the device for illumination is estimated to be 1.2×10^{-11}cm^2. A ray-tracing optical solver is employed to compute the absorbed photon density. The step-function quantum yield model is adopted to compute the optical generation rate, which incorporates material bandgap effects. A fraction of the calculated optical generation rate is integrated into the generation term of the continuity equation to account for additional photo-induced carriers [7]. The simulation framework, incorporating the proposed physical and optical models, has been calibrated against experimental data. The transfer characteristics of the proposed reconfigurable phototransistor under dark conditions for both p-type and n-type operations exhibit strong agreement with experimental results [15], as shown in Fig. 2(a). However, before activating the optical module in the reconfigurable phototransistor, it is calibrated with experimental data from a silicon nanowire-based junctionless device, as shown in Fig. 2(b) [4]. A slight offset, particularly in the dark current, is observed, primarily attributed to noise in the experimental characterization setup.

III. Results and Discussions

A reconfigurable phototransistor is primarily a Schottky barrier-based phototransistor, featuring two gates (program and control) that selectively control the flow of one type of carrier while simultaneously restricting the other within the channel material. The channel is typically undoped or intrinsic, allowing dynamic modulation of carrier transport. The device operates in two modes [19]: the off-state carrier transport is primarily governed by the thermionic emission mechanism, requiring carriers to surmount the Schottky barrier to traverse the channel. In the on-state, both field emission (barrier tunneling) and thermionic emission contribute to current flow. However, as the control gate voltage further increases, the barrier narrows, leading to the dominance of field emission current[19]. Firstly, the optical behavior, in terms of photo-responsivity, of the proposed reconfigurable phototransistor is evaluated by illuminating the active region of the device with a monochromatic light source. The device is operated in reverse bias conditions (V_{cg} = -1 V, V_{pg} = 2 V, V_{ds} = 2 V for n-type operation while V_{cg} = 1 V, V_{pg} = -2 V, V_{ds} = -2 V for p-type operation) to deplete the majority of carriers from the channel region. The responsivity is subsequently calculated using the following formula:

$$R\ (mA/W) = \frac{I_L - I_{dark}}{P_{in}} \quad (1)$$

where I_L is the drain current under light illumination and I_{dark} is the drain current in dark conditions.

The responsivity is evaluated across different wavelength ranges (visible and NIR wavelength spectra), as shown in Fig. 3(a)-(b), revealing a peak responsivity of 160–180 mA/W for the wavelength range of 350–500 nm in both n-type and p-type operations. Furthermore, a detailed analysis is conducted within the same 350–500 nm wavelength range. The photosensitivity is calculated as follows:

$$S = \frac{I_L - I_{dark}}{I_{dark}} \quad (2)$$

Maximum photosensitivity achieved for n-type operation is ~5.3×10^4 while for p-type operation is ~1.1×10^4 at 350-380 nm wavelength range. The transfer characteristics of the reconfigurable phototransistor under dark and light conditions are analyzed for both n-type and p-type operational modes at an incident wavelength of 350 nm. Fig. 3(c)-(d) shows the drain current as a function of control gate voltage (V_{cg}) for n-type and for p-type operational modes under varying illumination conditions. In the reverse-biased (V_{cg} = -1 V for n-type and V_{cg} = 1 for p-type operational modes), electron/hole depletion occurs in the channel region, resulting in a minimal thermionic emission current (3.9×10^{-15} A for n-type and 2×10^{-14} A for p-type). As the input optical power increases, the drain current also rises in the reverse-bias condition due to the increased generation of

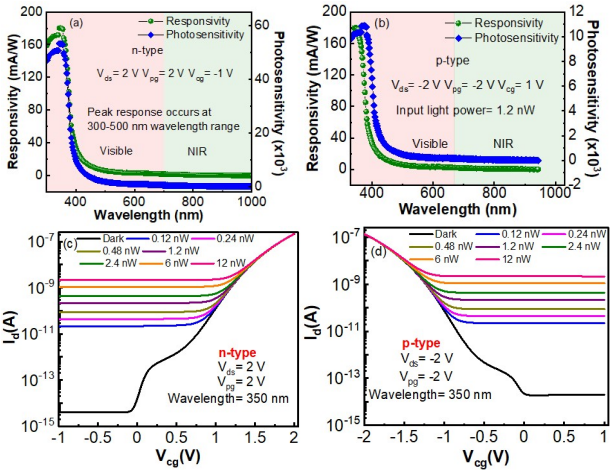

Fig. 3. Responsivity of reconfigurable phototransistor as a function of input wavelength for (a) n-type and (b) p-type operational modes, where input light power is considered to be 1.2 nW. Drain current (I_d) vs control gate voltage (V_{cg}) with dark and light illumination conditions for (c) n-type and (d) p-type operational modes.

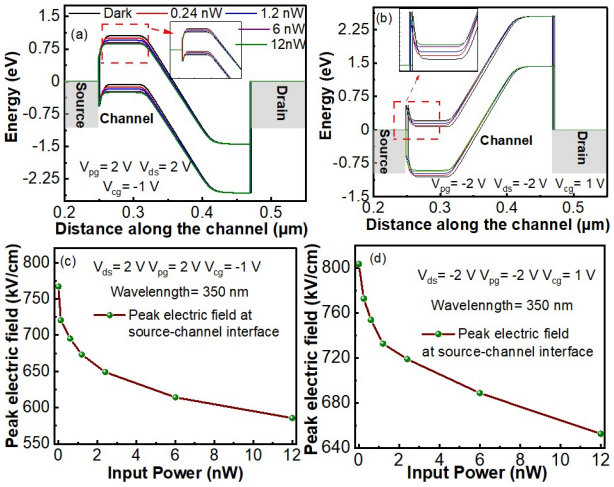

Fig. 4. Energy band diagram of the reconfigurable phototransistor under dark and illumination conditions for (a) n-type and (b) p-type operational modes. Peak electric field at source-channel interface as a function of input light power for (c) n-type and (d) p-type operational modes.

electron-hole pairs in the channel region. However, in the on-state, the drain current remains relatively unchanged, as a significant number of electrons for n-type and holes for p-type are already present due to electrons barrier tunneling for n-type and holes barrier tunneling for p-type at the channel-source interface. At an incident optical power of 12 nW, the ratio of photocurrent to dark current is observed to be $\sim 5.4 \times 10^5$ for n-type operation and $\sim 1.1 \times 10^5$ for p-type operation of the reconfigurable phototransistor.

The electronic properties of the reconfigurable phototransistor in both n-type and p-type operational modes are also evaluated under dark and light conditions to analyze the conduction mechanism and the impact of light on device characteristics. Fig. 4(a)-(b) shows the energy band diagrams of the reconfigurable phototransistor along the channel length for the n-type and p-type operational modes under dark and light conditions at the wavelength of 350 nm. When the reconfigurable phototransistor is reverse biased (V_d = 2 V, V_{pg} = 2 V, V_{cg} = -1 V for n-type, vice-a-versa for p-type operation), barrier tunneling is inhibited, allowing conduction only through thermionic emission, i.e., charge carriers must acquire sufficient thermal energy to surmount the barrier, resulting in minimal conduction. Upon light illumination, electron-hole pairs are generated in the active region of the device. Additionally, as the incident light power increases, the energy barrier decreases due to the higher density of photogenerated carriers in the channel. This reduction in the Schottky barrier is also corroborated by the peak electric field plot, as shown in Fig. 4(c)-(d). The peak electric field is computed at the channel-source interface with respect to the input light power for n-type (see Fig. 4(c)) and p-type (see Fig. 4(d)) operational modes. It is observed that as optical power increases at a fixed wavelength, the peak electric field at the source-channel interface decreases. The primary reason for the reduction in electric field with increasing optical power is the larger number of photogenerated carriers in the channel region, which lowers the magnitude of the barrier potential at the channel-source interface. Additionally, it is noted that the peak electric field in p-type operation is slightly higher than that in n-type operation. This disparity arises due to the asymmetric Schottky barrier heights at the source-channel interface for

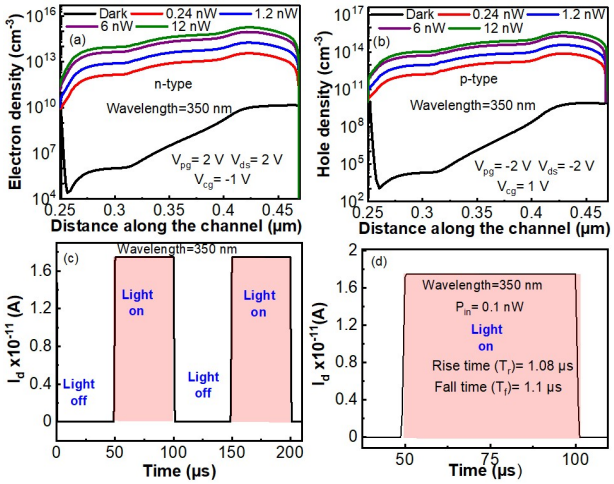

Fig. 5. (a) Electron concentration in the channel region for n-type operational mode and (b) hole concentration in the channel region for p-type operational mode under dark and light conditions. (c) Transient analysis of drain current with respect to time with multiple light pulses and (d) only one pulse at the input power (P_{in}) =0.1nW.

n-type and p-type operational modes. The asymmetry occurs because the metal Fermi level does not perfectly align with the mid-band gap of intrinsic silicon. The carrier concentration in the channel region is computed under both dark and illuminated conditions, as shown in Fig. 5(a) for electron concentration in n-type operation and in Fig. 5(b) for hole concentration in p-type operation, as a function of distance along the channel length. Under dark conditions, due to the reverse-biased configuration, the electron concentration in the reconfigurable phototransistor for n-type operation remains low $\sim 10^4$ near the channel-source interface and $\sim 10^8$ near the channel-drain interface. As the incident optical power increases, photon absorption leads to the generation of additional carriers, thereby increasing the electron concentration in the nanowire channel. At an input power of 12 nW, the maximum electron concentration for n-type operation reaches $\sim 1.8 \times 10^{15}$ cm^{-3}, while in p-type operation, the maximum hole concentration is $\sim 3 \times 10^{15}$ cm^{-3}, as shown in Fig. 5(a)-(b). Due to the presence of a high electric field in the channel region, photogenerated carriers

TABLE I. RECONFIGURABLE PHOTOTRANSISTOR FIGURE OF MERITS

Devices	This Work		Si JL-NW [4]	Ge JL-NW [7]
Type of channel	n-type	p-type	n-type	p-type
Active Area	1.2×10^{-11}cm^2	1.2×10^{-11} cm^2	~6×10^{-10} cm^2	4.4×10^{-11} cm^2
Responsivity	180.36 mA/W	179.78 mA/W	~118 mA/W	50 mA/W
Photosensitivity	5.3×10^4	1.1×10^4	-	~10^3
I_L/I_{dark}	5.4×10^5 @12nW	1.1×10^5 @12nW	~20 @28.79 nW	311.32 @44nW
T_{rise}/T_{fall}	1.08/1.1 µs	1.08/1.1 µs	300/480 µs	2.41 / 3.36 µs

drift toward the drain interface, resulting in a higher carrier concentration near the drain interface compared to the source interface. The transient analysis of the reconfigurable phototransistor is conducted to evaluate its speed performance, as shown in Fig. 5(c)-(d). An input light pulse with a pulse width (T_{pulse}) of 50 µs and a period (T_{period}) of 100 µs is considered. The incident wavelength is set to 350 nm, and the input optical power is 0.1 nW. The photo-response speed is assessed by measuring the rise and fall times of the drain current (I_d) corresponding to the rising and falling edges of the input light pulse. The rise (T_r) and fall time (T_f) of the drain current are determined to be 1.08 µs and 1.1 µs, respectively, for n-type and p-type operational modes. The slight disparity between the rise and fall times is attributed to the difference in carrier recombination rates at the rising and falling edges of the light pulse, leading to an asymmetry in the transient response. The comparative figure of merits for the proposed Si nanowire (NW)-based reconfigurable phototransistors, along with previously reported Si and Ge based phototransistors [4] [7] are summarized in Table 1.

The key performance parameters considered for comparison include responsivity, photosensitivity, the ratio of photocurrent to dark current (I_L/I_{dark}), and switching speed (T_{rise}/T_{fall}). With a minimal active area of 1.2×10^{-11} cm^2, the proposed device demonstrates superior responsivity compared to the devices reported in [4] and [7]. It exhibits higher photosensitivity on the order of 10^4, surpassing that of [7], primarily due to its significantly reduced dark current. The I_L/I_{dark} ratio reaches ~10^5, attributed to the well-defined Schottky barrier at the source-channel interface. This barrier effectively suppresses leakage current under reverse bias, while under illumination, photo-generated carriers modulate the barrier height and enhance internal photoemission, thereby increasing the drain current. Additionally, the proposed device shows the fastest transient response among the compared devices, with T_{rise} and T_{fall} measured at 1.08 µs and 1.1 µs, respectively, which is primarily attributed to the low junction capacitance at the Schottky interface, resulting from the intrinsic nature of the channel material.

IV. CONCLUSION

In this work, the optoelectronic behavior of the Si NW-based reconfigurable phototransistor is investigated to enhance performance in advanced photonics applications on the CMOS platform. The analysis demonstrates high responsivity across different wavelength spectra, achieving a peak responsivity of 160–180 mA/W in the wavelength range of 350–500 nm. At an optical power of 12 nW, the ratio of reverse-bias photocurrent to dark current reaches $\sim 10^5$, attributed to Schottky barrier lowering at the source-channel interface. This enhancement results from increased carrier generation in the channel under illumination, facilitating both internal photoemission and thermionic emission. Furthermore, transient analysis reveals fast photo-response, with T_r and T_f of 1.08 µs and 1.1 µs, respectively. The combination of high sensitivity, low dark current, nano-dimensions, and ultrafast response highlights that the Si NW-based reconfigurable phototransistor could be a strong candidate for next-generation on-chip CMOS photonic platforms.

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