A 12b 1GS/s SAR-Assisted Pipelined ADC with Gain-Error-Cancelled Dual-Path Amplifier and Partially Look-Ahead Parallel Quantization

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***Abstract*—This paper presents a 12b 1GS/s SAR-assisted pipelined ADC, featuring two key techniques for high speed and high resolution: gain-error-cancelled dual-path amplifier and partially look-ahead quantization. Fabricated in 28-nm CMOS, the prototype ADC achieves an SNDR above 60 dB and an SFDR above 72 dB at 1 GS/s across -40 °C to 125 °C and with ±10% supply voltage variation without background calibration. It consumes 9.63 mW, yielding an FoMw of 11.4 fJ/conv-step and FoMs of 167.5 dB.**

Keywords—SAR-assisted pipelined ADC, residue amplifier, gain error cancellation, parallel quantization

I. Introduction

The SAR-assisted pipelined ADC achieves high-speed and power-efficient conversion but faces two main challenges: accurate residue amplification (RA) and fast SAR conversion. Digital calibration can effectively address inter-stage gain errors but introduces design complexity and convergence concerns [1]. To obtain stable gain, open-loop (OL) Gm-R residue amplifiers require sophisticated PVT and linearity compensation [2]. Closed-loop (CL) digital amplifiers [3] and correlated level shifting (CLS) amplifiers [4] mitigate gain error by driving the virtual ground to zero, albeit at the cost of an additional phase. The gain-corrected residue amplifier in [5] eliminate CL amplifier gain error without extra phase, but requires an auxiliary amplifier and a background digital calibration loop, increasing power consumption and circuit complexity. To address these challenges, we propose a gain-error-cancelled dual-path amplifier that employs the OL path to eliminate the gain error of CL path without extra phase. The proposed amplifier avoids background digital calibration and achieves low power consumption through reusing current between the OL and CL paths, resulting in a simplified and efficient design.

The serial nature of SAR conversion consumes significant time, limiting amplification time and overall speed of the SAR-assisted pipelined ADC. The post-amplification residue generation scheme in [6] parallels amplification and quantization, but increases the amplifier output swing. In [7], the subADC samples the MDAC residue and convert it during the amplification phase, achieving parallel conversion and amplification without increasing amplifier output swing. However, this approach introduces an extra phase. Besides, relative offset and full-scale range mismatch between subADC and MDAC necessitate complex calibration logic. To address these issues, we propose a partially look-ahead parallel quantization, where a subrange SAR ADC samples the first stage input and performs look-ahead conversion of the second stage during the amplification phase. This approach

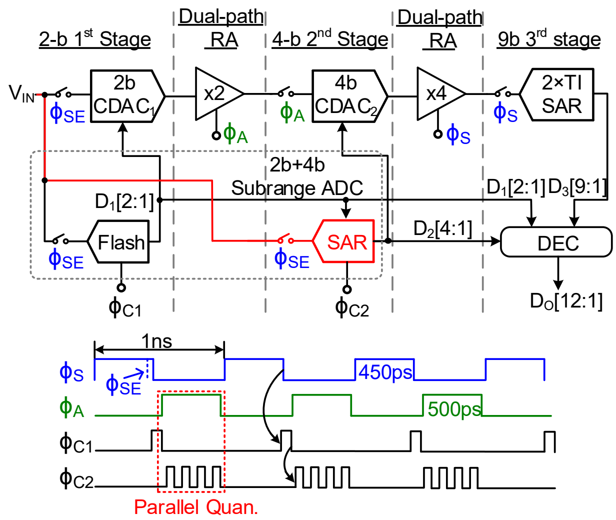


Fig. 1 Block and timing diagram of the proposed ADC.

enables parallel quantization without requiring an additional residue sampling phase or increasing residue swing. Additionally, a low-cost background offset calibration is implemented to prevent the backend ADC from saturating.

With the proposed gain-error-cancelled dual-path amplifier and partially look-ahead parallel quantization, the ADC achieves an SNDR above 60 dB and an SFDR above 72 dB at 1 GS/s across a temperature range of -40 °C to 125 °C and ±10% supply voltage variation without background calibration. Fabricated in 28-nm CMOS, the prototype ADC consumes 9.63 mW from 1V/1.4V supply, resulting in an FoMw of 11.4 fJ/conv-step and FoMs of 167.5 dB.

II. ADC Architecture

The block and timing diagram of the proposed ADC is shown in Fig. 1. It consists of two dual-path amplifiers and three stages, configured as 2b+4b+9b, with 2b inter-stage and 1b inner-stage redundancy. A subrange SAR ADC, integrating a 2b flash and a 4b SAR ADC, performs the conversion of first two stages, while the third stage utilizes a 9b 2× TI-SAR ADC for fine conversion.

After $CDAC_1$ and the subrange SAR ADC sample the input in the first stage, a low-cost 2-bit coarse flash quantizes during the non-overlapping phase, feeding results to $CDAC_1$ and the fine SAR's MSBs to generate the residue. During $CDAC_2$ sampling, the 4-bit fine SAR continues residue conversion until amplification ends, enabling simultaneous

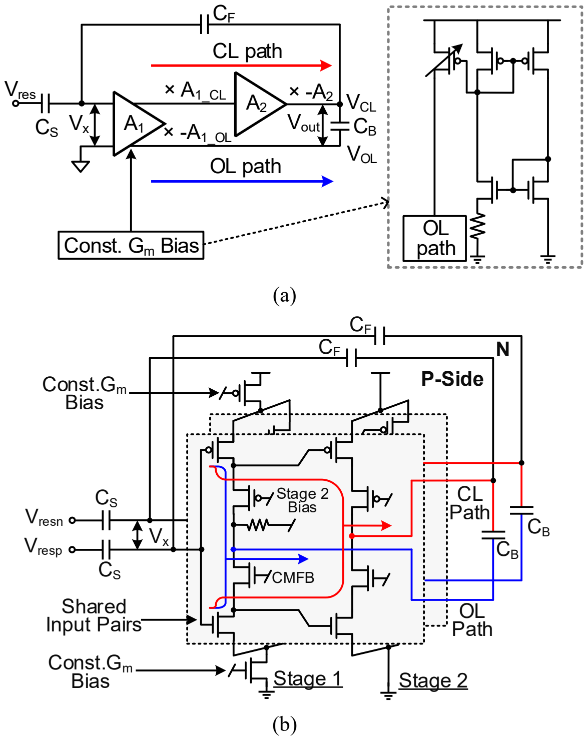


Fig. 2 Proposed gain-error-cancelled two-path amplifier: (a) topology; (b) schematic.

RA and conversion. $CDAC_2$ then generates the residue, which is processed by the backend 9b 2× TI-SAR ADCs.

This architecture establishes a high-speed two-phase timing framework, similar to conventional pipelined ADCs. By extending each stage amplification time to approximately 50% of the clock period, it enhances SAR-based pipelined ADC efficiency while reducing area and power consumption compared to pipelined ADCs that utilize high-resolution flash quantizers.

III. Proposed Gain-Error-Cancelled Dual-Path Amplifier

The topology of the proposed gain-error-cancelled dual-path amplifier (single-ended for simplicity) is shown in Fig. 2(a). The operation principle is similar to that in [5], [8]. In a conventional CL amplifier, the finite loop gain causes a constant gain error V_X/β as the output settles, where V_X is the voltage at the virtual ground and β is the feedback factor. In the gain-error-cancelled amplifier, the gain error in the CL path is effectively cancelled by setting the OL path gain to $1/\beta$ and connecting the OL output to the opposite plate of the load capacitor. Importantly, the cancellation does not introduce any extra phase.

Fig. 2(b) illustrates the schematic of the proposed amplifier: the OL path uses a Gm-R-based amplifier, while the CL path consists of a gm-loaded input stage and a cascode output stage. To improve output swing of stage two, bias voltage and CMFB are implemented in the input stage using trans-linear loop. Since $1/\beta$ is determined by capacitance ratio, it remains stable under VT variations. At power-on, the OL path gain is set to $1/\beta$ by trimming bias current, while the constant gm biasing provides background gain tracking as shown in Fig. 2(a). Consequently, the gain error is effectively cancelled.

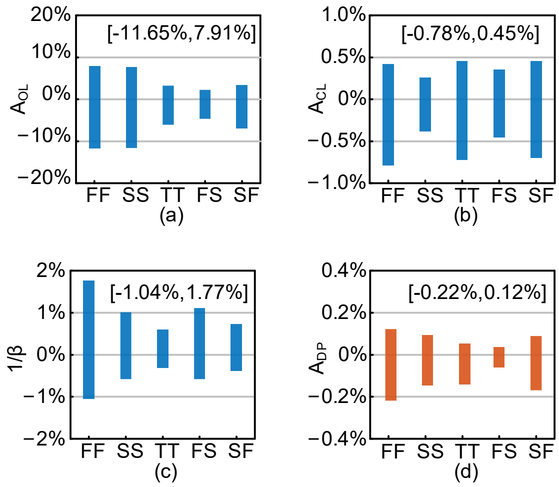


Fig. 3 Simulation results of normalized gain variations over ±10% supply voltage and -40°C to 125°C temperature.

The gain-error-cancelled amplifier not only eliminates the gain error but also minimizes gain variation. As shown in Fig. 3, simulation results indicate that the OL path exhibits normalized gain variations of -11.65% to +7.91%, while the CL path shows variations of -0.78% to +0.45% across ±10% supply voltage and -40°C to 125°C temperature. In contrast, the dual-path structure achieves minimal gain variations of -0.22% to +0.12%. Therefore, the gain error cancellation remains stable over PVT variations.

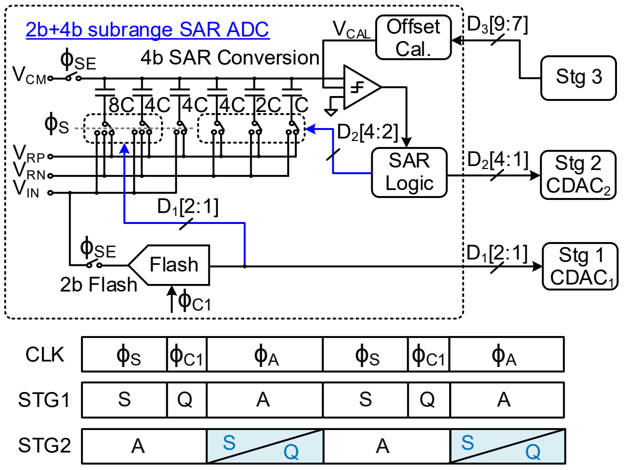
The proposed dual-path amplifier achieves gain error cancellation without requiring an extra phase. Compared to [5] and [8], it reuses both the current and the input pair, resulting in lower power consumption and minimal parasitic capacitance on the virtual ground. The main overhead is the need for foreground bias current trimming to set OL gain, with a complexity comparable to foreground capacitor mismatch calibration.

IV. Proposed Partially Look-Ahead Parallel Quantization

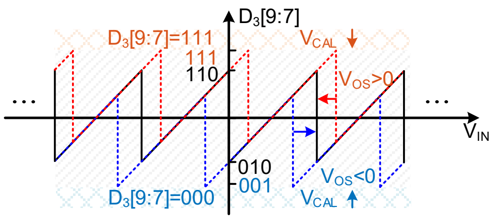
The proposed partially look-ahead parallel quantization scheme, illustrated in Fig. 4, enables parallel sampling and conversion in the second stage, which is implemented using a subrange SAR ADC. This subrange SAR ADC is configured as 2b+4b and incorporates 1b redundancy to align with the inter-stage redundancy between the first and second stages. It samples the first-stage input and performs 2b conversion using a flash ADC during the non-overlapping phase, with the results sent to $CDAC_1$ and the fine SAR ADC to generate the residue. Subsequently, the subrange SAR ADC conducts 4b SAR conversion during ϕ_A, enabling parallel look-ahead quantization.

In the scheme, the 2b flash ADC is employed for the first-stage conversion, minimizing conversion time and reducing the overhead of the flash ADC. Meanwhile, the 4b parallel SAR ADC handles the second-stage conversion, providing low-power multi-bit conversion.

A key challenge in look-ahead quantization is the mismatch error between the second-stage $CDAC_2$ sampling voltage and the 4b look-ahead quantization result, which necessitates background calibration. This mismatch primarily



(a)



(b)

Fig. 4 Proposed partially look-ahead quantization: (a) detailed implementation and timing diagram; (b) background offset calibration of 4b fine SAR ADC.

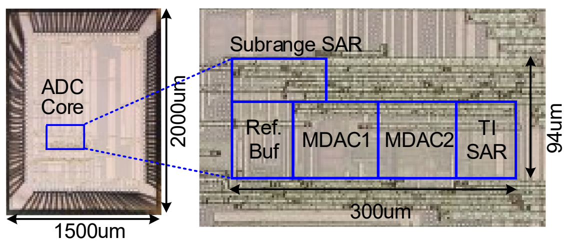


Fig. 5 Die photo.

arises from the offsets of the 4b SAR ADC, the dual-path amplifier and the interstage gain error. Since the dual-path amplifier exhibits minimal gain error, only the relative offset between the 4b SAR ADC and the dual-path amplifier requires calibration.

To eliminate the relative offset, a background offset calibration is employed. The third stage cancels its own offset as in [9], while its three MSBs determine the direction of relative offset adjustment, as shown in Fig. 4(b). To facilitate this adjustment, an additional input pair is introduced to the comparator in the 4b SAR ADC, with its voltage tuned accordingly based on the adjustment direction. The proposed offset calibration is low-cost and fully integrated on-chip.

V. Measurement Results

The prototype ADC, implemented in a 28-nm CMOS process, occupies 0.028 mm² as shown in Fig. 5. Operating at 1 GS/s, it consumes 9.63mW, with the power distribution as follows (Fig. 6): 3.95mW and 2.31mW for the dual-path-amplifier-based $MDAC_1$/$MDAC_2$ from 1V/1.4V supplies,

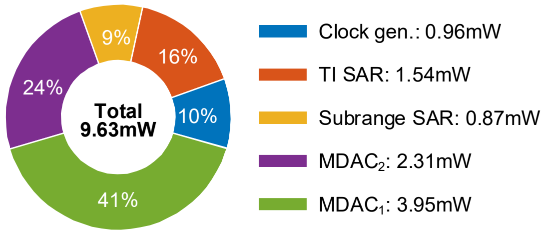


Fig. 6 Power breakdown.

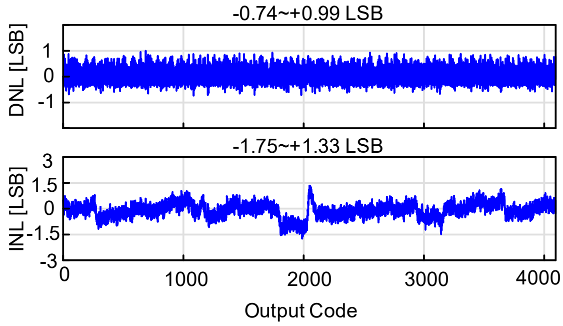


Fig. 7 Measured static performance.

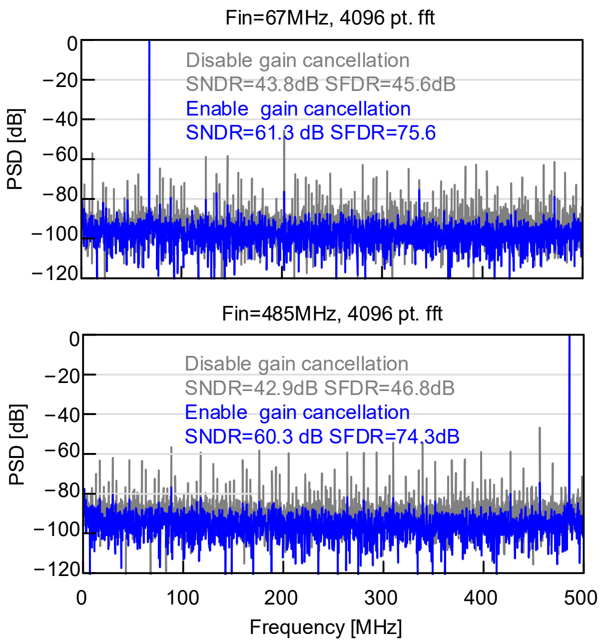


Fig.8 Measured output spectra.

0.87 mW for the subrange SAR, 1.54mW for the TI-SAR backend ADC, and 0.96mW for clock generation. CDAC mismatch errors are foreground calibrated once. The measured DNL and INL as depicted in Fig. 7 are -0.74/+0.99 LSB and -1.75/+1.33LSB.

The measured spectra are shown in Fig. 8. When OL path cancellation is disabled, the measured SNDR/SFDR are 43.8dB/45.6dB at 67-MHz and 42.9dB/46.8dB at Nyquist input. Enabling OL path cancellation improves the SNDR/SFDR to 61.3 dB/75.6 dB at 67 MHz and 60.3 dB/74.3 dB at the Nyquist input.

Across temperature variations from -40°C to 125°C and supply voltage variations of ±10%, all four measured chips achieve an SNDR >60 dB and SFDR >72 dB at Nyquist input, as shown in Fig. 9, demonstrating the VT robustness.

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART HIGH-SPEED AND HIGH-RESOLUTION ADCS

	This work		ISSCC'19 W.Jiang	CICC'22 X.Guo	VLSI'20 B.H.	VLSI'21 L.Wei
Process [nm]	28		28	40	16	28
Architecture	Look-Ahead Pipelined-SAR		Pipelined-SAR	Pipepelined-SAR	Pipelined	Pipelined-SAR
Area [mm^2]	0.028		0.0091	0.022	0.095	0.135
Supply [V]	1/1.4		1	1.15	1	1
Sample rate [MS/s]	1000		1000	625	1000	1000
Resolution [bit]	12		12	13	11	12
SNDR@Nyq [dB]	60.3		60	62.4	59.5	59.3
SFDR@Nyq [dB]	74.3		74.6	70	75.9	67.1
Power [mW]	9.63		7.6	7.05	10.9	19.2
FoM$_S$ [dB]	167.5		168.2	168.9	166.1	160.4
FoM$_W$ [fJ/step]	11.4		9.28	10.5	14.1	25.5
BG Cal. Free	Yes				No	
ΔSNDR [dB] under VT Variation	±10% ΔV	-40~125℃	0~80℃	-40~80℃	--	--
	0.7	0.5	5.3	6.3	--	--
Gain Error Solution	Gain Error Cancellation		TC Comp.	FG. Ref. Trim	--	BG LMS Cal.

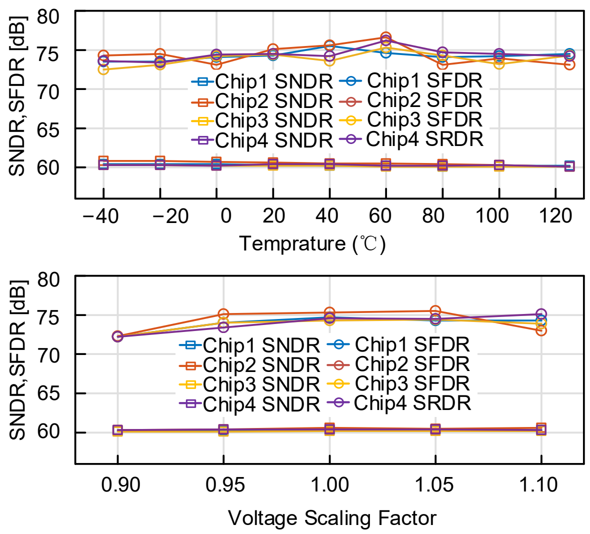


Fig. 9 Measured 4-chip performance under supply voltage and temperature variations.

Table I compares the performance of this work with other state-of-the-art high-speed and high-resolution ADCs. Operating at 1GS/s, this ADC achieves >60 dB SNDR and demonstrates minimal SNDR variation without background calibration under VT variations, attributed to the gain-error-cancelled amplifier and the partially look-ahead parallel conversion.

VI. CONCLUSION

This work proposes a dual-path gain-error-cancelled amplifier and a partially look-ahead parallel quantization scheme. The amplifier effectively cancels gain error without requiring an additional phase or significant hardware overhead, enabling high-speed, high-resolution, and power efficient residue amplification. Moreover, the partially look-ahead parallel quantization extends the amplification time and simplify the clock control through optimized timing arrangements. These two techniques enable a prototype 12b 1GS/s SAR-assisted pipelined ADC that achieves an SNDR >60 dB and SFDR >72 dB at Nyquist input cross temperature variations from -40°C to 125°C and supply voltage variations of ±10%.

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