A 24 GHz Compact 3:1 VSWR-Resilient Power Amplifier with a Reconfigurable Output Matching Network and Integrated Power Sensors

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***Abstract*—This paper presents a 24 GHz power amplifier (PA) with a reconfigurable output matching network (RMN) using switched capacitors that is both compact and resilient to VSWR. Furthermore, power sensors are integrated at the PA input and output for gain estimation and power monitoring. With a 100 MHz single-carrier 64-QAM signal over 3:1 VSWR, after reconfiguration, the P_{AVG} and PAE_{AVG} are > 12.3 dBm and > 14.4%, respectively. The maximum P_{AVG} after reconfiguration is 14.6 dBm, and the maximum PAE_{AVG} is 20.5%. With a fixed P_{AVG} at 12 dBm, the EVM_{rms} is maintained below -25 dB, after reconfiguration.**

***Keywords*—CMOS, Power amplifiers, VSWR.**

I. Introduction

In modern communications and sensing systems, phased arrays are used extensively to meet link budget requirements. However, each antenna element in the array will electromagnetically couple to its neighbors, resulting in an antenna impedance that varies over the scanning angle in the array. This antenna impedance mismatch will cause large variations in the voltage standing wave ratio (VSWR) at the power amplifier (PA) output, severely degrading its performance (e.g. linearity, output power, efficiency) and potentially causing reliability issues. Therefore, it is necessary to develop techniques which mitigate the effects of VSWR on the PA performance. Furthermore, the PA must be very compact, as the area of each transmitter channel needs to be minimized in a large high-density array.

Non-reciprocal output networks, such as circulators, can isolate the PA from the antenna VSWR. However, on-chip circulators have high insertion loss and a large footprint, limiting their potential for integration in large phased arrays [1]. Similarly, the balanced PA architecture also has an inherent resilience to antenna VSWR events by using an output quadrature coupler. As this coupler is often single-ended, differential PAs need an extra balun at the output to interface with it. Therefore, balanced PAs also suffer from a large area overhead, especially since two or more PA paths are required [2], [3], [4], [5]. By the same reasoning, VSWR-resilient reconfigurable Doherty PAs or series-parallel Doherty PAs are also challenging for array level integration [6], [7]. Similarly, the multi-port active load pulling technique in [8] suffers from the same issue where multiple PA paths are needed, and its large-signal linearity over VSWR has not been demonstrated. The paramount concern, as evidenced by all prior works, is to reduce the PA area while maintaining its VSWR resilience. To address this challenge, this paper presents a PA with a reconfigurable output matching integrated at the PA input and output for gain estimation and power monitoring [9].

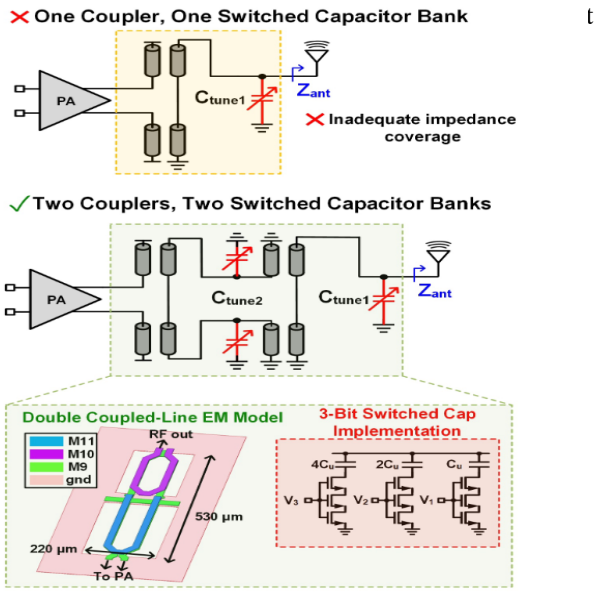

Fig. 1. Reconfigurable matching network with two couplers and two switched capacitor banks.

II. Proposed Reconfigurable Output Matching Network

The implementation of a basic RMN is shown in Fig. 1, adopting a topology with one coupled-line balun and one switched capacitor bank. As shown in the Smith chart in Fig.2, it does not achieve an acceptable impedance tuning range and therefore it cannot recover the PA performance over the majority of VSWR points in the 360º span. Instead, a RMN with two couplers and two switched capacitor banks is used. Compared to the basic RMN, it allows for two switched capacitor banks, shown as C_{tune1} and C_{tune2}, to extend the load impedance reconfiguration region and match a mismatched antenna load to the desired PA loadline impedance. Each cap bank is addressable with three bits, for a total of eight different capacitor values for each bank. Therefore, there are a total of 64 distinct combinations for reconfiguration. Each switch is implemented as a stack of three NMOS devices for an optimum trade-off between switch power handling and insertion loss.

The equivalent resistance of the switch stack when all three switches are on is 2.4Ω. The 3-D electromagnetic (EM) model

of the cascaded coupled-line baluns is only 0.12mm^2. Although coupled lines are usually larger in area compared to

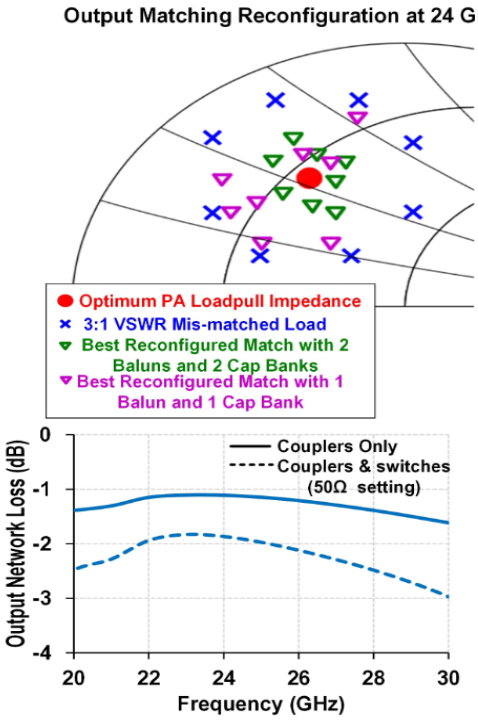

Fig. 2. 360º span, 3:1 VSWR resilience and Output Network Loss.

transformers, they can be designed with much lower loss. For instance, in the implemented RMN, the loss of both couplers combined is just 1.1 dB at 24 GHz. When the switches are added and configured to the 50Ω setting, the loss increases to 1.9 dB.

III. CIRCUIT SCHEMATIC

The top-level schematic of the PA is shown in Fig. 3, and the PA is designed in the GlobalFoundries 22FDX+ process. It consists of a common source (CS) driver and a cascode PA stage. The CS devices in the PA stage are implemented with the ENBFMOAT device variant for its lower parasitics and better RF performance compared to the standard NMOS devices [10]. Furthermore, the common gate (CG) devices in the cascode PA stage are implemented with the EDMOS variant, allowing for better power handling and an elevated total VDD of 2 V. Both the driver and PA stages use neutralization cross-coupled capacitors, enhancing the gain and differential-mode stability. At the output, a VSWR-resilient power sensor is implemented, which uses a differential current sensing loop and single-ended voltage sensing loop, which feed a Gilbert multiplier [9]. This sensor can extract the real power delivered to the complex antenna impedance by using a one-time proportionality factor (PF), which is defined as the average ratio of the sensor output voltage to the PA output power.

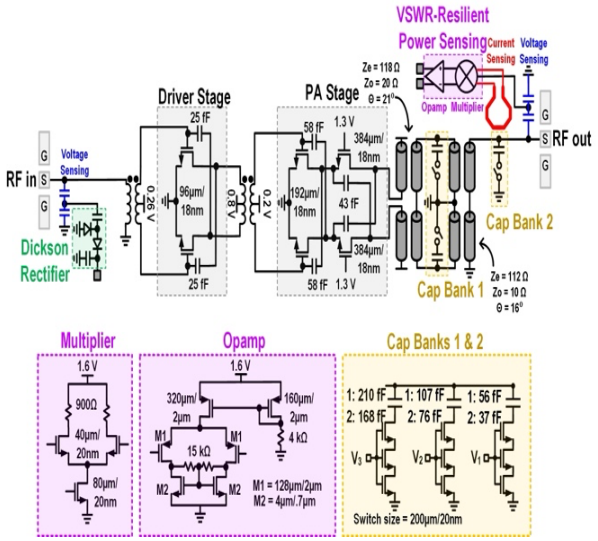

Fig. 3. Top level schematic of the VSWR-resilient reconfigurable PA.

At the PA input, a Dickson rectifier is used to sense the input RF power. Since the two-stage PA has a high S_{12}, the PA input impedance is relatively constant, despite the output load VSWR variations. Therefore, the Dickson rectifier is still accurate for input RF power sensing even with output load VSWR.

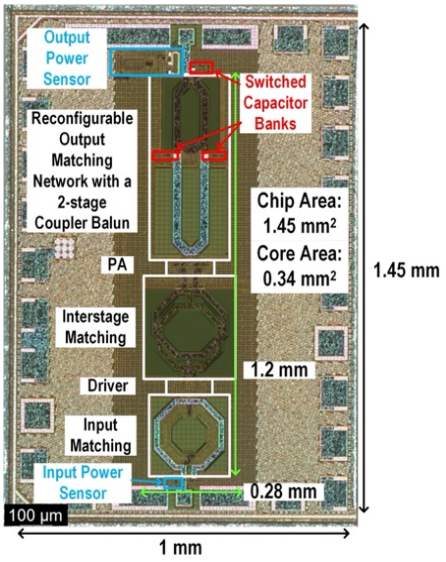

Fig. 4. Chip microphotograph.

IV. MEASUREMENT RESULTS

The PA (Fig. 4) and sensors are first tested with on-chip probing under the 50Ω condition. As shown in Fig. 5, the S_{11} is <-10 dB from 18.8 to 25.5 GHz. With a large signal continuous-wave (CW) test at 24 GHz, the PA achieves an OP_{1dB} of 17.8 dBm and a PAE_{1dB} of 26%. The output of the multiplier-based sensor is shown alongside the PA output, and the PF is shown to vary slightly over P_{out} when compared to an average value.

This error in dB is the integral nonlinearity (INL) of the sensor, and the dynamic range (DR) can then be defined as the range of P_{out} in which the INL is +/- 0.5 dB.

The DR of the input Dickson rectifier-based power sensor is 17 dB, and the DR of the output multiplier-based true-power sensor is 15 dB.

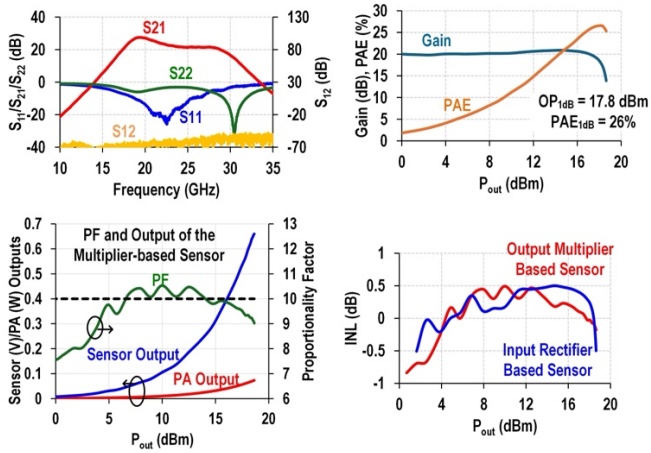

Fig. 5. Measured PA and power sensor performance at 24 GHz and 50Ω.

Then, the PA and sensor are tested with large-signal CW under 3:1 VSWR with both the nominal and the reconfigured settings (Fig. 5). To accurately vary the PA load impedance, a Maury MT985AL impedance tuner is used. Taking a mismatched Z_L = 19 – 18j ($\Gamma = 0.5\angle 225^o$) as an example, the OP_{1dB} is enhanced from 15.5 to 17.3 dBm, and the PAE_{1dB} is enhanced from 23% to 27%. In another case with a mismatched Z_L = 30 – 40j ($\Gamma = 0.5\angle 270^o$), the OP_{1dB} is not changed since it is close to the 50Ω case, even with no reconfiguration. However, the PAE_{1dB} sees a substantial boost from 23% to 29% with reconfiguration. The CW performance summary over 360º VSWR angle (VSWR = 3:1) is shown in Fig. 6. Overall, the PA achieves an OP_{1dB} enhancement at every VSWR angle. Before reconfiguration, the OP_{1dB} is > 15.5 dBm with a range of 2.3 dB, and after reconfiguration the OP_{1dB} is > 17.1 dBm with a range of 0.9 dB. Additionally, the PAE_{1dB} is boosted from > 21% to > 26% after reconfiguring. As the RMN loss varies over both VSWR and switch setting, some angles (e.g. 90º) do not see the full reconfiguration benefit as others. Nevertheless, the overall PA performance is still significantly enhanced with the reconfiguration. Furthermore, the power sensing error (PSE) of the sensors are also measured over VSWR. Ideally, the PF stays constant over VSWR and is equal to the PF at 50Ω. However, in practice the power sensing is not perfect, leading to PSE which is defined as $10\log_{10}(PF_{VSWR}/PF_{50\Omega})$ [11]. For the output/input sensor, the worst case PSE is -2.5 dB and -0.5 dB, respectively.

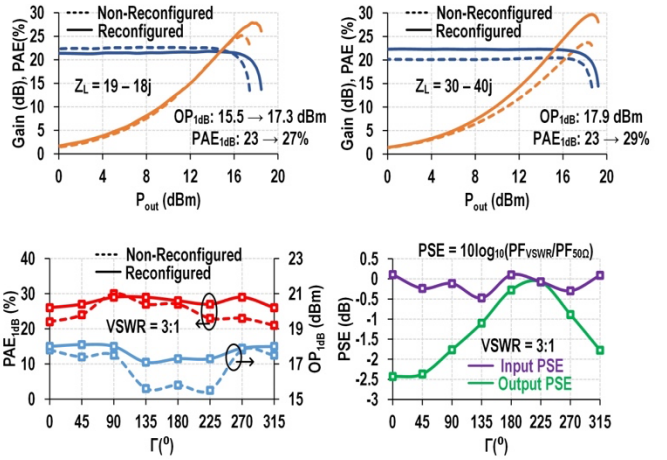

Fig. 6. Measured PA and power sensor performance without and with reconfiguration at 24 GHz under 3:1 VSWR.

Lastly, the PA is tested with a single-carrier 64-QAM signal over VSWR as shown in Fig. 7. Limited by the load tuner, the modulation bandwidth is set to 100 MHz. With a load of 50Ω, the PA achieves an P_{AVG} of 13.2 dBm and a PAE_{AVG} of 17% at an EVM_{rms} of -25.4 dB and a center frequency of 24 GHz. To measure the PA under VSWR, first the EVM_{rms} target is fixed to -25 dB. The measurements are performed under 3:1 VSWR over the full 360º VSWR angles. Without reconfiguration, the P_{AVG} and PAE_{AVG} are >10.5 dBm and > 11.3 %, respectively. After reconfiguration, the P_{AVG} and PAE_{AVG} are > 12.3 dBm and > 14.4%, respectively. The maximum P_{AVG} after reconfiguration is 14.6 dBm, and the maximum PAE_{AVG} is 20.5%. Next, the P_{AVG} is fixed at 12 dBm, and the EVM_{rms} is compared before/after reconfiguration over VSWR. Overall, the EVM_{rms} is maintained below -25 dB, improved from the maximum of -21 dB.

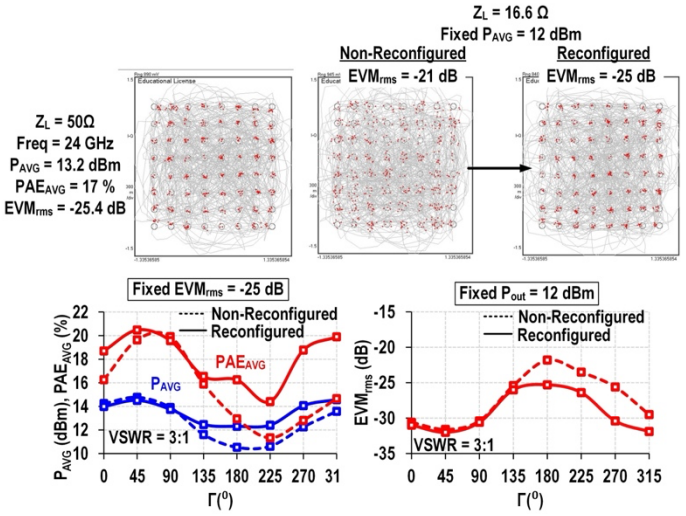

Fig. 7. Modulation measurements without and with reconfiguration using a 100 MHz single-carrier 64-QAM signal at 24 GHz for both 50Ω and 3:1 VSWR loads.

	This Work	N. Mannem ISSCC 2020	G. Diverrez EuMC 2022	G. Diverrez RFIC 2024	M. Pashaeifar ISSCC 2024	M. Pashaeifar ISSCC 2021	C. Chappidi VLSI 2019	M. Eleraky ISSCC 2025
Technology	**22nm FD-SOI CMOS**	45nm SOI CMOS	28 nm FD-SOI CMOS	28 nm FD-SOI CMOS	40nm CMOS	40nm CMOS	65nm CMOS	22nm SOI
Architecture	**Reconfigurable Coupler-Based PA**	Coupler-based reconfigurable series/parallel Doherty	Balanced PA	Inductive Doherty PA	Chain-Weaver Eight-Way Balanced PA	TX with Doherty Balanced PA	Broadband Doherty-like	Complex-Cascode LC-Neutralized
Supply (V)	**2**	2	2	2	2	1	1.1	1.96
Freq. (GHz)	**24**	39	26	28	37	26	28	39
Gain (dB)	**20**	12.5	20	22	29.9	21.8 (TX)	15*	22.7
OP1dB, 50Ω (dBm)	**17.8**	20.2	20.5[a]	19.8	22.67	20.1	19	17.3
OP1dB, 3:1 VSWR (dBm)	**17.1 – 18 (with reconfig.)**	18.5 - 19.12	18.5 - 19.5*[a]	> 18.2[a]	> 20*	N/A	> 17 (4:1 VSWR)	11.5 - 15.5*
PAE1dB, 50Ω (%)	**26**	32.2	39[a]	34.4[a]	16.18[a]	29[b]	21.6	37
PAE1dB, 3:1 VSWR (%)	**26 – 29 (with reconfig.)**	20.6 - 25.3	25 - 28*[a]	> 24*[a]	N/A	N/A	N/A	17.5 - 30*
Sensor Integration	**Yes**	No	No	No	Yes	Yes	No	No
Modulation	**Single-carrier 64-QAM**	Single-carrier 64-QAM	64-QAM 5G NR FR2	64-QAM 5G NR FR2	64-QAM OFDM	Single-carrier 64-QAM	64-QAM OFDM	Single-carrier 64-QAM
Load Impedance	**3:1 VSWR**	3:1 VSWR	50Ω	50Ω	50Ω	3:1 VSWR	50Ω	3:1 VSWR
Data Rate (MHz)	**100**	100	500	200	2000	100	1000	100
Freq. (GHz)	**24**	39	29	24	37	27	28	39
EVM_{rms} (dB)	**-25**	< -22	-21.37	-22	-25	< -25	-22.2	< -24.6
$Pout_{avg}$ (dBm)	**> 12.3**	> 11.2**	11.58	11.8	16	> 10*	7.5	> 7*
PAE_{avg} (%)	**> 14.4**	> 9.6**	N/A	11.9	4.1	N/A	5.1	> 10.5*
ACPR (dBc)	**< 23.3**	< -22.8	-28	-27.5	-29.8	N/A	N/A	N/A
Core Area (mm^2)	**0.34**	1.18	0.9	0.82	2.08	1.38	1.35 (chip area)	0.093

* Estimated from plots [a] Psat/PAEsat

** EVMrms = - 24 dB [b] Drain Efficiency

Table 1. Comparison table with state-of-the-art-mm-Wave-resilient PAs.

Table 1 shows the comparison between the proposed PA and other state-of-the-art mm-Wave VSWR-resilient PAs. This PA is the most compact design, with a core area reduction of over 2.4× over the next smallest design. Furthermore, this PA achieves the highest PAE under 3:1 VSWR after reconfiguration. Due to its substantially improved linearity after reconfiguration, this PA also has the highest modulated output power and efficiency under a 3:1 VSWR. Most importantly, this is the first mm-Wave VSWR-resilient reconfigurable PA design that is co-integrated with on-chip real power sensors, achieving enhanced modulation performance over 3:1 VSWR and the full 360º span.

V. CONCLUSION

This paper describes a PA architecture that achieves 3:1 VSWR resiliency through its reconfigurable output matching network.

From Table 1, this PA achieves a core area reduction of over 2.4× over the next smallest design. With a 100 MHz single-carrier 64-QAM signal over 3:1 VSWR, after reconfiguration, the P_{AVG} and PAE_{AVG} are > 12.3 dBm and > 14.4%, respectively. The maximum P_{AVG} after reconfiguration is 14.6 dBm, and the maximum PAE_{AVG} is 20.5%. With a fixed P_{AVG} at 12 dBm, the EVM_{rms} is maintained below -25 dB, after reconfiguration.

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