Stacked 2D Monolayer MoS_2 Nanosheet FET with Gate-all-around and Top gates Architecture

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***Abstract*—In this work, we present, for the first time, a stacked 2D nanosheet FET featuring a gate-all-around (GAA) and top-gate architecture with monolayer MoS_2 channels. Additionally, a gate-last process is introduced to scale down nanosheet FETs to a channel width of 40 nm without inducing damage to the MoS_2 monolayer. For the first time, conformal gate stack deposition on monolayer MoS_2 is achieved without an interfacial layer. The electrical performance of the devices is systematically evaluated in terms of device yield, subthreshold slope (SS), and on/off current ratio. This successful demonstration of 2D nanosheet FETs highlights their strong potential as fundamental building blocks for future 2D CFET applications.**

Keywords—2D, GAA, Nanosheet FET, CFET, Monolayer MoS_2

I. Introduction

In the AI era, the exponential growth of data generation and dissemination continues to drive increasing computational power demands, necessitating the extension of Moore's Law. However, as silicon thickness scales down to just a few nanometers, carrier mobility significantly degrades due to surface roughness scattering, limiting further miniaturization. Two-dimensional (2D) semiconductors, particularly transition metal dichalcogenides (TMDCs), have emerged as promising alternatives due to their superior carrier transport properties and enhanced resistance to short-channel effects at advanced technology nodes [1], [2].

When integrated with gate-all-around (GAA) architectures, 2D FETs further enhance power, performance, and area (PPA) efficiency, offering significant advantages for next-generation transistors [4]-[7]. Nevertheless, critical challenges such as process integration complexity, thermal/chemical stability of 2D channels, and fab compatibility remain unresolved bottlenecks for 2D semiconductor technology [8]-[12]. Inspired by silicon-based transistor advancements, the foundational structure of 2D complementary field-effect transistors (CFETs) is illustrated in Fig. 1(a), featuring vertically stacked 2D n- and p-type channels. Figure 1(b) outlines the developmental roadmap for 2D FETs, progressing from planar architectures to nanosheet FETs and ultimately to 2D CFETs. The stacked 2D nanosheet FET with gate-all-around (GAA) and top-gate architectures represents an intermediary step toward this evolution.

In this work, we have developed a gate-last process for stacked 2D nanosheet FETs by combing the GAA and top gates stack for the first time. In addition, conformal GAA high-k and metal deposition were achieved in a fab-compatible reactor without interfacial layer. Operational stacked 2D nanosheet FETs with monolayer MoS_2 are presented, showing high potential for the future 2D CFET chip integration.

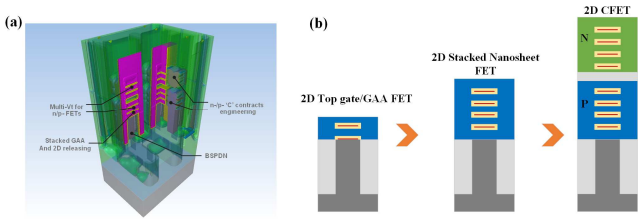

Fig. 1. (a) Schematic diagram of the stacked 2D CFET. (b) Similar to silicon nodes, the possible path for 2D FETs, from the 2D Nanosheet FET to 2D CFET.

II. Results and Discussion

A. Stacked 2D Nanosheet FETs process simulation

To achieve the final device architecture of stacked 2D CFETs, it is essential to evaluate the integration of a stacked nanosheet FET with a 2D monolayer. Figure 2(a) illustrates the key fabrication process flow for the stacked 2D nanosheet FET featuring a gate-all-around and top-gate architecture, as virtually processed using SEMulator3D (Fig. 2(b)–(i)). Based on '3D virtual fabrication' via COVENTOR, critical process and integration aspects are elucidated. The feasibility of the gate-first process was developed at several key stages, including the multi 2D transfer onto oxide trenches and fine contacts, 2D sheet release, and GAA gate stack deposition.

The substrate for the fabricated devices was prepared on a 300 mm silicon wafer with a 90 nm thermally grown SiO_2 layer, incorporating electron-beam markers. The wafer was diced into 26.5 × 26.5 mm coupons. Trenches defining the gate length were patterned using electron-beam lithography and subsequently etched via reactive ion etching (RIE). A monolayer of MoS_2 was transferred onto the substrate, followed by the deposition of 50 nm palladium (Pd) source and drain contacts using a lift-off process. A second MoS_2 monolayer was then transferred, suspended across the trench and fine contacts. The active area was patterned in a single RIE step, followed by the deposition of a 10 nm HfO_2 gate dielectric and a 20 nm TiN gate electrode using atomic layer deposition (ALD). Finally, metallization was performed with 50 nm Pd deposited by electron-beam evaporation after via opening.

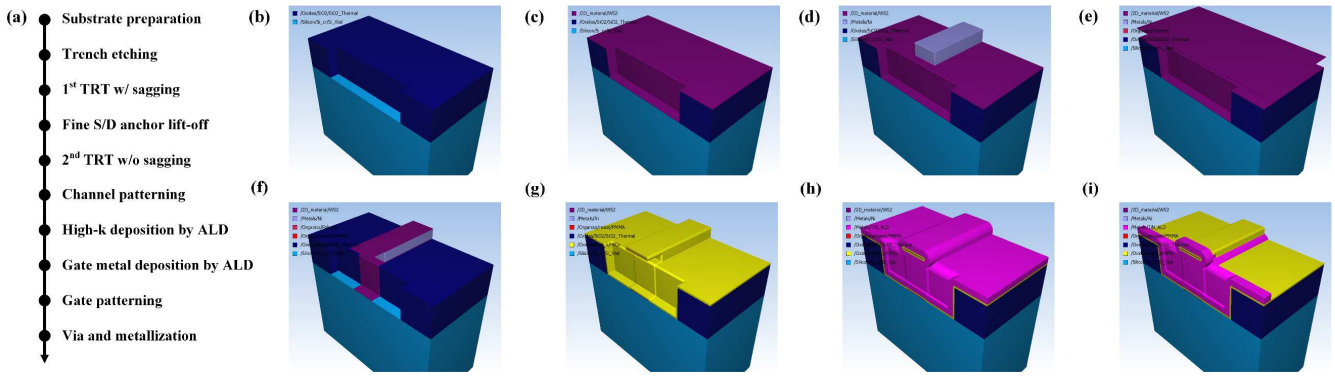

Fig. 2. SEMulator3D-based process simulation of the front-end-of-line (FEOL) fabrication for a stacked 2D nanosheet FET with GAA and top-gate architectures. (a) Key fabrication steps for a stacked 2D nanosheet FET using a gate-last integration scheme. Steps (b)–(i) illustrate the corresponding simulated process flow, including 2D transfer, channel definition and gate stack deposition, modeled using the COVENTOR platform.

B. TMD growth, characterization, and transfer

Large-grain monolayer MoS_2 was grown on a 2-inch sapphire wafer by metal-organic chemical vapor deposition (MOCVD). Fig. 3(a) presents an atomic force microscopy (AFM) image of a continuous monolayer of large-grain MoS_2 on sapphire, demonstrating its high uniformity. The monolayer MoS_2 channel for nanosheet FETs was subsequently prepared via a thermal release tape (TRT) transfer from the sapphire to a SiO_2 substrate. The Raman spectra in Fig. 3(b) further confirm the monolayer characteristics and superior quality of the MoS_2 film before and after TRT.

Notably, for TRT performed on nano-trenches, smaller trenches had a lower delamination yield compared to larger trenches [13]. A nano-trench with a high aspect ratio and a depth of 50 nm was fabricated using an optimized RIE process. To further enhance the adhesion of the monolayer MoS_2 film on the substrate, an oxygen plasma treatment was applied to the SiO_2 surface prior to the TRT transfer. Additionally, a post-annealing treatment was utilized to reduce the 2D film exfoliation [14].

C. Conformal high-k oxide and gate metal deposition

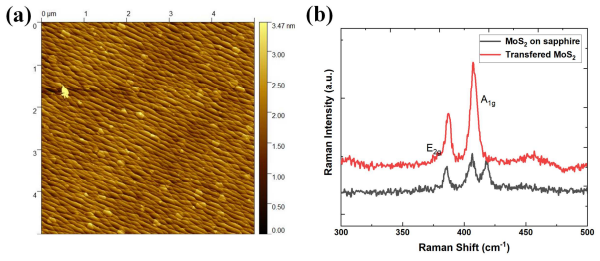

Fig. 3. (a) Tapping-mode AFM topographic image of a continuous monolayer MoS_2 film with large-grain morphology on a sapphire substrate before TRT. (b) Room-temperature Raman spectra of monolayer MoS_2 on sapphire (pre-TRT) and transferred to a silicon substrate (post-TRT), highlighting the E^1_{2g} and A_{1g} vibrational modes as markers of structural integrity. Substrate-dependent peak shifts are evident post-TRT.

As reported in our previous work [15], the mechanical limitations of 2D TMD monolayers necessitate defining the sagging ratio as a function of the SiO_2 trench depth, and the width and length of the 2D nanosheet in the absence of anchor support. With an increase in trench length from 50 nm to 500 nm, the sagging ratio of the monolayer MoS_2 film gradually increases. For a trench with a depth of 50 nm and a length of 200 nm, the monolayer MoS_2 film progressively conforms to the bottom of the trench following the initial TRT [16]. Subsequently, the second 2D layer is suspended across the trench with the aid of fine contacts. Thereafter, the 2D channel is etched by RIE using PMMA as a protective resist. To mitigate sagging induced by the polymer's viscosity and the capillary forces of solvents, a critical point drying (CPD) process utilizing supercritical CO_2 ($SCCO_2$) was developed to remove the resist after MoS_2 patterning. Finally, remote H_2 plasma cleaning is employed to eliminate residual polymer on the MoS_2 surface prior to the deposition of high-k and gate dielectric layers by ALD.

In our previous work, we developed a surface physisorption-based soaking process to nucleate a sub-1 nm AlOx interfacial layer on the non-reactive surface of TMDs, facilitating subsequent HfO_2 deposition by exposing MoS_2 to a high vapor pressure of TMA [17]. In the present study, the extremely narrow width of the 2D nanosheet promotes nucleation from the boundaries and defect sites near the edges, as illustrated in Fig. 4. Following the growth of a 10 nm HfO_2 layer at 300 °C using $HfCl_4/H_2O$ as the high-k precursor, a 20 nm TiN gate metal was deposited by ALD using $TiCl_4/NH_3$ at

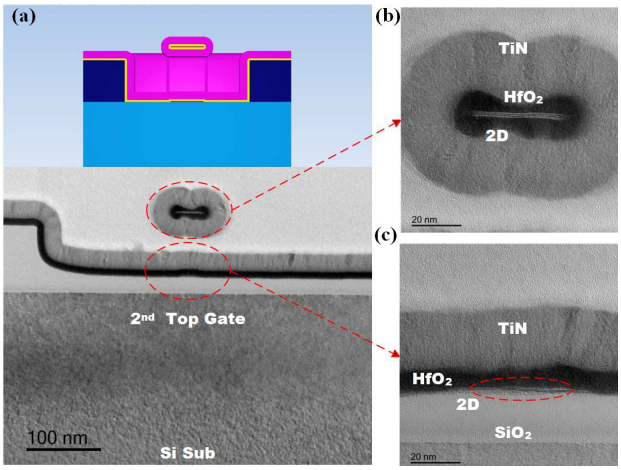

Fig. 4. (a) Cross-sectional TEM image of a 2D Nanosheet FET with a MoS_2 nanosheet channel width of 40 nm. Inset: Cross-sectional schematic corresponding to the device in Fig. 2(i). (b) High-resolution TEM image of the top GAA structure, highlighting the conformal gate stack encapsulation and flat monolayer MoS_2 channel. (c) High-resolution TEM image of the top gate stack for the second 2D nanosheet.

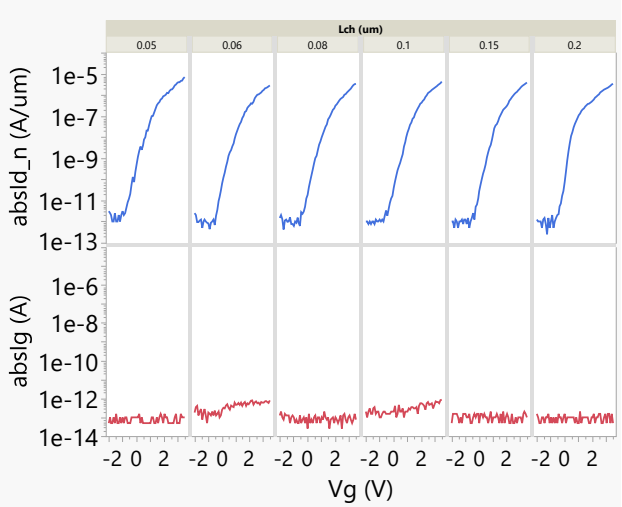

Fig. 5. Median transfer characteristics and gate leakage current of all stacked 2D nanosheet NS-FETs across channel lengths ranging from 50 nm to 200 nm and gate voltage sweeping from -2.0 V to 3.5 V.

350 °C. Figures 4(b) and 4(c) show a clearly defined MoS_2 layer without an interfacial layer between MoS_2 and HfOx. Both the TiN and HfOx films exhibit excellent coverage and conformal profiles, effectively wrapping the 40 nm wide top monolayer MoS_2 nanosheet. Additionally, as shown in Fig. 4(c), the bottom 2D nanosheet is capped by the planar top gate stack. Following the conformal gate deposition, the gate metal was removed using time-based dry etching. Subsequently, the source and drain windows were opened on the fine contact surface, and device fabrication was finalized via metallization.

D. Electrical characterizations of stacked 2D Nanosheet FETs

Figure 5 presents the median transfer characteristics and gate leakage of stacked 2D nanosheet FETs with channel lengths (Lch) ranging from 50 nm to 200 nm. The on-current exhibits a slight decrease as Lch increases, measured at a drain

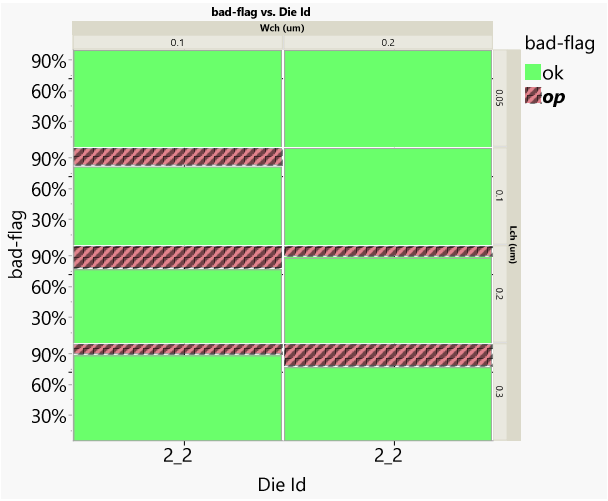

Fig. 6. Yield comparison of stacked 2D nanosheet FETs with channel lengths ranging from 50 nm to 200 nm and channel widths of 100 nm and 200 nm. The analysis contrasts normal current-voltage (IV) characteristics with open-circuit devices. As channel length increases, the sagging ratio rises, leading to a higher rate of nanosheet collapse.

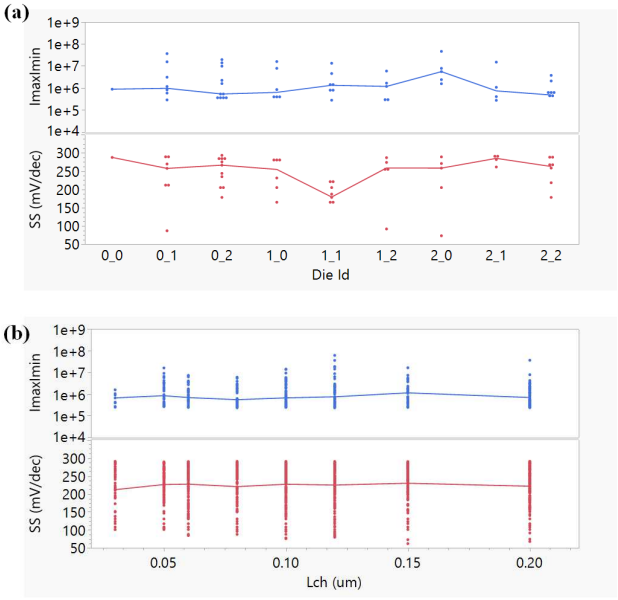

Fig. 7. (a) I_{ON}/I_{OFF} ratio and SS variations of stacked 2D nanosheet FETs across different dies. (b) I_{ON}/I_{OFF} ratio and SS variations of stacked 2D nanosheet FETs for various Lch.

voltage (Vd) of 1 V with the gate voltage (Vg) swept from -2.0 V to 3.5 V. The elevated contact resistance is attributed to the absence of doping in the contact areas and the extended access regions between the gate, source, and drain. All devices demonstrate low gate leakage currents, underscoring the stability of the gate stack. Figure 6 illustrates the yield of 2D nanosheet FETs with Lch ranging from 50 nm to 200 nm and channel widths (Wch) of 100 nm and 200 nm, determined by comparing functional devices with open-circuit devices. Notably, as the channel length increases, the sagging ratio also increases, leading to a higher propensity for nanosheet collapse. Fig. 7(a) and (b) present the I_{ON}/I_{OFF} ratio and subthreshold slope (SS) of stacked 2D nanosheet FETs across different dies and channel lengths. The top-performing devices demonstrate excellent performance, achieving an SS of ~70 mV/dec and an I_{ON}/I_{OFF} ratio of ~10^8. Variations in SS and ON/OFF ratio are attributed to process-related factors, including non-uniform 2D film deposition and sagging effects. The integrations of the stacked 2D Nanosheet FETs gate last flow can be further improved. The trench with high depth can be introduced to get the suspend bottom channel. The performance may be further enhanced by improving TMD mobility, reducing the access region, and incorporating additional TMD nanosheet layers.

III. Conclusions

In this work, we present an integration flow for stacked 2D nanosheet FETs employing a combined gate-all-around and top-gate architecture using dual MoS_2 nanosheets. The process feasibility of critical modules is evaluated via COVENTOR, and the electrical performance of the devices is comprehensively analyzed in terms of device yield, subthreshold slope, and on/off current ratio.

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