# First Demonstration of High Performance IGO TFT with Mobility >30cm$^2$V$^{-1}$s$^{-1}$ and Ideal Stability at Cryogenic Temperatures Down to 2 Kelvin

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***Abstract*—In this work, we have presented an indium-gallium oxide (IGO) transistor demonstrating exceptional stability and high carrier mobility under ultra-low-temperature conditions. At 2K, the device maintains a $\mu_{FE}$ > 30cm²V⁻¹s⁻¹, achieves an $I_{on}/I_{off}$ ratio of $10^8$, and exhibits a distinct positive $V_{TH}$ of 5.5V. In contrast, room-temperature operation reveals band-like transport characteristics with a maximum $\mu_{FE}$ of 45cm²V⁻¹s⁻¹. A notable polarity reversal of $V_{TH}$ to positive occurs at ~ 100K during cooling, accompanied by an anomalous mobility increase during the 5K ~ 2K transition regime. Temperature-dependent electrical characterization identifies ultralow band-tail states in IGO Urbach energy ($E_U$) ~ 5.4meV, enabling direct electron excitation into the $E_C$ for efficient transport. Four-probe measurements further confirm a remarkably low contact resistance of 1kΩ·cm at 2K. These findings establish IGO as a promising material platform for cryogenic electronics, offering critical insights for quantum computing and deep-space exploration technologies.**

***Keywords*—Cryogenic, Amorphous semiconductor, InGaO, Mobility, Quantum computing**

## I. Introduction

The growing demand for cryogenic electronics stems from next-generation computing paradigms like quantum systems and AI accelerators, where ultra-low-temperature operation suppresses thermal noise and enables to high fidelity qubit control [1, 2]. In quantum-classical hybrid architectures, peripheral circuits (e.g., cryogenic DRAM for qubit state buffering) must be co-integrated with quantum processors operating in sub-Kelvin regimes. This integration requires transistors exhibiting high mobility (>30cm²V⁻¹s⁻¹) and bias stability at corresponding cryogenic temperature (e.g., below 4K) [3, 4].

Amorphous oxide semiconductor thin-film transistors (AOS TFTs), particularly InGaZnO-based devices, have gained attention for their low-temperature processing (<300°C) and ultralow off-state current (< $10^{-18}$A/μm), making them compatible with 2T0C 3D DRAM architectures [5-8]. However, standard IGZO TFTs exhibit thermally activated charge transport, where carrier mobility drastically decreases below 100K due to electron localization in Urbach tail states with characteristic energies > 20meV [9, 10].

In this work, we investigated Indium-Gallium Oxide (IGO) films for potential applications in high-performance cryogenic thin-film transistors (TFTs). With an ultrahigh In-Ga ratio (30:1), the IGO-TFTs exhibit ideal cryogenic transport behaviors, demonstrating a mobility exceeding

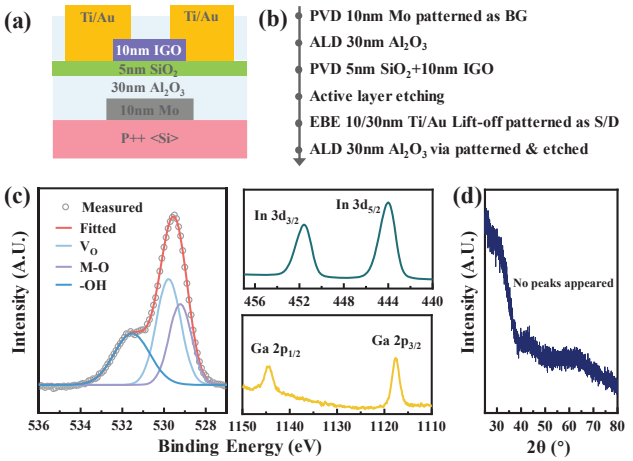


Fig. 1. (a) Device structure of the IGO BG TFT in this work and (b) detailed fabrication process flow; (c) XPS spectra for O1s, In3d, Ga2p, of the IGO film; Metal-oxygen (M-O), $V_O$, and -OH atomic percentages from O1s spectra are29.2%, 41.3%, and 29.5% respectively; the ratio of In:Ga of IGO film is 30:1; (d) XRD pattern.

30cm²V⁻¹s⁻¹ at 2K, even higher than the room-temperature values of most amorphous oxide semiconductor (AOS) TFTs. Systematic investigations on the electrical transport behaviors of IGO-TFTs over a broad temperature range (2K ~ 300K) indicate that the near disorder-free nature of electron transport enables their ideal operation at 2K. Additionally, phenomena including bias stress instability and contact resistance at cryogenic temperatures were investigated. Negligible threshold voltage shifts were observed under both positive and negative bias stress tests, suggesting that low-temperature operation introduces no physical processes degrading device reliability. Contact resistance as low as several tens of Ω·cm was obtained at cryogenic temperatures, comparable to room-temperature.

## II. Device Fabrication and Characterization

Schematic IGO TFT shown in Fig. 1(a) and (b) are key fabrication steps. The process of IGO TFT on a heavily doped P$^{++}$ silicon substrate. A 10nm Mo BG electrode is DC-sputtered (Ar plasma, 3mTorr) and patterned via $SF_6/Cl_2$ based dry etching. Next, a 30nm $Al_2O_3$ gate dielectric is deposited by thermal ALD at 300°C (TMA). A dual-layer stack is then formed via sequential RF magnetron sputtering: first a 5nm $SiO_2$ interfacial optimization layer deposited at 120°C under pure Ar flow, followed by a 10nm IGO active layer sputtered at 50°C using an In:Ga = 9:1 alloy target with $O_2$/Ar gas ratios of 7.8/12sccm. S/D electrodes are formed by electron-beam evaporation of

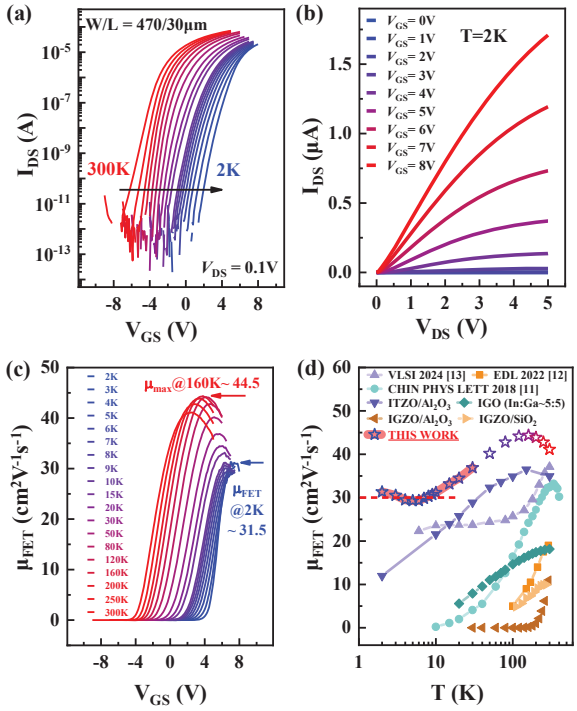


Fig. 2. (a) Transfer characteristics of IGO TFTs measured at various temperatures, from 300K to 2K; (b) Output characteristics of IGO TFTs measured at 2K with $V_{GS}$ from 0V to 8V, 1V per step; (c) The extracted temperature dependent $\mu_{FE}$ as a function of $V_{GS}$, showing a maximum $\mu_{FE}$ of 44.5 $cm^2V^{-1}s^{-1}$ and considerable $\mu_{FE}$ of 31.5$cm^2V^{-1}s^{-1}$ at 2K; (d) A comparative analysis of temperature dependent $\mu_{FE}$ between prior studies; this work reveals no distinct scaling trends in cryogenic regimes.

Ti/Au 10/30nm bilayers using lift-off lithography. The channel width ($W$) and length ($L$) were patterned to be 470 and 30μm ($W/L$= 470/30μm). 30nm thick ALD $Al_2O_3$ (200°C) encapsulation layer is deposited, with via openings etched by $H_3PO_4$ at 80°C to expose S/D and BG contacts.

The varying temperature electrical characteristic was carried out in Quantum Design PPMS DYNA COOL, connected to customized measuring instrument (FS-Pro, PRIMARIUS), after written the Hall device by using Al wire. The PBTI and NBTI were measured at $V_{GS}$=±9V, time interval 150s and 10 periods.

## III. Results and Discussion

Fig. 1(c) shows the XPS spectra for O1s, In3d, Ga2p, of the IGO film. The O1s spectra is deconvoluted into three components as indicated in the legend. Oxygen vacancy ($V_O$) concentration is of 41.3%; impurities–hydroxyl groups (-OH) and Metal-oxygen (M-O) are of similar concentration, 29.5% and 29.2%. The amorphous nature of IGO film was verified by X-ray diffraction, in Fig. 1(d).

### *A. Temperature dependent performance of IGO transistors*

Fig. 2(a) shows the temperature dependent transfer curves of IGO TFT. The output characteristics curves at 2K measured over different $V_{GS}$ (0 to 8V) shows in Fig. 2(b). Fig. 2(c) extracts the variation of $\mu_{FE}$ in a function of $V_{GS}$ at different temperatures It can be observed that as the temperature decreases, the $\mu_{FE}$ initially increases, then decreases, and finally increases below 5K, its maximum value of 44.5$cm^2V^{-1}s^{-1}$ is observed at 160K. The $\mu_{FE}$ is

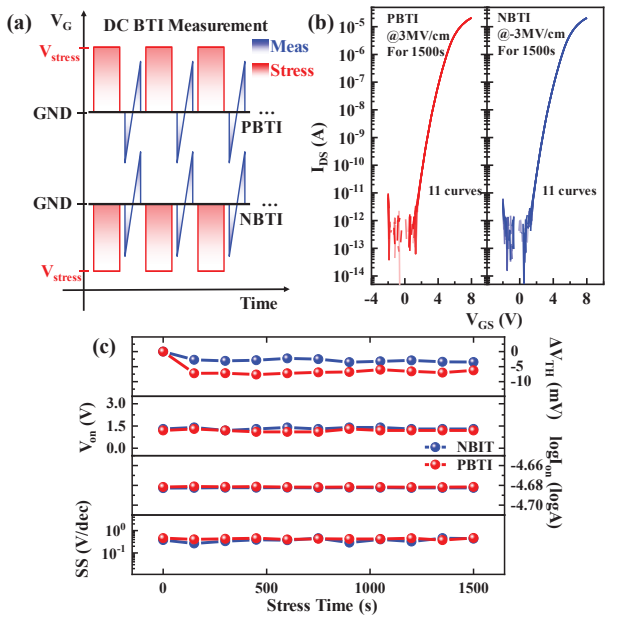


Fig. 3. (a) DC PBTI and NBTI measurement scheme adopted; (b) Measured PBTI and NBTI characteristics of IGO TFTs under $E_{stress}$ of ±3MV/cm, respectively, for 1500s at 2K; (c) The corresponding $\Delta V_{TH}$, $V_{on}$, $SS$ and $I_{on}$ as functions of stress time.

TABEL I. Benchmark for Stability in Cryogenic Tfts.

| | [15] | [12] | [13] | This work |
|---|---|---|---|---|
| $E_{Stress}$ (MV/cm) | 0.44 | N.A. | N.A. | **±3** |
| $\Delta V$th (V) | 2.2 for 1000s | N.A. | N.A. | **<-0.01 for 1500s** |
| Temp (K) | 77 | 100 | 6 | **2** |
| $\mu_{FET}$ ($cm^2V^{-1}s^{-1}$) | 3.75 | 5 | 22.5 | **31.5** |

observed to decrease by only 29% to 31.5$cm^2V^{-1}s^{-1}$ at $T$=2K. A comparative analysis of temperature-dependent mobility between this work and conventional IGZO-based devices included ever reported ones is shown in Fig. 2(d), demonstrating that the fabricated IGO TFT achieves the lowest reported variation amplitude with temperature [11-14]. Furthermore, an anomalous carrier mobility enhancement with decreasing temperature was observed within ultra-low temperature regime ($T$<5K), demonstrating a distinct inverse temperature dependence compared to conventional thermal activation transport mechanisms. This possibly relates to a metallic ground-state for the electrons gas in IGO-TFT.

### *B. PBTI and NBTI stability of devices at 2K*

Fig. 3(a) shows the BTI measurement scheme adopted in this study. Fast IV method is used to extract $V_{TH}$ to minimize recovery effect. $V_{TH}$ is calculated by fitting the linear equation $I_{DS}$~A($V_{GS}-V_{TH}$). Fig. 3(b) depicts the positive bias temperature instability (PBTI) and negative bias temperature instability (NBTI) tests results conducted on IGO TFT at 2K. The conditions for the PBTI and NBTI test were $V_{GS}$ = ±9V for 1500s. 11 curves at different stress times basically overlap. The results exhibit that a $\Delta V_{TH}$ of PBTI ~ -0.007V and NBTI ~ -0.003V, could be achieved down to 2K. The key parameters, $\Delta V_{TH}$, $V_{on}$, $SS$ and $I_{on}$, extracted from transfer characteristics vary with the

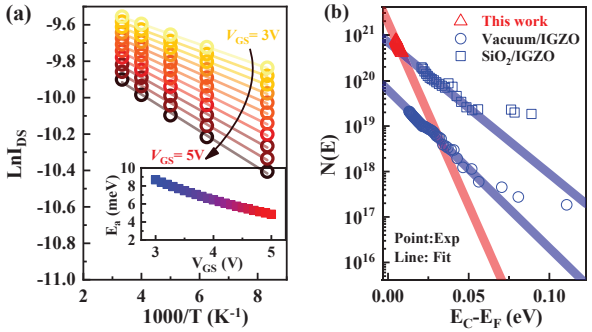


Fig. 4. (a) The extracted $I_{DS}$ (symbol) versus temperature at $V_{GS}$ = 3V to 5V fitting by Arrhenius relationship; Inset: the active energy $E_a$ in a function of $V_{GS}$; (b) Sub-gap DOS at $SiO_2$/IGO interfaces in this work compared with vacuum/IGZO and $SiO_2$/IGZO interfaces, extracted from the temperature-dependent $I_{DS}$-$V_{GS}$. The points are the experiments results, the solid lines are the fitting curves of the DOS.

TABEL II. FITTING PARAMETERS OF TAIL STATES.

| | Vacuum/IGZO | $SiO_2$/IGZO | This work |
|---|---|---|---|
| $N_{tail}$ (cm$^{-3}$) | 6.2×10$^{19}$ | 7×10$^{20}$ | **1.9×10$^{19}$** |
| $E_U$ (meV) | 12.5 | 15 | **5.4** |

duration of bias stress are plotted in Fig. 3(c) orderly [12, 13, 15]. The IGO TFT exhibited excellent electrical stress stability in both PB and NB modes.

Table Ⅰ. lists parameters related to cryogenic device stability from previous works for comparison with the results in this work. This study reports an exceptional bias stability under cryogenic conditions.

### C. *Quantitatively understanding temperature dependence carrier transport*

Fig. 4(a) displays the $V_{GS}$ dependent $I_{DS}$ as a function of temperature. It could be described by Arrhenius-type relationship $I_{DS}$~Aexp$(-E_a/k_BT)$, through which activation energy $E_a$ could also be extracted as a function of applied $V_{GS}$. In the inset of Fig. 4(a) $E_a$ varies from 8.5 to 5meV decreases with $V_{GS}$ increasing. The smaller value of $E_a$ corresponds to the smaller energetic distance for electrons' excitation from band tails to extended band ($E_C$) for transport. To be more quantitative, the density of states (DOS) of channel are evaluated based on the mobility edge framework. Based on our previous work, the extracted DOS of band tail states $N(E)$ below the $E_C$ is plotted in Fig. 4(b) with vacuum/IGZO and $SiO_2$/IGZO interface as comparisons. $N(E)$ was written as:

$$N(E) = \frac{C_i}{qa}\left(\frac{dE_a}{dV_{GS}}\right)^{-1} = N_{tail}\left(-\frac{E}{E_U}\right) \quad (1)$$

here a is the assumed effective thickness of IGO accumulation layer (10nm, here), $N_{tail}$ is the pre-exponential factor and $E_U$ is the Urbach energy. The fitting results are displayed in Table Ⅱ. It is found that the $SiO_2$/IGO interface has the least $N_{tail}$ of 1.9×10$^{19}$cm$^{-3}$among these three types of devices. Evidently, the $N(E)$ of $SiO_2$/IGO interface decays the most rapidly as the distance from $E_C$ increases as the minimum $E_U$ of 5.4meV less than $1k_BT$ at room temperature. This relates to a near disorder-free nature for charge transport, which possibly origins from the relatively low ratio of Gallium. Tabel Ⅱ. compares the

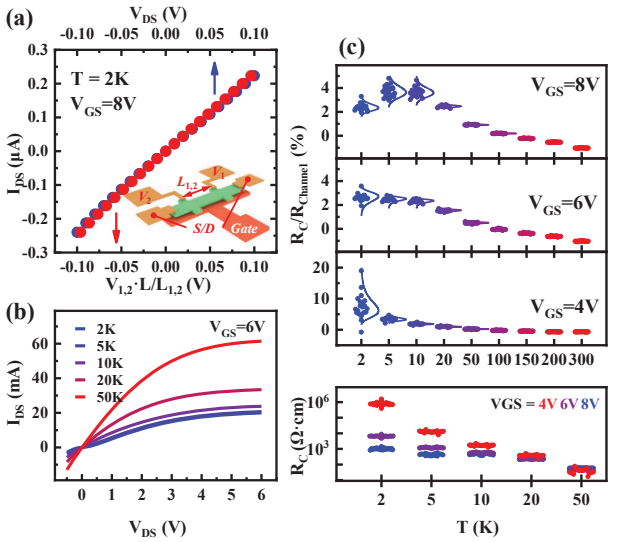


Fig. 5. (a) Extracting the contact resistance of an IGO TFT with $V_{GS}$ = 8V in on state at 2K using the four-probe method; (b) The trend of temperature variation in the output curve at 6K; (c) The extracted resistance ratio of $R_C/R_{channel}$ (%) and the normalization real $R_C$ in variation of temperature under different $V_{GS}$.

conditions of IGZO/$SiO_2$ and IGZO/vacuum interfaces with IGO/ $SiO_2$ one [10].

Besides, contact resistance should be excluded from the channel's intrinsic behavior at cryogenic temperatures via reasonable methods. Here, 4-probes methods is adopted to extract resist of channel and contact. Fig. 5(a) compared the on state partial voltage of channel with $V_{DS}$ at 2K, which is written as $V_{1,2} \cdot L/l_{1,2}$, where $V_{1,2}$ and $l_{1,2}$ are the voltage and distance difference between two inner probes, respectively, shows most of the $V_{DS}$ is applied on the channel. Fig. 5(b) demonstrates the variation trend of the output characteristics in the on-state ($V_{GS}$ = 6V) with temperature under cryogenic conditions. At 2K, the linear region of the output curve for a transistor in the on-state exhibits nonlinear trends within a small $V_{DS}$ range, primarily due to significant contact resistance. As the temperature rises up to 50K, the nonlinearity gradually diminishes. When entering the saturation region with pinch-off, the $I_{DS}$ also increases.

Fig. 5(c) illustrates the temperature dependence of $R_C$ under varying gate voltages. At elevated gate biases ($V_{GS}$ = 6V, 8V), the $R_C$ remains below 5% of the total resistance across the entire temperature range, confirming negligible contact resistance and well electron transport under high gate voltages. This observation validates the high $\mu_{FE}$ at cryogenic conditions in the device. Additionally, the extracted intrinsic $R_C$ under different operational states demonstrates a monotonic increase with decreasing temperature. This trend is attributed to the suppression of phonon activation at low temperatures, leading to suppression of the thermionic emission which contribute significantly to charge injections.

## IV. CONCLUSION

In summary, our cryogenic study of IGO TFT reveals exceptional performance at 2 K, including a high $\mu_{FE}$, a sharp $I_{on}/I_{off}$ ratio, and a positive $V_{TH}$. The anomalous mobility surge at 5K ~ 2K and ultralow $E_U$ enable efficient carrier excitation into the $E_C$. With a contact resistance of 1

kΩ·cm at 2 K, these results confirm IGO's superiority for cryogenic electronics, particularly advancing quantum computing and deep-space technologies demanding ultralow-temperature stability.

## ACKNOWLEDGMENT

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