Self-Selective Memristors for Real-Time Wireless Communication Encryption System with Ultra-low Bit Error Rate

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***Abstract*—We present self-selective memristors (SSMs) with a record rectification ratio (RR) exceeding 10^6, demonstrating excellent reliability and potential for ultra-large-scale integration. These devices are designed to address pressing security threats and challenges posed by data explosion. The Pt/HfO_2/WO_{3-x}/TiN SSMs exhibit high-efficiency, low-power read/write capabilities, and compatibility with CMOS technology, which are integral for in-memory computing. We showcase a 1-kb passive crossbar array achieving an ultra-low-bit error rate (BER) within a comprehensive wireless communication circuit equipped with radio-frequency (RF) modules for real-time communication encryption, highlighting the transformative potential of SSMs in enhancing data security and encryption methodologies.**

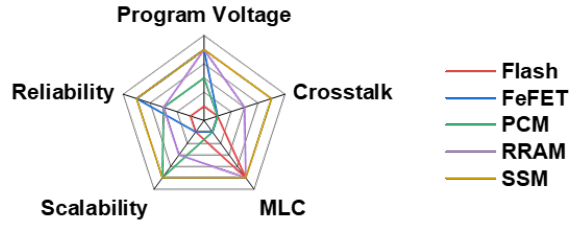
Keywords—self-selective memristor, reliability, large-scale, wireless communication, encryption

I. Introduction

In the big data era, the exponential growth of data has led to unprecedented information transparency, posing significant security threats to users' data worldwide [1, 2]. Wireless communication, which carries a substantial portion of users' daily information, has become particularly vulnerable to potential attacks due to the vast volume of data transmitted [3, 4]. Consequently, there is an urgent need to develop efficient in-memory computing solutions capable of real-time encryption across a wide range of wireless communications.

Memristors, with their unique electrical characteristics, such as adjustable non-volatility, low-power operation, and CMOS compatibility, have emerged as promising candidates for in-memory computing applications [5-7]. However, the presence of significant sneak path currents in large-scale memristor arrays can severely interfere with the precise read/write operations and cause inter-cell crosstalk [8]. While integrating additional circuit elements like transistors, diodes, or selectors can mitigate this issue, it often comes at the cost of increased area and power requirements, compromising the efficiency of future in-memory computing applications. SSMs offer a compelling solution by leveraging the high asymmetry of their intrinsic energy band structure to mitigate the leakage current in the ultra-large-scale crossbar array with critical self-selective function, further realizing an anti-crosstalk function within a single device [9-11].

In this work, we propose SSMs with an RR exceeding 10^6 to significantly suppress read errors in large passive arrays. Furthermore, we demonstrate a real-time wireless communication encryption system based on 1-kb crossbar SSM arrays and designed RF modules, achieving ultra-low BER near zero. Compared to Flash, FeFET, PCM, and conventional RRAM [12-14], our SSM exhibits breakthrough advantages in scalability, reliability, and multi-level cell (MLC) storage (Fig. 1).



	Program	Crosstalk	MLC	Scalability	Reliability
Flash	×	×	√	×	×
FeFET	√	×	×	×	√
PCM	-	×	×	√	-
RRAM	√	-	√	-	-
SSM	√	√	√	√	√

× : Bad - : Medium √ : Great

Fig. 1. Comparison of memory core characteristics between Flash, FeFET, PCM, regular RRAM and our SSM. Our SSM demonstrates the feasibility of ultra-large-scale integration and the great potential for high-precision and high-reliability in-memory computing.

II. Experiments

In this study, the thin films of SSMs were fabricated using the magnetron sputtering technique with the DISCOVERY-635 equipment. The sputtering targets employed included three-inch 99.99% pure Pt, TiN, WO_3, and HfO_2 targets. Thin film deposition was conducted on pre-patterned wafers. Initially, Pt films were deposited at a sputtering power of 200 W for 70 s. Subsequently, 10 nm HfO_2 and 40 nm WO_{3-x} thin films were deposited at sputtering powers of 100 W and 80 W, respectively, for durations of 300 s and 600 s, with an argon flux of 37 sccm and a chamber pressure maintained at 10 mtorr. Finally, TiN thin films were deposited at a sputtering power of 200 W for 240 s. After the magnetron sputtering process, the residual photoresist on the wafer was removed using acetone. For electrical characterization, a Keithley 4200-SCS semiconductor parameter analyzer was utilized. Transmission electron microscopy (TEM) images were acquired using either a Thermo Scientific Tecnai F20 TEM with an accelerating voltage of 200 kV or a Thermo Scientific Themis Z spherical aberration-corrected TEM.

III. Results and Discussion

RR and nonlinearity (NL) are the two most important figures of merit for SSMs and the most intuitive reflection of device performance RR is defined as the ratio of the response current of the device to the applied voltage (V) to the

response current generated by the applied bias at the two ends of the device the negative current region (not selected unit). Similarly, NL is defined as the ratio of the response current of the device to the applied voltage to the response current generated by the bias at the two ends of the device in the positive current region (partially selected unit) [8].

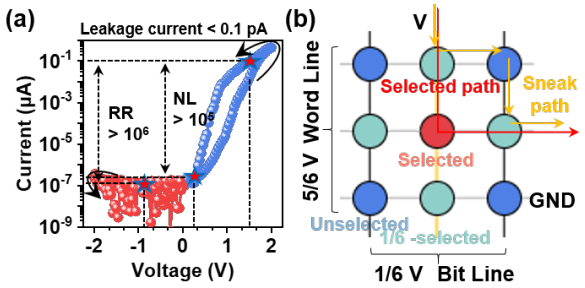


Fig. 2. (a) DC electrical characteristics I-V curves of the proposed SSMs. (b) The 1/6V scheme employed on the passive crossbar array. We used a 1/6V scheme with the operating voltage of 1.5 V to drive the SSMs in the array to achieve optimized rectification characteristics with ultra-low leakage current below 0.1 pA.

The direct-current (DC) electrical characteristics of the fabricated SSMs are shown in Fig. 2(a). We used a 1/6V scheme with an operating voltage of 1.5 V to drive the SSMs in the array, obtaining an extraordinarily large RR of over 10^6 and NL of over 10^5. Fig. 2(b) shows the 1/6V scheme as well as a schematic representation of the sneak path currents in a crossbar array. If the memristor cells are not rectified, the significant sneak paths can lead to severe inter-cell crosstalk which can disrupt the entire read circuit.

Fig. 3(a)~(c) illustrates the scanning electron microscope (SEM) image of the 32×32 crossbar array composed of the proposed SSMs, the schematic diagram of the electrical test wiring, and the TEM image of the SSM cells in the array, respectively. Fig. 3(d)~(e) illustrates the conductive mechanism in detail. Continuous conducting pathways formed by oxygen vacancies in the resistive layer WO_{3-x} dominate the Poole-Frenkel emission while the large potential barrier between the bottom electrode Pt and the insulating layer HfO_2 hinders the critical Schottky emission during the negative sweeping.

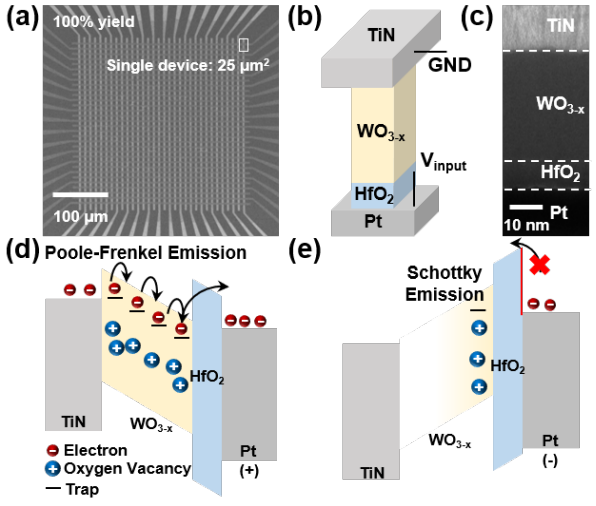


Fig. 3. (a) The SEM image of the 32×32 passive crossbar array with 100% yield based on the proposed SSMs as cells. (b) Schematic diagram of electrical test wiring. (c) The TEM image of the proposed SSMs. (d) Positive conductive mechanism of the SSM. (e) Negative Conducting Mechanism of the SSM.

Fig. 4 demonstrates the data retention and endurance characteristics of the proposed SSM at room temperature (RT) and 150 °C, confirming the superb reliability for frequent wireless communications. Fig. 5(a) displays the equivalent circuit diagram of the array shown in Fig. 3. The scalability of the proposed SSM was characterized using the "pull-up method" at RT and 150 °C. A 10% read margin corresponds to the upper limit of the scalable array size, which demonstrates the super-optimal scalability of the proposed SSM against high temperatures (Fig. 5(b)).

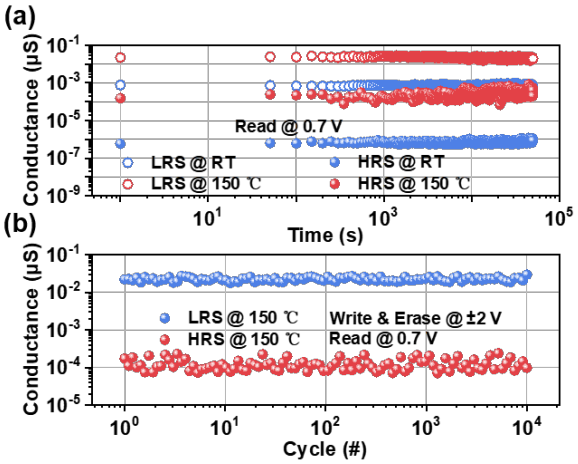


Fig. 4. Reliability characterization of the proposed SSM. (a) Data retention characteristics of the proposed SSM at RT and 150 °C. (b) Endurance characteristics of the proposed SSM at 150 °C. Both in terms of data retention and endurance, our devices demonstrate ultra-high temperature reliability.

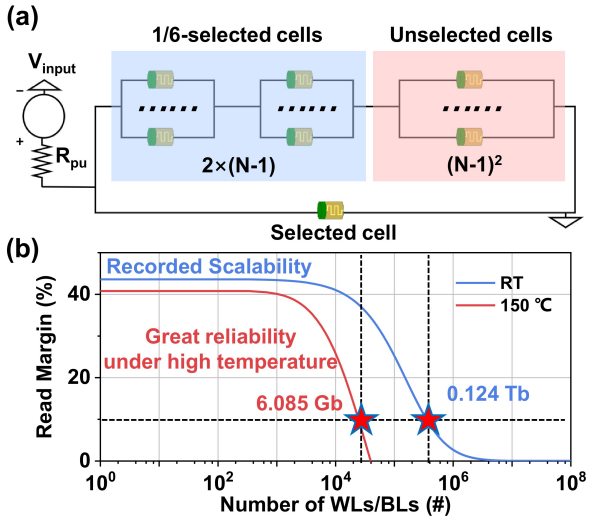


Fig. 5. (a) Equivalent circuit diagram of the "pull-up method" for the crossbar array shown in Fig. 1(b). The selected cells are connected in parallel with 2×(N-1) partially selected cells and $(N-1)^2$ unselected cells. (b) Scalability of the SSMs with the dimension of 25 μm² at RT and 150 °C. 10% read margin corresponds to the upper limit of scalable array size.

SSMs exhibit MLC features for recording 32 analog states (5 bits) with ultra-low device-to-device variations (1.9%) in the passive crossbar array, providing a solid foundation for high-precision in-memory computing (Fig. 6). The architecture of the real-time wireless communication encryption system based on the SSMs is shown schematically in Fig. 7, employing quadrature frequency division multiplexing (QFDM) and 16-quadrature amplitude modulation (16-QAM) to process and transmit the target signal. On the transmitter side, 32-word lines (WLs) correspond to 16 pairs of in-phase and quadrature

components, while 32-bit lines (BLs) periodically achieve an asynchronous output of the signal. The RF modules of the sender and receiver are responsible for signal transmission. The output signal fragments are then spliced into a complete string of encrypted data through the cooperation of a multiplexer (MUX) and a clock. The signal is encrypted to the ciphertext in real time by multiplication and accumulation (MAC) operations within the 1-kb crossbar array during the parallel processing. At the transmitting end, the RF module consists of a frequency modulator (FM), amplifier (AMP), and transmission antenna. Correspondingly, at the receiving end, the antenna receives the ciphertext signal, which is then pre-processed by a low noise amplifier (LNA), the FM, the second-order low-pass filter (LPF), and the variable gain amplifier (VGA). The signals are subsequently output through the MUX to the 1-kb crossbar array, where the final in-phase and quadrature signal components are reconstructed.

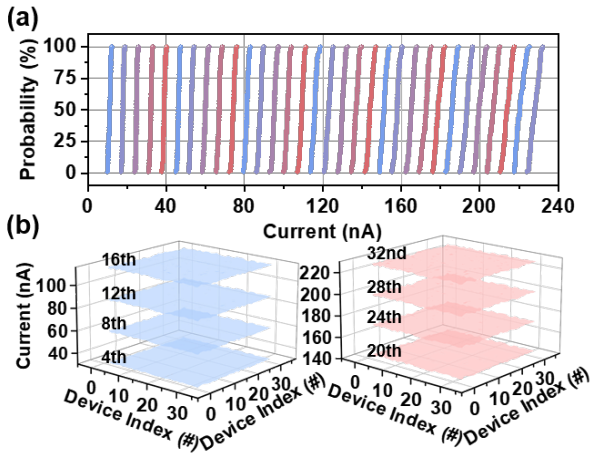


Fig. 6. (a) The 32 analog conductance states of the proposed SSM, corresponding to 5 bits, demonstrate the great potential of multilevel storage and further in-memory computing with high precision. The amplitude of the programming pulse is 2 V and the amplitude of the reading pulse is 1.5 V with the width of 700 ns. (b) Mapping of device-to-device variations for 8 sets of analog states as examples in a 32×32 passive crossbar array.

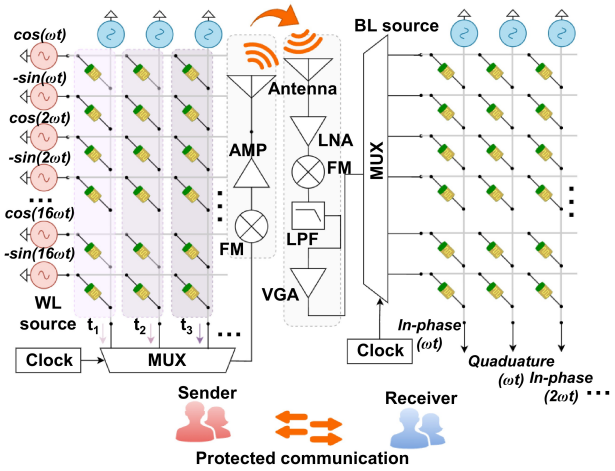


Fig. 7. Diagram of wireless communication circuit. Signal fragments are spliced by a MUX and a clock into encrypted data. The transmitter's RF module includes FM, AMP, and antenna. The receiver pre-processes the signal with LNA, FM, the second-order LPF, and the VGA.

Real-time encryption occurs via multiplication and addition computing (MAC) in the 1-kb crossbar array (Fig. 8). After discrete Fourier transform (DFT) on plaintext, parallel input was mapped into a random key from PUF generated by amplified random telegraph noise in the crossbar array for real-time matrix encryption. Consequently, the signals were output to the 1-kb crossbar array, where the final in-phase and quadrature signal components were reconstructed through decryption and inversed DFT. Fig. 9 shows the structural similarity index measurement (SSIM) variations of the sender's ciphertext as well as the receiver's plaintext with the original plaintext. After 10^7 cycles, the programmed stability of the circuits and crossbar arrays in the whole system remains very reliable. More intuitively, Fig. 10(a) illustrates the 16-QAM constellation diagram of the transmitted signal from the sender. 1024 sets of signal points are modulated onto 16 concentrated in-phase and quadrature coordinates. After wireless transmission and parallel processing through the receiver's crossbar array, the 16-QAM constellation diagram of the received signal is depicted in Fig. 10(b).

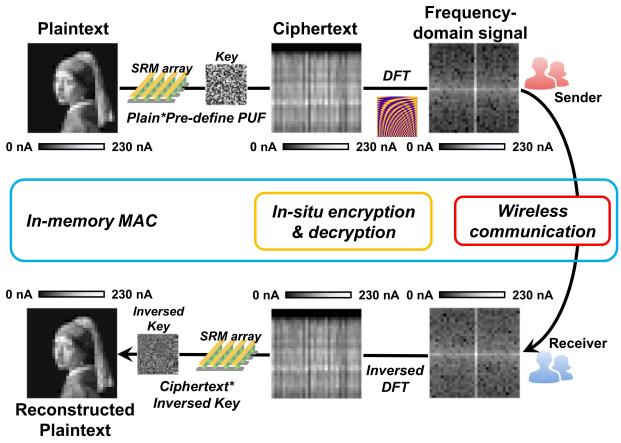


Fig. 8. The overall flow of real-time wireless encrypted communication. The programmed plaintext ("Girl with a pearl earring" 32×32-pixel image here) is encrypted in situ by the PUF stored in the SSM-based crossbar array after DFT. After receiving the ciphertext, the receiver reconstructs the plaintext by virtue of the crossbar array as well as the inversed PUF and inversed DFT.

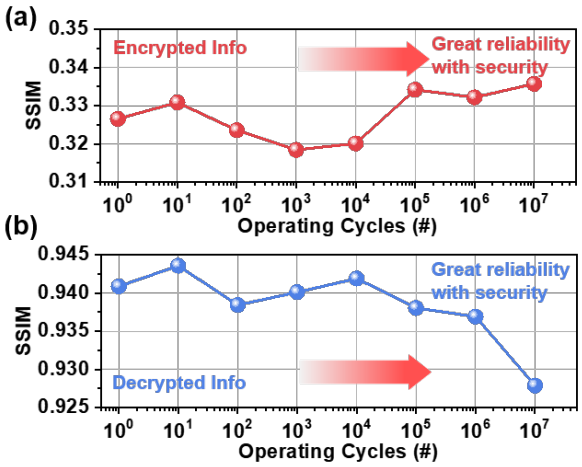


Fig. 9. The SSIM of the encrypted information at the sender and the decrypted information at the receiver with the original plaintext varies with the number of operation cycles. Obviously, after 10^7 cycles, the SSIM between the encrypted information and the original plaintext is still in the "irrelevant" region while the information at the receiver is still highly relevant to the original plaintext after wireless transmission and decryption.

All decrypted signals can be restored with an unprecedentedly remarkable BER of 0/1024. The signal constellation diagrams illustrated in Fig. 10 demonstrate the transmission and reception performance of the real-time communication encryption system across different stages. Fig. 10(a) displays the transmitted signals from the

transmitter array, exhibiting 16 well-defined constellation centers corresponding to the signal points, with a highly concentrated distribution pattern. The received signals in Fig. 10(b) show perfect recovery with 0 errors out of 1024 transmitted symbols. After 10^7 operational cycles, Fig. 10(c) presents the transmitted signals maintaining the same 16-point constellation structure. The corresponding received signals in Fig. 10(d) continue to demonstrate error-free performance (0/1024) despite the extended operation, confirming the system's stability and reliability. The consistent concentration of signal points around the constellation centers throughout all stages indicates excellent signal integrity preservation in both the encryption system and transmission channel [1].

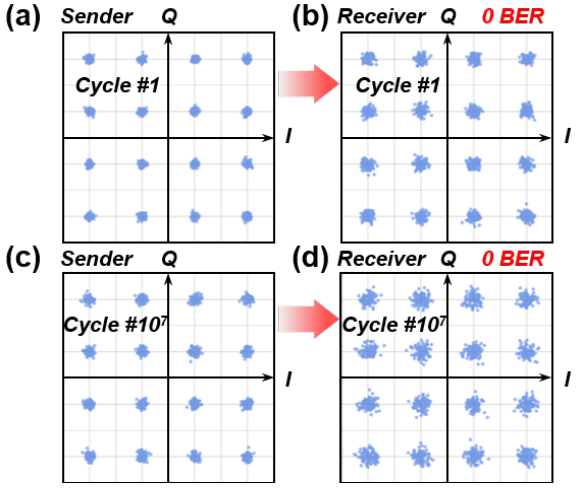


Fig. 10. The constellation diagram of signals (a) transmitted by the real-time communication encryption system, (b) received by the receive, (c) transmitted after 10^7 cycles, and (d) received after 10^7 cycles.

IV. Conclusion

We developed SSMs with a record-breaking RR exceeding 10^6 and NL exceeding 10^5 with exceptional MLC, reliability and scalability. The proposed SSM demonstrates state-of-the-art performance compared to previously SSMs and priority over 1T1R cells to improve the array scale and avoid unnecessary huge circuit overhead significantly (Table 1). The 1-kb passive crossbar array integrated into a real-time wireless communication encryption system achieved ultra-low BER near zero relying on the rich analog states of the proposed SSMs.

TABLE I. Comparison with state-of-the-art memory technology to mitigate sneak path current

	[15]	[16]	[17]	Our work
Cell	1T1R	SSM	SSM	SSM
Area efficiency (F^2)	108	4	4	4
RR/NL	-	>4.8×10²/>10³	>10⁴/>10⁴	>10⁶/>10⁵
Retention (s)	-	-	>3×10⁴ (125 ℃)	>3×10⁴ (150 ℃)
Endurance	-	>10⁵	>10⁶	>10⁴ (150 ℃)
Leakage current	-	<1 nA	<0.1 pA	<0.1 pA
MLC	1 bit	1 bit	1 bit	5 bits
Scalability	Bad	-	95 Mb	0.124 Tb
Native BER	10%	-	-	0
Security?	Yes	No	No	Yes

Acknowledgment

This work is supported by the National Natural Science Foundation of China (Grants No.62204219) and Major Program of Natural Science Foundation of Zhejiang Province (Grants No. LDT23F0401).

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