

A 56-Gb/s PAM-4 Injection-Locked CDR

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Abstract—This paper reports an injection-locked clock and data recovery (CDR) circuit achieving 56-Gb/s PAM-4 for the first time, aimed at improving the jitter tolerance (JTOL) and locking range. To generate injection pulses for high-speed PAM-4 signals, the oscillator’s output is used instead of the input data. To integrate this technique with a conventional phase locked loop (PLL)-based CDR including a bang-bang phase detector (BBPD), we activate the injection path only for large phase errors. This controlled self-injection into the LC oscillator allows the system to correct large phase errors with minimal disruption to the normal operation of the PLL-based loop, thus improving JTOL without affecting the jitter transfer (JTRAN). The added injection path improves the JTOL while employing two out of four phases of the quarter-rate clock for phase detection. Additionally, this injection path enhances the locking range of the CDR by counteracting cycle-slipping. Fabricated in a 28-nm bulk CMOS process, the proposed PAM-4 CDR achieves a JTOL value of 1-UI at 15 MHz, which represents a 50% improvement over existing solutions. The injection path contributes 65% to the JTOL improvement, while JTRAN remains unchanged with a bandwidth of 75 MHz. The measurements also indicate that enabling the injection path more than doubles the CDR’s locking range. The power consumption of the proposed CDR is 35.8 mW, with less than 8% contributed by the added injection path.

Keywords— Clock and data recovery (CDR), four level pulse-amplitude modulation (PAM-4), injection-locked CDR, jitter tolerance, locking range, self-injection.

I. INTRODUCTION

The primary objective of a clock and data recovery (CDR) system is to recover data with high fidelity in the presence of jitter. A common metric of success for these systems is jitter tolerance (JTOL). Conventional phase locked loop (PLL)-based CDRs use a feedback loop to align the recovered clock with the data. However, they often exhibit suboptimal JTOL due to their narrowband characteristics, even when bang-bang phase detectors (BBPDs) are used to enhance phase detector gain. In PAM-4 systems, JTOL is further compromised due to the difficulty in utilizing all transitions for phase detection, resulting in reduced phase detector gain [1]. Injection-locked CDRs offer a potential improvement in JTOL by instantaneously adjusting the recovered clock edges to align with the data. However, their application has been primarily limited to non-return-to-zero (NRZ) and low-speed applications [2], as they depend on data edges and limiting amplifiers for injection pulse generation. This complexity increases with PAM-4 signals, which feature varying transition types, amplitudes, and threshold level crossings. This paper introduces an approach for PAM-4 injection locking and integrates it into a conventional PLL-based CDR, targeting high-speed applications with improved JTOL and locking range.

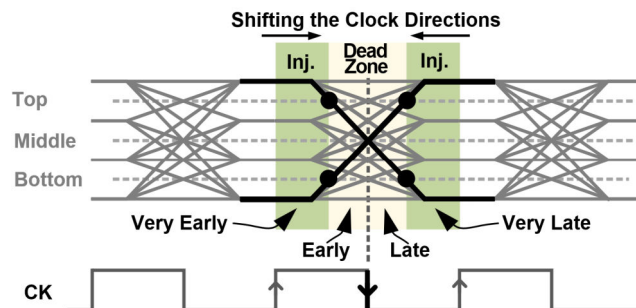


Fig. 1. Relation of the recovered clock and PAM-4 data transition midpoint.

II. PROPOSED INJECTION-LOCKED PAM-4 CDR

A. Basic Idea

As depicted in Fig. 1, the position of a recovered clock’s falling edge relative to the middle of a data transition can be classified into two categories: small phase errors (early/late) and large phase errors (very early/very late). When a PLL-based CDR functions correctly, the clock edge remains within the early/late area, indicating small phase errors. However, if the feedback loop fails to track the jitter present in the data, the clock edge shifts into the dark area, leading to erroneous data recovery and eventual loss of lock. We propose enhancing this loop by using controlled injections into the oscillator only when large phase errors occur, thereby avoiding constant disturbance of the oscillator. Since the injection into an oscillator pulls the clock edges toward the injected signal, by properly selecting the timing (phase difference) between the injection pulses and the oscillator, we aim to steer the clock edges into the injection dead-zone of Fig. 1. To address the issues associated with generating injection pulses directly from PAM-4 data with varying transitions, we propose generating the injection pulses from the oscillator itself. This approach is depicted in the conceptual injection-locked CDR diagram shown in Fig. 2. In this diagram, the PLL-based CDR operates similarly to conventional ones. It includes a phase detector (PD), a charge pump (CP), a loop filter (LPF), a voltage-controlled oscillator (VCO), a divider, and PAM-4 slicers. The injection pulses are derived from the clean, high-swing, and single threshold-crossing divided version of the VCO output, delayed by $\pm\Delta T$. The very early/very late (VEL) generator selects the appropriate phase for pulse generation to adjust the oscillator speed in the correct direction in response to large phase errors. By pulling the clock’s falling edge back into the small phase error region, this approach can achieve high JTOL and a wide locking range by reducing the error rate and preventing cycle-slipping.

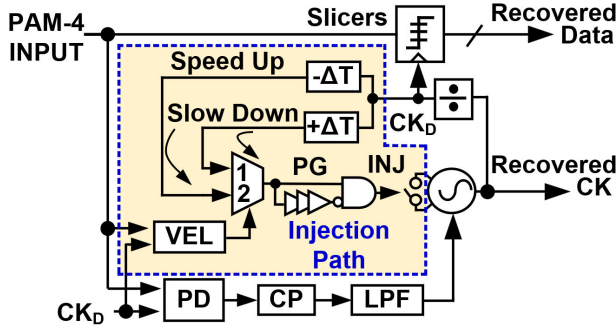


Fig. 2. Conceptual diagram of controlled self-injection into the oscillator to assist the PLL-based CDR in correcting large phase errors.

B. Controlled Self-Injection into the Oscillator

Injecting a pulse from the oscillator back into it at different points in the oscillation period can cause phase shifts and frequency changes in various directions as shown in Fig. 3. The maximum absolute frequency change occurs when the injection pulses are injected into the rising and falling edges of the oscillator output with positive or negative signs respectively. Conversely, the minimum frequency change and maximum amplitude change occur when they are injected at the peak and valley of the oscillator output. We choose to inject at the rising and falling edges for maximum injection strength and minimal amplitude change. Fig. 4 illustrates the operation principle of the proposed VEL generation for a rising major transition of the PAM-4 signal. By comparing the edge sample with the thresholds of the top and bottom eye slicers, large phase errors of very early and very late can be identified. For rising transitions, edge samples above +2 indicate very late clocks, while those below -2 indicate very early clocks. Conversely, for falling transitions, edge samples above +2 and below -2 indicate very early and very late clocks, respectively. Furthermore, the transitions from -3 to +3 and -1 to +3 cross +2 very close to each other. Therefore, in the proposed VEL generation block, we utilized the transitions (-3, -1 to +3) and (+3, +1 to -3) for VL, and (-3 to +1, +3) and (+3 to -1, -3) for VE generation.

III. ARCHITECTURE AND IMPLEMENTATION

Fig. 5 presents the architecture of the proposed quarter-rate CDR, with injection path blocks highlighted. It includes a class-AB LC voltage-controlled oscillator (VCO) with single-ended injection, a two-stage ring divider, a loop filter, and two paths for data recovery and phase detection. Six slicers in total are employed (four for data and two for edge) for phase detection [4]. The slicers include sample-and-hold circuits, CML buffers, and Strong-Arm latches. The outputs of the data slicers are converted to binary recovered data by the thermometer-to-binary converter (T2B) blocks. The charge pump outputs connect to the loop filter, and the early/late generator performs conventional BBPD phase detection [5]. The outputs of the VEL generator of the two paths are combined and retimed by the VEL combiner block. An injection number multiplier is added to enable the injection between 0 and 14 pulses per VEL detection into the oscillator. This allows the adjustment of the average injection strength for VE and VL, controlling their relative strengths, or deactivating the injection path. This block includes two 4-bit writable counters, one for VE and one for VL, which are clocked by the quarter-rate clock (7 GHz) and triggered by

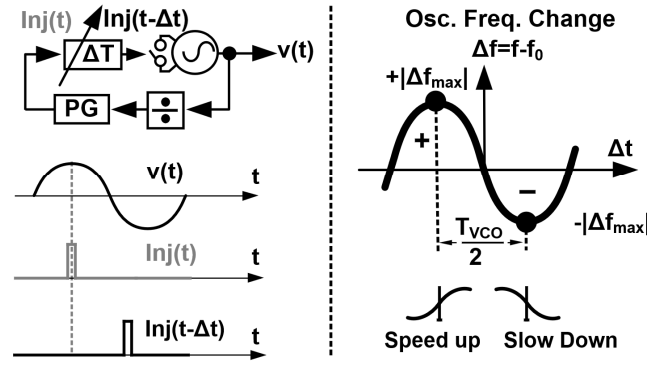


Fig. 3. By adjusting the delay between the injection pulses and the oscillator, the frequency and phase of the oscillator can be modified.

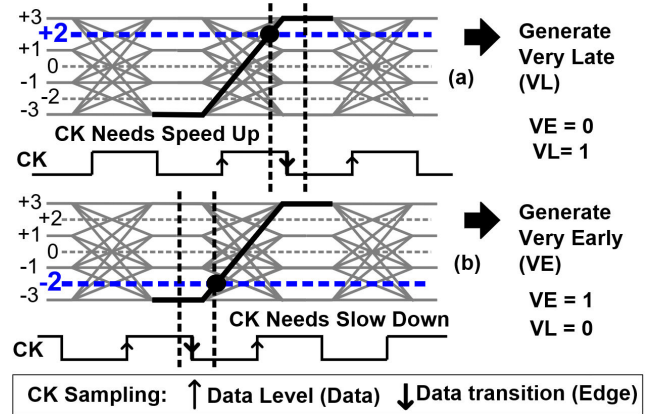


Fig. 4. Comparing edge samples with top and bottom eye thresholds identifies (a) very late and (b) very early regions. The notation for PAM-4 levels is similar to that in [3].

VE or VL, respectively. Given the high-speed requirements, the injection number multiplier block is implemented using linear feedback shift register (LFSR)-based counters and true single-phase clock (TSPC) flip-flops.

The highest injection strength, with minimal amplitude disturbance, is achieved when pulses are injected at the rising or falling zero-crossings of the oscillator's output, which are half a period apart (Fig. 3). We select between CK0 and CK45 of the divider to naturally meet this requirement. By controlling the delay with the voltage-controlled delay line (VCDL), the injection pulses are applied at the rising or falling zero-crossings of the oscillator, according to VL or VE detection. The VCDL is implemented using a varactor-based delay line. Varactors are sized to ensure more than 1-UI delay is covered in all corners. The pulse generator (PG) block creates the injection pulses from the output of the VCDL, the delayed version of the selected clock (CK0 or CK45). The width of the injection pulse is tunable using a four-bit switch capacitor-based digitally controlled delay line (DCDL).

To ensure the alignment of the injection pulse and oscillator output despite process, voltage, and temperature (PVT) variations, we incorporated a background delay locked loop (DLL)-based calibration into the injection path. The oscillator's output, sampled by two types of injection pulses, INJ_E and INJ_L , is subtracted and amplified in the DLL loop to guide them to converge at the oscillator's zero crossings. Matching between these sampling pulses and the injected pulse (INJ) into the oscillator is carefully ensured. Series resistors are added to prevent degrading the VCO

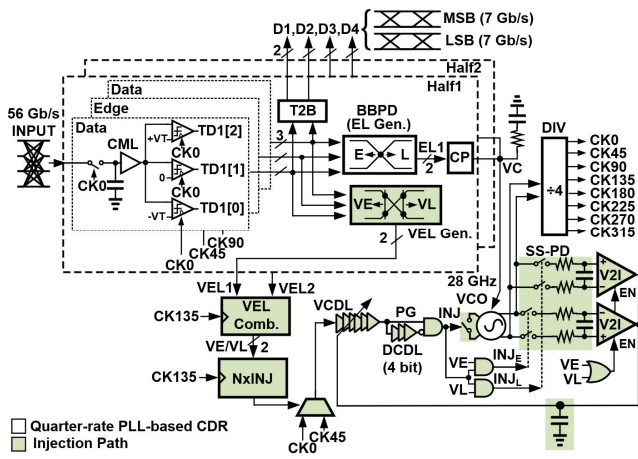


Fig. 5. The architecture of the proposed injection-locked CDR.

tank's quality factor. It is noteworthy that unlike the implementation of such a PVT tracking loop for PLLs [6], INJ itself cannot be used for sampling the VCO output. In that case, samples taken with opposite signs would add together and cancel each other out.

IV. MEASUREMENT RESULTS

This CDR is fabricated in a 28-nm CMOS technology, with the wire-bonded die photo shown in Fig. 6(a). The chip is tested with a Keysight M8040A bit error rate tester (BERT) and a Rohde & Schwarz spectrum analyzer FSW67. The measured VCO frequency change due to self-injection is depicted in Fig. 6(b). For this measurement, we opened the DLL loop and connected the VCDL control voltage to an on-chip R2R DAC, sweeping its control voltage. The input data rate was set outside the VCO frequency band to ensure VEL generation while avoiding locking. In addition, only the VE signal was activated. The result shows that the frequency of the VCO can be changed by ± 160 MHz. We chose the VCDL gain large enough to ensure that the maximum

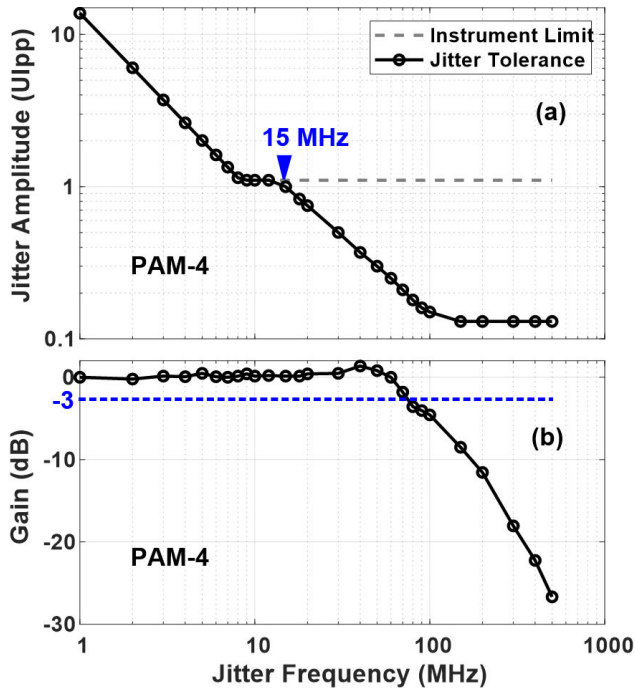


Fig. 7. Measured (a) JTOL and (b) JTRAN for 56 Gb/s PAM-4 input.

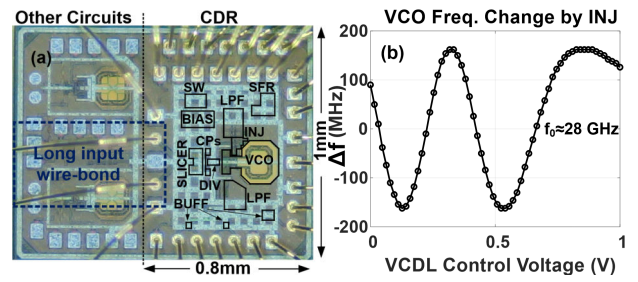


Fig. 6. (a) Die photo and (b) measured VCO frequency change by self-injection.

increase and decrease of the VCO frequency change through injection is covered. Therefore, only one cycle of that sinusoidal-like curve is sufficient for our injection path calibration. The nonlinearity of the curve at high values of the VCDL control voltage is not problematic, though it can be avoided by initializing the loop to settle in the first half of

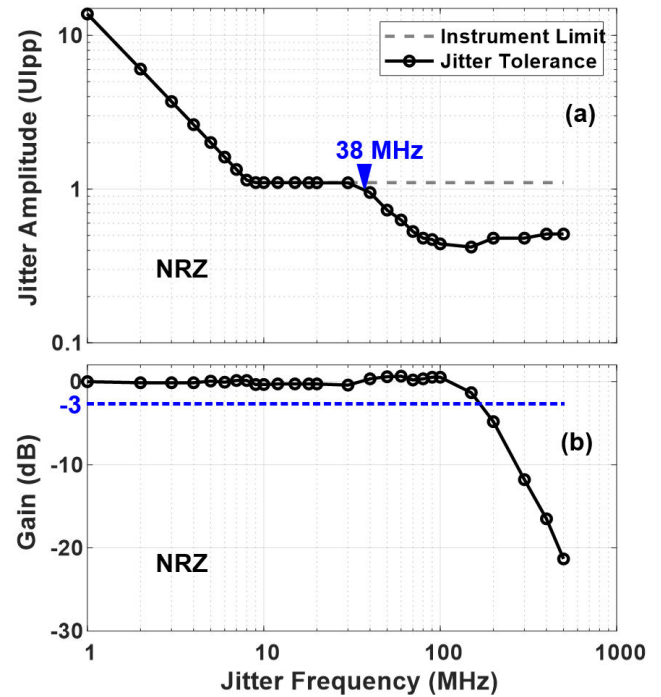


Fig. 8. Measured (a) JTOL and (b) JTRAN for 28 Gb/s NRZ input.

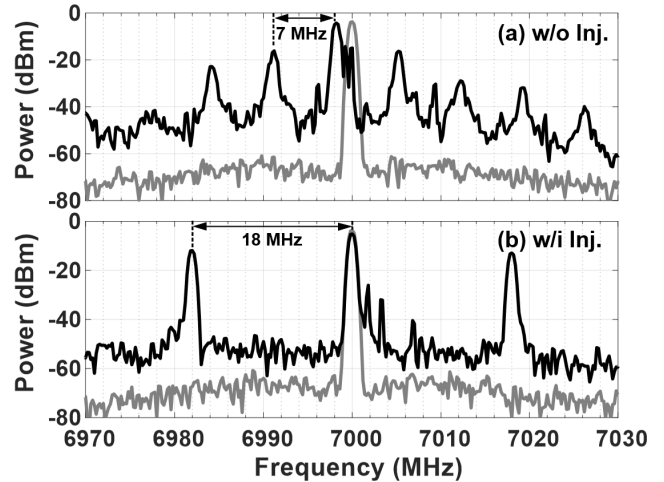


Fig. 9. Measured Locking range (a) without (b) with injection.

TABLE I. PERFORMANCE SUMMARY AND COMPARISON WITH PRIOR ART

	[2] JSSC'19	[8] JSSC'18	[1] JSSC'22	[5] JSSC'22	[4] JSSC'20	[3] JSSC'24	[7] JSSC'24	This work	
Architecture	Injection-locked	PLL-based	PLL-based	PLL-based	PLL-based	PLL-based	PLL-based	Injection-locked	
PD Type	BB	BB	Analog	BB	Linear	BB-baud	BB	BB	
Technology (nm)	28	40	28	28	40	28	40	28	
Data Format	NRZ	NRZ	PAM-4	PAM-4	PAM-4	PAM-4	PAM-4	PAM-4	NRZ
Data Rate (Gb/s)	10	12.5-25	56	28	32	52	60	56	28
1UI JTOL (MHz)	31	4	10	1.8	3	1.5	8	15	38
Power (mW)	12.8	46	8	19.2	14.7	43	70	35.8	35.8
Power Efficiency (pJ/bit)	1.28	1.8	0.14	0.68	0.46	0.83	1.18	0.64	1.28

the curve. The measurement results for JTOL and JTRAN of the proposed CDR are shown in Fig. 7 and Fig. 8. The measurements are for 10^{-12} BER and PRBS-7. The 1-UI JTOL of the proposed architecture, which is emphasized in the literature, is 15 MHz for PAM-4, 1.5 times higher than that of the state-of-the-art. This is achieved while using only two out of four clock phases (CK45 and CK225) for edge information extraction. Furthermore, the PD of [5] that was adopted is more suitable for low bandwidth loops with low JTOL. The jitter transfer is not affected by the injection as it is activated only when the PLL loop cannot correct the phase errors. Therefore, the 3-dB bandwidth (BW) of jitter transfer remains around 75 MHz (Fig. 7(b)). Shown in Fig. 8, the 1-UI JTOL for NRZ input to the proposed CDR is 38 MHz for the data rate of 28 Gb/s, which compares favorably in terms of both JTOL and speed with state-of-the-art injection-locking-based NRZ CDRs. We also measured the effect of the added injection path on the locking range of the proposed CDR. In our measurements, we added a sinusoidal jitter with an amplitude of 1-UI peak-to-peak to the input 56-Gb/s PAM-4 data and observed the recovered clock on the spectrum analyzer. This measurement is for a 25 MHz BW, with the most complete set of data, while improvements are observed across the board. As shown in Fig. 9, without injection, the CDR loses lock when the input frequency is modulated by 7 MHz, and the spectrum shows a false lock. However, when the injection is activated, it loses lock at 18 MHz, showing more than a two-time improvement. When no sinusoidal jitter is added, both conditions exhibit the same spectrum as the PLL loop functions correctly, and the clock edge stays in the injection dead-zone.

The power consumption of the proposed CDR is 35.8 mW, distributed as follows: 46% for the data path, 32% for the divider, 11% for the VCO, 8% for the injection path, and 2% for the charge pump. It should be noted that the reported power consumption for the injection path is for the worst-case scenario when the injection multipliers are set to 14. The recovered 7 GHz clock jitter, integrated from 1 kHz to 3 GHz, is 985 fs_{rms} for PAM-4 and 772 fs_{rms} for NRZ. In another measurement for PAM-4, with the loop bandwidth set to 45 MHz, the integrated jitter was 662 fs_{rms} and the 1-UI JTOL achieved was 10 MHz. It is noteworthy that the contribution of the injection path to the JTOL improvement is around 65% for PAM-4 and 90% for NRZ, respectively. Tables I compare this CDR with the state-of-the-art. This work, with acceptable power efficiency, improves the JTOL for both PAM-4 and NRZ.

V. CONCLUSION

We present a high-speed PAM-4 injection-locked CDR implemented in a 28-nm CMOS technology for the first time. This design targets high-speed applications while achieving improved JTOL and locking range, with the injection path contributing less than 8% power overhead at worst.

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