

A 94% Peak Efficiency Class-E Power Amplifier with Auto-Aligned Current Phase for Guaranteed ZVS under Impedance Variations

Yingming Liu^{*†}, Wing-Hung Ki[†], Chi-Ying Tsui[†], and Yuan Gao^{*}

Email: yliukb@connect.ust.hk gaoy@sustech.edu.cn

^{*}School of Microelectronics, Southern University of Science and Technology, Shenzhen, China

[†]Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong, China

Abstract—A 6.78 MHz load-independent Class-E power amplifier (PA) with auto-aligned current phase for wireless charging is proposed. It can adapt to rapid changes in real impedance and resolve mismatches in imaginary impedance. Consequently, this Class-E PA maintains zero-voltage switching (ZVS) for all switches and achieves efficient power transfer even during load transients and when driving reconfigurable resonant regulating rectifiers. The wireless power transfer (WPT) system delivers a maximum output power of 37.8 W, with peak transmitter efficiency of 94% and peak end-to-end (E2E) efficiency of 86.3%.

Keywords—Class-E power amplifier (PA), wireless charging, zero-voltage switching (ZVS), load-independent

I. INTRODUCTION

The demand for compact high-power wireless power transfer (WPT) systems is rapidly increasing, driven by the need for fast wireless charging of consumer electronics. Compared to Class-D power amplifiers (PAs), Class-E PAs can handle higher power with better efficiency, making them ideal for mid- to high-power applications. Class-E PAs are designed to operate with zero-voltage switching (ZVS) to minimize turn-on switching losses, but ZVS is difficult to maintain due to varying loads, as shown in Fig. 1. Fluctuations in the real impedance $Re(Z)$ (caused by changes in the coupling coefficient k or load resistance R_L), and shifts in the imaginary impedance $Im(Z)$ (resulted from mismatches between the switching frequency f_s and resonant frequencies of the LC tanks of the transmitter (Tx) and the receiver (Rx)), can distort the output voltage waveform of the Class-E PA, thus compromising ZVS operation and degrading efficiency by having hard-switching (HS) loss and body-diode conduction (BDC) loss, as shown in Fig. 1(b).

Load-independent ZVS approaches for Class-E inverters have been proposed [1, 2] to deal with variations in $Re(Z)$, which rely on the precise calculation of circuit parameters. However, they are unable to deal with shifts in $Im(Z)$ that could cause significant waveform distortion, and any resonance mismatch could cause significant waveform distortion.

A simple ZVS scheme is presented in [3], in which the main power switch is activated only when a zero-voltage condition is detected. However, this method forces the load to operate in the inductive region, which increases the voltage stress on the switch and requires the Rx resonant frequency to deviate from

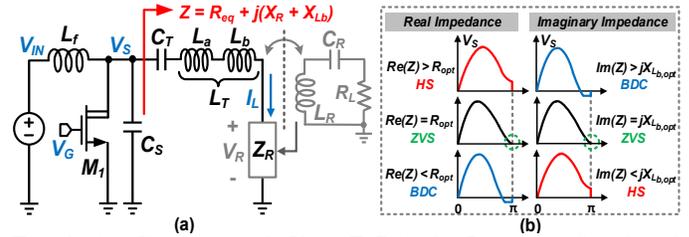


Fig. 1. (a) Conventional Class-E PA; (b) Impacts of real and imaginary impedance variations.

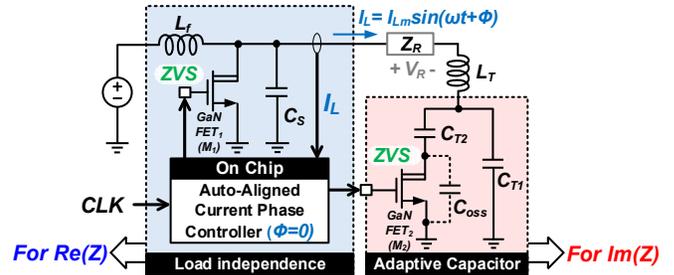


Fig. 2. Overall system implementation of the proposed PA.

f_s , reducing the link efficiency. Another method is to tune the output capacitance C_{oss} of a discrete FET via closed-loop bias voltage adjustment to compensate for $Im(Z)$ [4, 5], but this technique cannot handle changes in $Re(Z)$.

A new solution is proposed to address variations in both $Re(Z)$ and $Im(Z)$ [6], by using an imaginary-part phase compensation (IPC) controller for $Im(Z)$ and a real-part impedance matching (RIM) network to optimize $Re(Z)$. However, the IPC requires an on-chip 200V power switch array, and the RIM needs an additional capacitor and inductor. Additionally, all three methods described above rely on detecting the high-voltage switching node V_S in each cycle to calibrate for ZVS, and an expensive SOI process is needed to implement the control chip.

To address these issues, we propose an auto-aligned current phase control scheme with an adaptive capacitor structure to realize a load-independent Class-E PA with ZVS on all switches, as shown in Fig.2. This design automatically adapts to rapid changes in $Re(Z)$ while compensating for mismatches in $Im(Z)$, ensuring ZVS even during abrupt load transients.

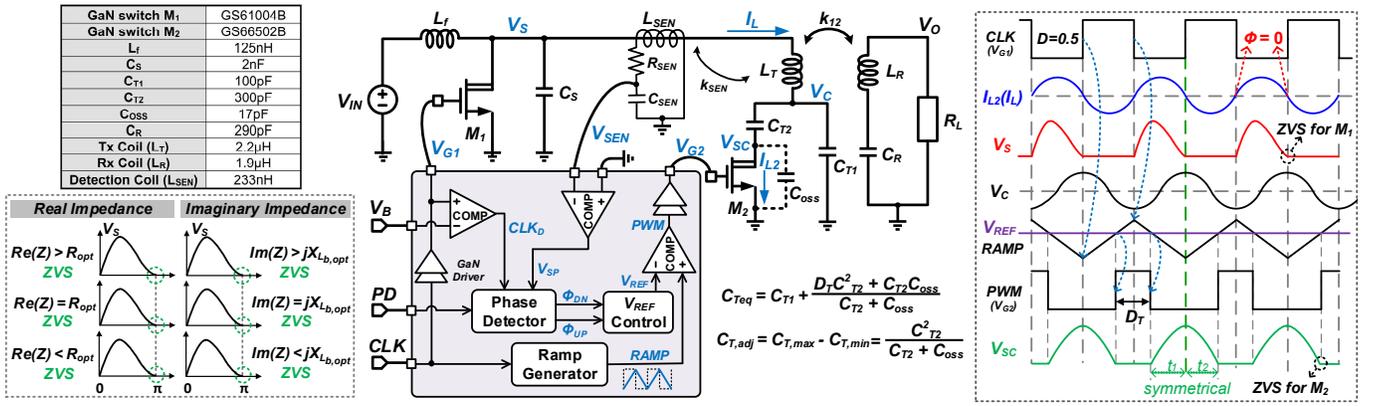


Fig. 3. Proposed load-independent class-E PA with auto-aligned loop, and waveform alignment principle for ZVS of M₁ and M₂.

II. PROPOSED CLASS-E PA WITH AUTO-ALIGNED LOOP

The proposed Class-E PA is shown in Fig.3. All switches can operate under ZVS conditions in the steady state, regardless of variations in the real and imaginary impedance.

A. Analysis of Impedance Requirements

As shown in Fig. 1(a), the Tx coil inductance L_T can be divided into L_a and L_b , where L_a resonates with C_T at the switching frequency f_s , and L_b introduces a phase shift to the output current I_L . The current I_L is given by

$$I_L = I_{Lm} \sin(\omega t + \phi) \quad (1)$$

where I_{Lm} and ϕ are the amplitude and initial phase of I_L , respectively. The entire series-resonant secondary circuit can be modeled as an equivalent impedance Z_R . Thus, the impedance Z of the combination of the equivalent Rx and Tx LC tank is

$$Z = Z_R + Z_T = (R_{eq} + jX_R) + (jX_{L_b} + j\omega L_a + \frac{1}{j\omega C_T}) \quad (2)$$

Here, $\omega_{resT} = 1/\sqrt{L_a C_T}$ and $\omega_{resR} = 1/\sqrt{L_R C_R}$ are the resonant frequencies of the Tx and Rx LC tanks, respectively. To simultaneously achieve ZVS and zero-voltage derivative-switching (ZVDS), conventional Class-E PA requires perfect alignment at all frequencies, with both the real and imaginary impedances being fixed values, so (2) can be simplified as

$$Z_{opt} = R_{opt} + jX_{L_b,opt} @ \omega = 2\pi f_s = \omega_{resT} = \omega_{resR} \quad (3)$$

which means that once $Re(Z)$ or $Im(Z)$ deviate from the optimal values, HD loss and BDC loss may arise, as shown in Fig. 1(b).

B. Deal with Real Impedance Variations

To maintain ZVS of M₁ when the real impedance changes, we utilize the load-independent principle of the Class-E inverter to design the circuit, making the Class-E PA insensitive to $Re(Z)$, as shown in Fig. 2. Because ZVDS has much less effect on efficiency than ZVS, the load-independent condition for Class-E PA, discussed in [2], replaces ZVDS condition with

$$\frac{dV_{Rm}}{dI_{Lm}} = 0 \quad (4)$$

where V_{Rm} is the amplitude voltage V_R across Z_R . This ensures a constant output voltage despite variations in R_{eq} . To satisfy both ZVS and load independence in (4), $q = 1.29$ and $\phi = 0$ are

derived uniquely when the duty ratio of M₁ is 0.5 [2], with $q = 1/\omega\sqrt{L_f C_s}$, which is not affected by impedance, while the current phase ϕ is affected by the imaginary impedance $Im(Z)$.

C. Deal with Imaginary Impedance Shifts

The condition for maintaining $\phi = 0$ to achieve ZVS of M₁ requires that $Im(Z) = jX_{L_b}$ under perfect resonance alignment. An auto-aligned circuit consists of two capacitors C_{T1} , C_{T2} and a switch M₂ is designed to compensate $Im(Z)$ by adjusting the equivalent resonance capacitance C_{Teq} , ensuring that the current phase ϕ of I_L is always equal to 0, as shown in Fig. 2.

$$C_{Teq} = C_{T1} + \frac{C_{T2}(D_T C_{T2} + C_{oss})}{C_{T2} + C_{oss}} \quad (5)$$

where C_{oss} and D_T are the parasitic output capacitance and the duty ratio of the GaN FET M₂.

D. Switching Strategy for ZVS of M₂

To maintain high system efficiency, both M₁ and M₂ should operate under ZVS conditions, with M₂ serving as the switch in the auto-aligned loop. After M₂ is switched off, its drain voltage V_{SC} resonates with L_{L2} that is in phase with I_L . ZVS for M₂ is guaranteed if the PWM pulse is symmetrical around the zero-crossing points of I_{L2} , such that the energy charged to C_{oss} by I_{L2} during t_1 and discharged during t_2 is balanced.

When M₁ operates normally in ZVS and load-independent conditions, the phase difference ϕ between I_L and CLK is 0. Thus, by generating a RAMP signal that is symmetrical around the edges of CLK and comparing it with the reference voltage V_{REF} to produce a PWM pulse, the PWM pulse will be symmetrical about the zero-crossing point of I_L , allowing M₂ and M₁ to operate together in ZVS mode, as shown in Fig. 3.

E. Circuit Implementation

Unlike previous ZVS implementations that rely on V_s detection-based feedback or require precise circuit parameters, we propose an auto-aligned load-independent Class-E PA that detects and adaptively adjusts the initial phase ϕ of I_L . First, I_L is sensed by a detection coil L_{SEN} (a small coil fabricated on the back of the Tx coil) and converted to a sensing voltage V_{SEN} in phase with I_L . Next, the phase difference between the zero-crossing point of V_{SEN} and the switching edges of CLK_D

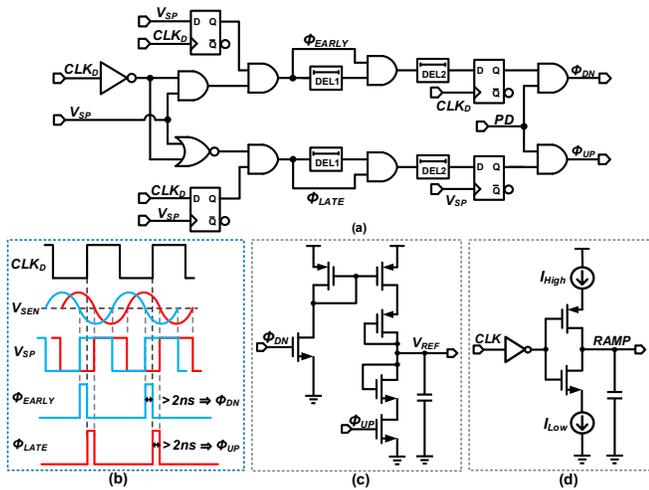


Fig. 4. (a) Phase detector circuit (b) the operating conditions for Φ_{DN} or Φ_{UP} (c) reference voltage controller (d) ramp generator.

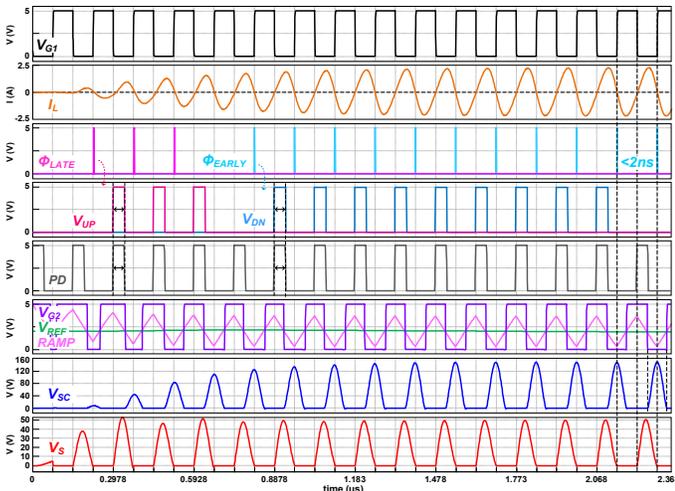


Fig. 5. Simulated waveforms during startup.

(CLK after delay compensation) is detected, which is used to adjust V_{REF} to generate the control signal PWM with the duty ratio D_T . Finally, the switch M_2 adjusts the equivalent capacitance C_{Teq} according to D_T , enabling the precise closed-loop control of the current phase ϕ , as shown in Fig. 3.

Fig. 4 shows the phase detector that generates trigger signals Φ_{DN} and Φ_{UP} based on the phase difference. A rectangular wave V_{SP} is produced when V_{SEN} crosses zero, and the phase difference between CLK_D and V_{SP} is extracted. If V_{SP} leads CLK_D , a Φ_{EARLY} pulse is generated; otherwise, a Φ_{LATE} pulse is generated. The circuit evaluates the phase difference and generates Φ_{DN} or Φ_{UP} only when the width of Φ_{EARLY} or Φ_{LATE} exceeds 2 ns, thus adjusting V_{REF} . The width and frequency of Φ_{DN}/Φ_{UP} are determined by the external pulse signal PD , and by controlling PD , the adjustment precision of V_{REF} can be modified, further adjusting the PWM . Consequently, the Class-E PA operates robustly under load-independent conditions, allowing all switches to operate under ZVS state despite variations in real and imaginary impedance. Fig. 5 shows the PA's simulated regulation process during startup.

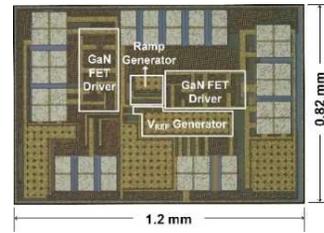


Fig. 6. Chip micrograph.

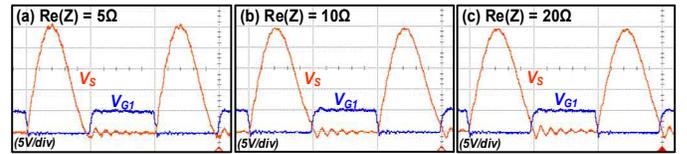


Fig. 7. Measured waveforms with different real impedances.

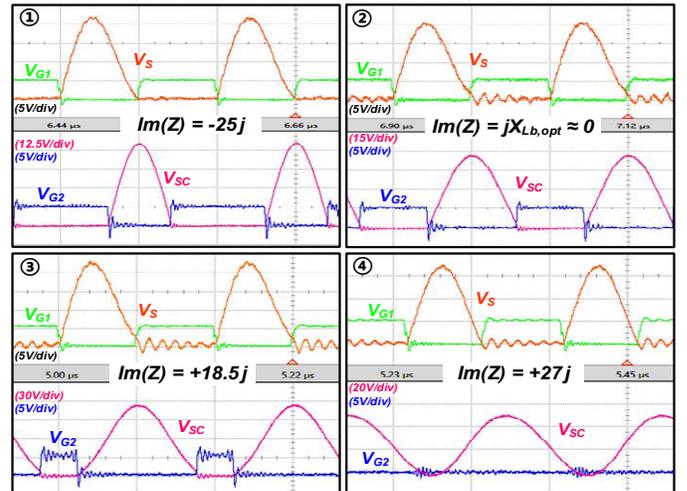


Fig. 8. Measured waveforms with imaginary impedance shifts.

III. MEASUREMENT RESULTS

The proposed PA controller chip was fabricated in a $0.18 \mu\text{m}$ BCD process. Fig. 6 shows the chip micrograph with a die area of 0.984 mm^2 . Fig. 7 shows the waveforms of the switching node V_S when the PA was driving different resistances, proving its load independence characteristic. Fig. 8 shows the adaptive regulation capability of the PA in the presence of imaginary impedance mismatches.

To further validate the functionality of the proposed Class-E PA, the WPT transmitter is used to drive a simplified receiver with a 2-mode rectifier (Fig. 9). By turning on and off the signal V_{RG} , the rectifier switches between full-bridge rectification (IX) and short-circuit operation (OX). This variation of the equivalent load $R_{L_{ac}}$ causes periodic changes in the equivalent load R_{eq} at the Tx side. The measured waveforms presented in Fig. 9 demonstrate that, even under rapid load variations, the proposed Class-E PA, based on the load-independent principle, can operate in the ZVS condition during both transient and steady-state conditions, with a regulation time of less than $2 \mu\text{s}$. It can work in coordination with the Rx with a reconfigurable resonant regulating rectifier in [7, 8].

Fig. 10 shows the measured transmitter and E2E system efficiency with different loads, achieving peak Tx efficiency of

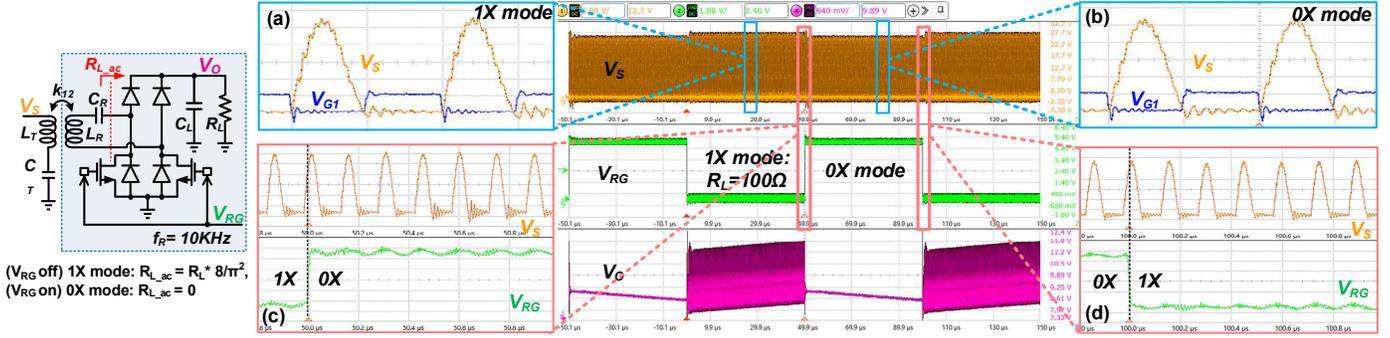


Fig. 9. The receiver with 1X/0X reconfigurable rectifier and measured waveforms during load transient response.

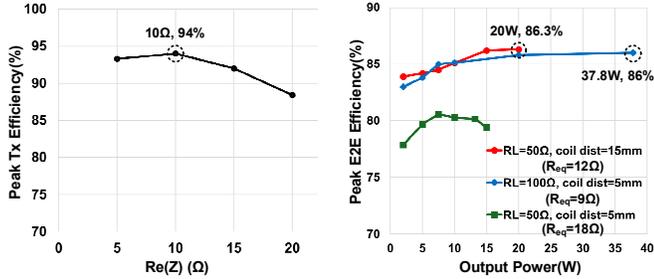


Fig. 10. Measured Tx and E2E efficiency of the proposed Class-E PA.

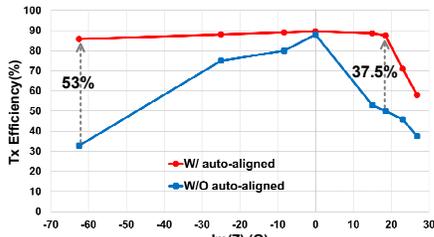


Fig. 11. Measured E2E efficiency subject to $Im(Z)$ mismatches.

TABLE I: COMPARISON WITH STATE-OF-THE-ART DESIGNS

	ISSCC'18[4]	ISSCC'19[5]	ISSCC'24[9]	JSSC'24[3]	ISSCC'25[6]	This work
Process	0.5 μ m CMOS SOI	0.5 μ m CMOS SOI	0.18 μ m BCD	0.18 μ m BCD SOI	0.18 μ m HV SOI	0.18 μ m BCD
Type	Class-E	Diff Class-E	Hybrid Class-ED	Regulated Class-E	Class-E	Class-E
V_{IN} [V]	40*	40*	7.4	10	20-35	10-20
Frequency [MHz]	6.78	13.56	6.78	6.78	6.78	6.78
ZVS during Rapid Load Transitions	N.A.	N.A.	N.A.	N.A.	N.A.	YES
Peak Output Power [W]	70	100	27	27	33	37.8
Peak Tx Efficiency [%]	90	91	N.A.	N.A.	94.2	94
Peak E2E Efficiency [%]	N.A.	N.A.	82	80	74.7	86.3

*Estimated from testing results

94% and peak E2E efficiency of 86.3%. The peak output power of 37.8 W is delivered at $V_{IN} = 20$ V with E2E efficiency of 86%. Fig. 11 highlights the efficiency improvement enabled by the auto-aligned structure under imaginary impedance mismatches. TABLE I compares the performance of the proposed PA with state-of-the-art designs.

IV. CONCLUSION

This paper presents a GaN-based 6.78 MHz Class-E PA for wireless charging. Based on the load-independent principle of

the Class-E inverter, an auto-aligned loop is designed using a duty ratio controlled switched-capacitor that adjusts for real impedance variations and imaginary impedance deviations. A WPT system using the Class-E PA that drives the transmitter coil and couples RF energy to the receiver with a reconfigurable regulating rectifier is built and tested successfully.

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