A 3.4-µW Active Charge Balancing With Optimal-Pulse-Width-Searching Technique for Implantable Biphasic Neural Stimulators

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***Abstract*—This paper presents a power efficient twin-track charge balancing method for implantable biphasic neural stimulators. Using a low-power digital optimal-pulse-width searching (OPWS) technique, the required balancing charge can be calculated within only one stimulus cycle. Therefore, the power consumption of the balancer is reduced significantly. In addition, a dual-hysteresis-based window comparator is adopted in order to avoid frequently reactivating balancer in the steady state, which is caused by the residual charge accumulation. The proposed charge balancer has been fabricated in a 0.18µm BCD process. For a stimulus current switching between 1.35mA and 1.65mA, the residual charge is compensated fast, and the anodic pulse-width is calibrated within one stimulus cycle. The measured power consumption of the proposed CB is 3.4µW.**

***Keywords*—Charge balancing (CB), electrode-tissue model, neural stimulator, optimal pulse-width searching (OPWS), residual charge accumulation.**

I. Introduction

Implantable neural stimulation has been proven as an effective approach to treat neurological disorders or restore sensations lost due to diseases or injuries. In the current-controlled biphasic stimulation, the anodic-phase charge is adopted to balance the cathodic-phase charge. However, partial stimulation charge will be consumed by the irreversible Faradaic reactions, and the required reversal-phase charge is difficult to estimate accurately. Thus, the typical perfectly matched biphasic stimulation usually brings residual charge accumulation [1], which may cause tissue damage and electrode corrosion.

In order to achieve long-term treatments, several efficient active charge balancing (CB) methods have been proposed to compensate for the residual charge adaptively. As shown in Fig. 1(a), simple short-pulse injection (SPI) techniques are proposed to instantaneously compensate the residual charge and make electrode voltage V_E return back to the safety region in each stimulation cycle [2]–[4]. However, the CB control circuits are frequently activated in these methods, which consume large amounts of power. A biphasic-pulse-charge control (BPCC) in Fig. 1(b) eliminates the charge accumulation by correcting the amplitude or pulse width of the cathodic and anodic stimulation pulses [5], [6], but long-time startup is required along with possible unwanted overshoot. In order to guarantee stimulus safety, an efficient twin-track scheme proposed in [7]–[9] combines SPI and BPCC to achieve an excellent CB performance as shown in Fig. 1(c). Unfortunately, since a relatively complex dual-loop

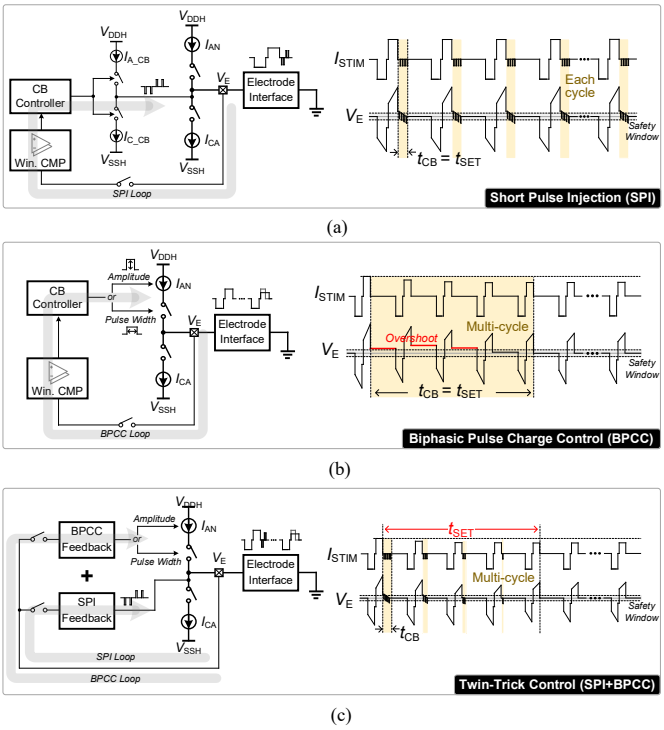


Fig. 1. Conventional charge balancing methods. (a) Short-pulse injection (SPI). (b) Biphasic-pulse charge control (BPCC). (c) Twin-track CB (SPI+BPCC).

control with a prolonged operation is adopted, the power consumption of its control circuits is still non-negligible. In contrast, the required balancing charge in [10] is predicted based on the measurement information of the real-time interface impedance, thus a one-shot CB can be achieved. However, the impedance-aware technique relies on the complex front-end (SAR ADC) and the digital back-end, which still consumes a lot of power.

II. Proposed Charge Balancing Method

A. Concept of the Proposed OPWS Technique

To address the limitations mentioned above, a power-efficient twin-track CB method is proposed in this work, as shown in Fig. 2(a). Using a low-power digital optimal-pulse-width-searching (OPWS) technique, the required balancing charge can be calculated within only one stimulus cycle. In the current stimulator, the current in anodic phase I_{ANO} is typically constant, and the charge in anodic phase depends on the anodic pulse duration T_{ANO}. A high frequency clock CLK_S is

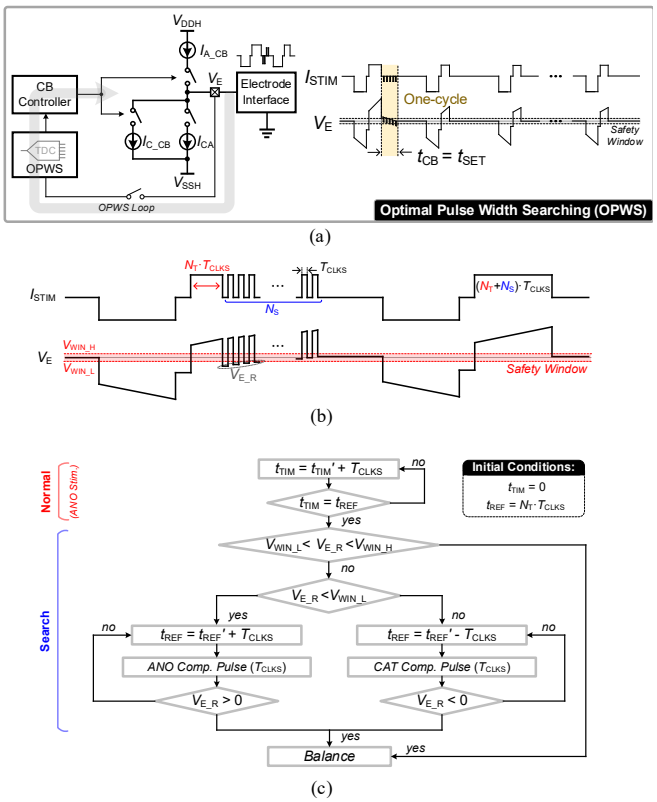


Fig. 2 (a) Proposed optimal pulse width searching (OPWS). (b) Concept of the proposed optimal balancing-charge searching. (c) Timing diagram of the proposed OPWS technique.

used for timing, and assuming that the pulse duration T_{ANO} lasts for N cycles, the charge Q_{ANO} can be easily quantified and adjusted, which can be expressed as

$$N = \frac{Q_{ANO}}{I_{ANO} \cdot T_{CLKS}} \tag{1}$$

Therefore, the optimal anodic pulse width can be calculated by searching the number N. For this purpose, an OPWS technique with Hill-climbing algorithm is introduced in this work to track the optimal pulse width in one stimulation cycle. As shown in Fig. 2(b), the initial anodic pulse width is set to $N_T \cdot T_{CLKS}$, and the optimal pulse width is searched by using a series of short cathodic/anodic current pulses with a duration of one cycle T_{CLKS} according to the safety window of the residual electrode voltage. In this way, the optimal pulse width can be calculated as $(N_T+N_S)\ T_{CLKS}$, and the parameter will be stored and used for the next stimulation cycle. Besides, all the short current pulses have the same amplitude with the initial balancing pulse to reduce the complexity of calculation, and the searching step can also be fixed.

Fig. 2(c) shows the simplified OPWS control flowchart. Each anodic phase can be divided into two operation modes: normal mode and search mode. The anodic pulse duration for normal mode in each stimulation cycle is indicated by the reference time t_{REF}. At the end of normal mode, the balancer will detect the residual electrode voltage V_{E_R} and determine whether the search mode needs to be enabled. If V_{E_R} exceeds the safety window, the balancer will enter the search mode. The detailed searching operation is described as follows. Once the residual electrode voltage V_{E_R} is higher than the upper bound V_{WIN_H} of the safety window, the reference time t_{REF}

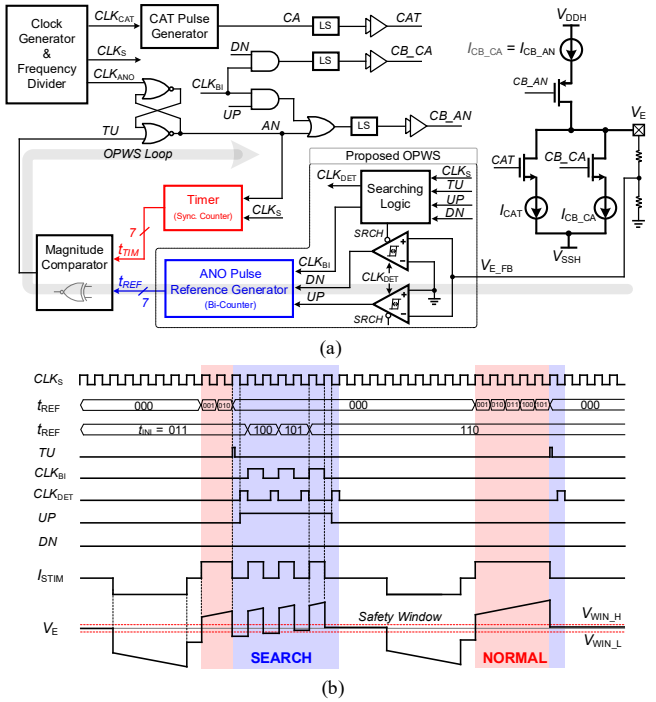


Fig. 3. (a) System architecture of the proposed active CB. (b) Timing diagram of the proposed OPWS technique.

will be reduced with a step of T_{CLKS}, and the corresponding short cathodic current pulse will be used for the residual charge compensation. This process is iterative until V_{E_R} returns to the common-mode voltage (0V), and both the search operation and charge compensation are finished. Similarly, once V_{E_R} falls below the lower bound, t_{REF} will be increased with a step of T_{CLKS} and the residual charge will be compensated by the corresponding short anodic current pulse. As a result, the CB can be easily achieved.

B. *Overall Architecture and Operation Principle*

The system architecture and operation principle of the proposed active CB are shown in Fig. 3 (a). The proposed OPWS technique mentioned above is implemented with a digital controlled feedback loop, which mainly consists of a window comparator, a 7-bit timer, a 7-bit anodic-pulse-reference generator, and a searching logic. The operation principle of the proposed CB is described as follows. In each anodic simulation phase, the anodic pulse is first generated by the timer. The stop time of the timer is controlled by a 7-bit pulse-width reference signal t_{REF} stored in the reference time generator, which indicates the anodic pulse duration. At the end of normal mode, the residual electrode voltage is detected by the window comparator, and the signals *UP* and *DN* are generated to control the searching operation. Once the residual electrode voltage exceeds the safety window, the search mode will be enabled. The signals *UP*=1 and *DN*=0 indicate the residual voltage is over the upper bound, while *UP*=0 and *DN*=1 indicate the residual voltage is below the lower bound. In these cases, the anodic pulse duration corresponding to the reference signal t_{REF} is adjusted by the digitally controlled feedback loop with a step of T_{CLKS}, and the residual charge is simultaneously compensated with a step of $I_{CB} \cdot T_{CLKS}$ accordingly. When the residual electrode voltage returns to the common-mode voltage level, both *UP* and *DN* become "0" and the optimal anodic pulse width searching is finished.

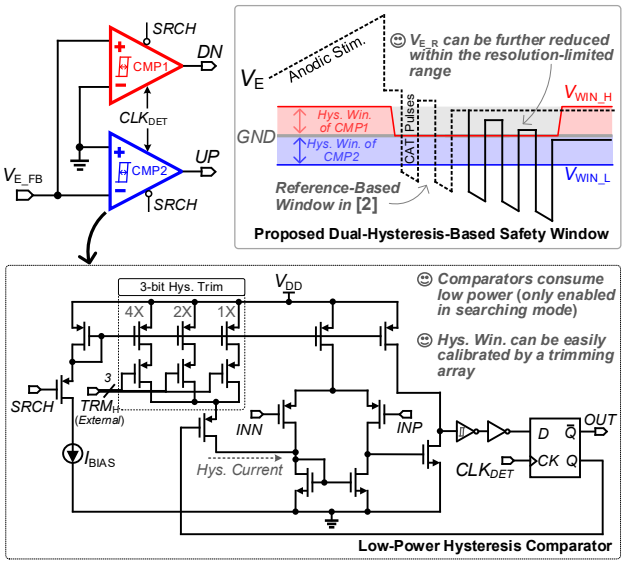


Fig. 4. The proposed dual-hysteresis-based safety window set by two hysteresis comparators.

Finally, the optimal pulse-width reference signal t_{REF} is generated and stored, which is used for the normal mode in the next stimulation cycle. The timing diagram of the proposed OPWS technology is illustrated in Fig. 3(b). After the duration of normal operation is adjusted, the reference time t_{REF} could be kept unchanged for a long time and the search mode is disabled. Generally, the reference time needs to be adjusted while the stimulus parameters are changed or the residual charge is accumulated for a long period.

III. Design Details of the Proposed CB

The detailed circuit implantations are shown in Fig. 4. The proposed dual-hysteresis-based safety window is set by two hysteresis comparators. Compared with the reference-based window in most conventional SPI schemes [2], the residual voltage after balancing depends on the searching resolution rather than the window bounds. Therefore, the residual voltage can be further reduced to the common mode voltage level. In this way, the speed of the residual charge accumulation can be slowed down, and the frequent reactivating can be avoided. A general two-stage hysteresis comparator with an output latch is adopted, and a 3-bit current array is used for hysteresis trimming. Note that the searching speed of OPWS is quite low, and thus the bias current is designed to be very small to save power consumption. Besides, since the output signal and the hysteresis state are stored, the comparator can always be shut down except for the searching operation, and its power dissipation can be further reduced. A simple searching logic used for generating main clock signals is also enabled only in search mode to minimize the dynamic power. The searching resolution will directly determine the accuracy of the charge compensation for the proposed CB. Note that the higher searching resolution can further reduce the residual charge, but might bring a higher power consumption. On the contrary, the large searching step might cause the oscillation. The searching clock cycle T_{CLKS} can be externally trimmed by a 2-bit selector to choose the appropriate searching resolution.

As shown in Fig.5, The power consumption of the CB control circuits in the balancing phase mainly include the drivers of the power transistors and the window comparator.

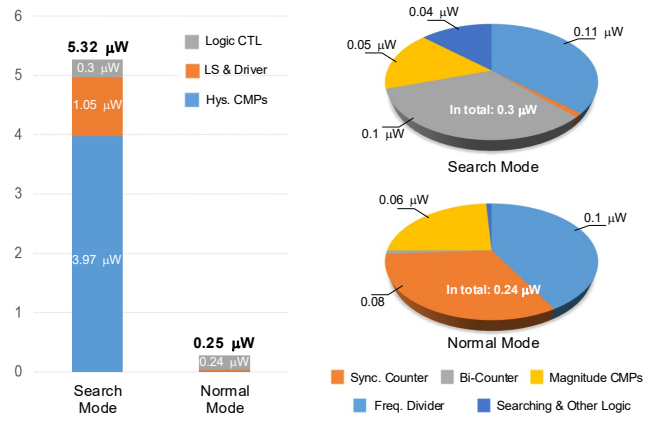


Fig. 5. (a) Power consumption breakdown of the proposed CB control loop in different modes. (b) Detailed power distribution of the logic control.

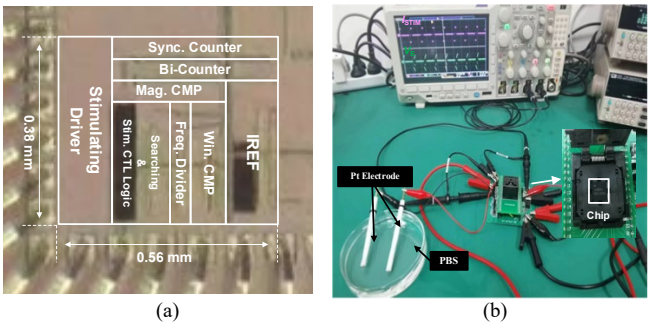


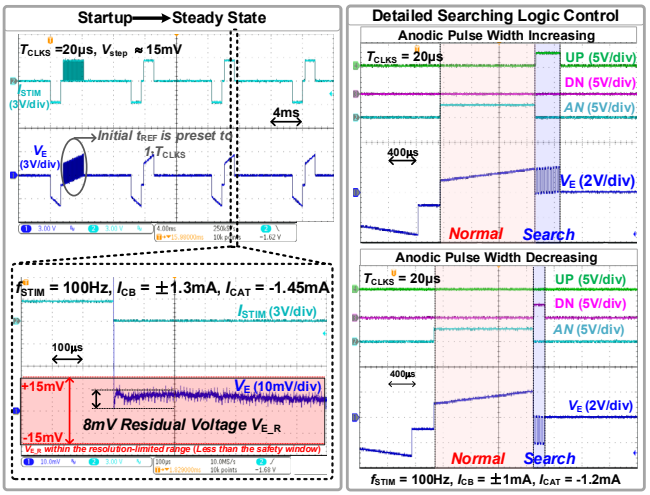
Fig. 6. (a) Chip photograph. (b) In-vitro measurement setup.

The simulated power loss breakdown shows that the proposed balancer is power efficient in each operation mode, and consumes only 5.32µW and 0.25µW in the search mode and the normal mode under the conditions of T_{CLKS}=20µs and V_{DD}=2.5V, respectively. Furthermore, the duration of the search operation is very short thanks to the proposed OPWS, and thus the average power dissipation of the entire control circuits is extremely low in a long duration.

IV. Measurement Results

The proposed stimulator IC was fabricated in a 0.18µm BCD process. Fig. 6 shows the chip photograph (the active area without pads is 0.21mm^2) and in-vitro measurement setup. The functionalities of the proposed OPWS is verified through the platinum electrodes in phosphate buffer solution (PBS). Using the methods introduced in [11], the parameters are extracted to be 2kΩ and 2.2µF, for R_s and C_{dl} in PBS, respectively, at stimulation frequency of 100Hz.

Fig. 7(a) shows the biphasic stimulation procedure from the startup to the steady state. In order to observe the initial searching phase clearly, the initial anodic pulse width is preset to $1 \cdot T_{CLKS}$. The optimal pulse-width searching and residual charge compensation are achieved in only one stimulation cycle. The residual electrode voltage after OPWS is also measured. With the proposed dual-hysteresis-based window comparator, the residual voltage can be compensated within the searching resolution limited range ±15mV instead of the safety window under the conditions of T_{CLKS}=20µs and I_{CB}=±1.3mA. The measurement results of the detailed OPWS



(a) (b)

Fig. 7 (a) Measured waveforms of the proposed OPWS-based CB from startup to steady state. (b) Detailed OPWS control.

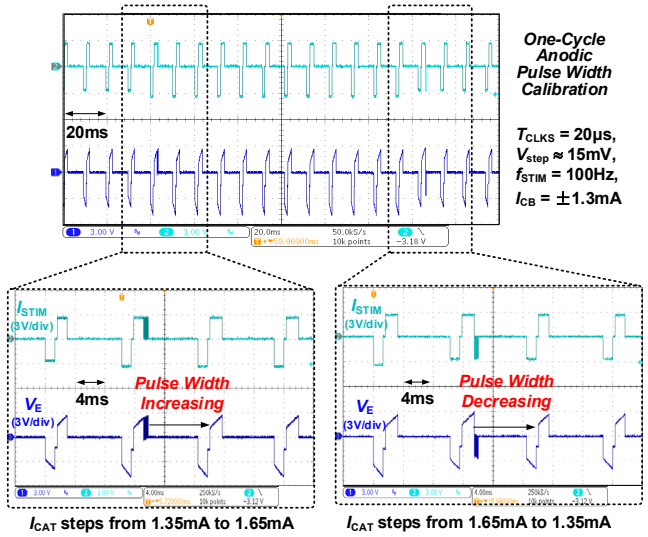


Fig. 8. Measured waveforms of stimulus transient response.

control logic during the stimulus load transient are shown in Fig. 7(b), and the mode switch can be observed clearly.

Fig. 8 shown the measured stimulus transient response. When the cathodic stimulus current I_{CAT} is switched between 1.35mA and 1.65mA, the anodic pulse-width calibration could be achieved within one cycle, and in the subsequent cycle the stimulator could be operated in the normal mode. The comparison with state-of-the-art is shown in TABLE I. This work can achieve one-cycle residual compensation with the proposed OPWS with a very low average power loss of only 3.4µW.

V. Conclusion

This paper presented a low-power CB for neural stimulation. The proposed OPWS technique achieved both residual compensation and optimal anodic pulse width calculation in only one stimulation cycle. The performance of the proposed techniques is verified by the experimental results. It improves the balancing speed and reduces the power consumption significantly.

TABLE I. Comparison With State-of-The-Art

	ISSCC 2020 [2]	TBCAS 2018 [6]	A-SSCC 2015 [7]	JSSC 2018 [8]	SSC-L 2021 [10]	This Work
Technology (µm)	0.35	0.35	0.18	0.35	0.18	**0.18**
Voltage Compliance (V)	4	49	20	22	3.3	**±6**
Max. I_{STIM} (mA)	0.775	10	1.2	5.12	1	**2**
ETI Model R_s (kΩ)+C_{dl} (µF)	2 0.5	N/A	10 0.2	3 1.3	100 2.8	**2** **2.2**
CB Methods	PI	BPCC	PI+BPCC	PI+BPCC	IACB	**OPWS**
Charge Compensating Strategy	Each-cycle	Multi-cycle	Multi-cycle	Multi-cycle	One-shot	**One-cycle**
Safety Win. (mV)	±50	±50/±100	±30	±50/±100	N/A	**±30**
CB Precision (mV)	50	20	30	20	4	**30[b]**
Power Consumption[a] (µW)	N/A	41	110	56	37.6	**3.4[c]**

[a] Only for CB control.
[b] Residual voltage can be further compensated within the resolution-limited range ±15mV.
[c] Average power loss during the stimulus procedure (@ T_{CLKS} = 20µs, I_{CB} = ±1.3mA).

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