A Four-phase Flying Capacitor Shared Dynamic Hybrid Converter with Hierarchical Power Delivery and Four-phase Temperature Management

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***Abstract*—This paper proposes a Four-Phase Flying Capacitor Shared Dynamic (4PFCSD) Hybrid Converter, optimized for high current delivery and integrated with a Four-Phase Temperature Management (FPTM) system. To enhance light-load efficiency, a phase-shedding strategy enables two-phase operation in discontinuous conduction mode (DCM), achieving up to 74.2% efficiency at a 100 mA load. The converter supports a wide voltage conversion ratio (VCR) of up to 0.5, covering the full duty cycle range from 0% to 100%. A hierarchical power delivery (HPD) 3D package is employed to suppress electromagnetic interference (EMI), reducing high-frequency noise by 15 dB. The FPTM system improves thermal performance, increasing per-phase efficiency by at least 7%, and enabling a peak overall efficiency of 91.4% at a 5 A load.**

Keywords—advanced temperature tuning (ATT) technique, Four-Phase Flying Capacitor Shared Dynamic (4PFCSD) Hybrid Converter, hierarchical power delivery (HPD) package.

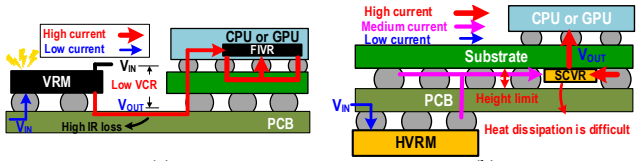
I. INTRODUCTION

In response to the surging demand for artificial intelligence (AI) and high-power processors, computing performance has advanced rapidly—even as available printed circuit board (PCB) space remains limited. As shown in Fig. 1(a), the conventional power delivery solution in [1] relies on a Voltage Regulator Module (VRM) that delivers power via a horizontal path over an extended transmission distance. This approach introduces significant drawbacks, including increased power distribution network (PDN) losses that reduce overall system efficiency. Additionally, the extended routing consumes valuable PCB area, driving up manufacturing costs and constraining space for external passive components.

To address some of these limitations, the vertical power delivery architecture in [2], shown in Fig. 1(b), adopts a two-stage strategy to gradually step down current and voltage, effectively reducing PDN losses and saving PCB area. However, this approach overlooks critical factors such as thermal management and bump height limitations. Inadequate heat dissipation can lead to thermal buildup, compromising component reliability and system longevity. Meanwhile, bump height constraints can restrict the flexibility and scalability of power routing. These challenges underscore the need for a more advanced and efficient power delivery architecture that simultaneously addresses layout, thermal, and electrical performance.

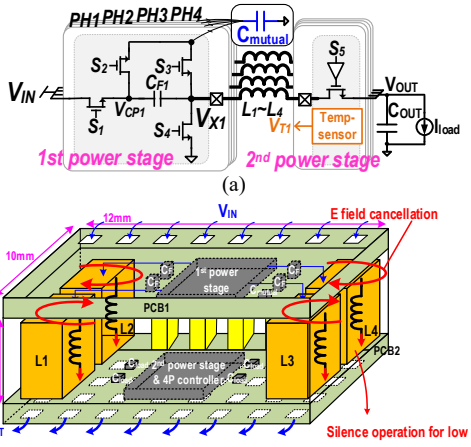
This paper proposes a 4PFCSD hybrid converter integrated with a Hierarchical Power Delivery (HPD) 3D package, featuring an advanced temperature-aware tuning technique to reduce PDN losses and optimize PCB area, as illustrated in Fig. 2(a). The 4PFCSD converter adopts a cost-effective two-stage PCB stack-up structure, minimizing the need for expensive 2.5D or 3D fabrication, as shown in Fig. 2(b). The first stage comprises interleaved switched-capacitor (SC) circuits mounted on the underside of the first PCB. The second stage integrates pass switches, inductors, and embedded temperature sensors for each phase into a compact module. These elements are managed by a Four-Phase Temperature Management (FPTM) system located on the top layer of the second PCB, enabling precise thermal control and enhanced performance.

High current arises at the second stage as V_{OUT} is stepped down from a high V_{IN} to the low voltage levels required by AI servers. To manage the resulting thermal stress, a temperature sensor is integrated into each output stage to determine when to activate the FPTM system. Unlike conventional interleaved multi-phase converters, the proposed 4PFCSD Hybrid Converter emphasizes thermal management, ensuring that heat is evenly distributed across the entire PCB. Moreover, in planar power designs, suppressing electric field interference becomes challenging due to high power density. When distributed inductive currents are not properly managed, the resulting electric fields can disrupt interleaved control and degrade high-current driving performance. To address this, the converter employs an inductor electric field cancellation topology that effectively reduces EMI and enables near-silent operation. By leveraging a vertically stacked 3D architecture, each PCB layer remains compact, with shortened current paths that reduce PDN impedance. This configuration also improves thermal dissipation, ultimately boosting both power density and overall efficiency.



(a) (b)

Fig. 1. (a) High current of conventional power delivery in [1] suffers from large IR power loss. (b) Heat dissipation becomes difficult in [2].



(a)

(b)

Fig. 2. (a) Schematic of the proposed 4PFCSD hybrid converter. (b) The two-stage hybrid converter has been packaged into one 3D package for better heat dissipation and EMI reduction.

The remainder of this paper is organized as follows. Section II details the operating principles of the 4PFCSD

hybrid converter. Section III introduces the advanced temperature tuning (ATT) technique, which enables efficient high-current delivery to CPUs or GPUs while enhancing thermal dissipation. Section IV presents the experimental results, and Section V concludes the paper.

II. Proposed 4PFCSD Hybrid Converter

A. Power stage of 4PFCSD

In continuous conduction mode (CCM), each phase of the 4PFCSD hybrid converter operates through two stages: Φ_1 and Φ_2, as illustrated in Fig. 3(a) and (b), respectively. During the Φ_1 stage, switches S_1, S_3, and S_5 are turned on, allowing the inductor to magnetize and produce a rising inductor current. In the Φ_2 stage, switches S_2, S_4, and S_5 are activated, causing the inductor to demagnetize and generate a falling current. The 4PFCSD hybrid converter, implemented using a 3D package, is divided into two distinct stages. In the first stage, each phase includes a flying capacitor (C_F) and a shared mutual capacitor (C_{mutual}) to optimize area usage. The alternating Φ_1 and Φ_2 operations automatically balance the voltage across C_F to $V_{IN}/2$.

Compared to the cross-connected capacitor (CCC) converter [5], this design reduces the switching node voltage swing (V_{X1}) from V_{IN} to $V_{IN}/2$, thereby lowering the maximum voltage stress on the power MOSFETs to $V_{IN}/2$. The intermediate inductors (L_1–L_4) between the two stages provide effective voltage isolation from V_{IN}, ensuring that the voltage stress on second-stage switches is constrained to V_{OUT}. Additionally, each of the four phases is spaced 90 degrees apart in phase, enabling interleaved inductor currents that significantly suppress current ripple, as depicted in Fig. 3(c).

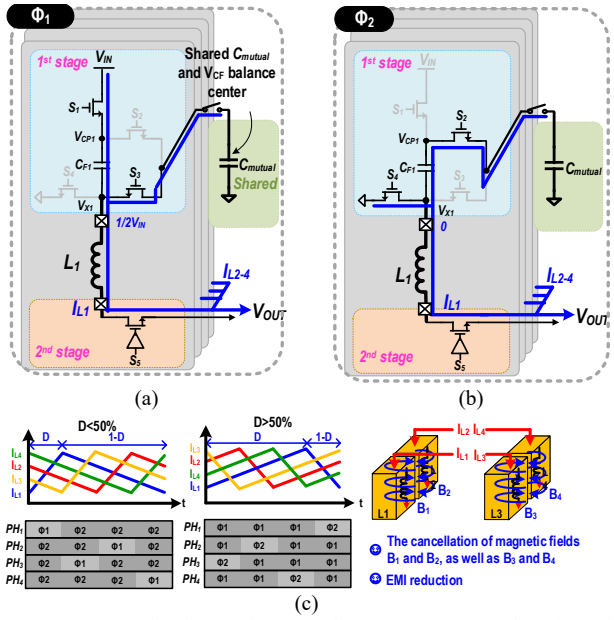


Fig. 3. (a) Operation in Φ_1. (b) Operation in Φ_2. (c) Φ_1 and Φ_2 in each phase when D < 50% and D > 50%.

In addition, unlike [3]–[6], the 4PFCSD hybrid converter supports discontinuous conduction mode (DCM) under light load conditions, maintaining high efficiency across a wide load range. As shown in Fig. 4, DCM operation is achieved through a time-multiplexed control scheme in which each phase is sequentially activated per cycle, while the remaining phases remain idle to cool down. This reduces the cumulative turn-on time per phase and enhances thermal dissipation.

Compared to [3]–[5], the 4PFCSD hybrid converter achieves a VCR of 0.5, supporting a full duty cycle range from 0% to 100%, thereby overcoming the conventional constraint of D < 50%. High overall conversion efficiency is made possible not only through well-balanced current distribution but also through effective thermal management. In contrast, previous works [3]–[6] focus solely on current balancing, which limits performance and efficiency, especially under heavy load conditions.

B. HPD 3D Package

The 3D HPD package, illustrated in Fig. 2(b), integrates both the first-stage and second-stage chips along with external passive components into a compact, vertically stacked structure. Each power phase includes a built-in temperature sensor, while the FPTM system—mounted atop the second PCB—actively monitors and regulates thermal performance. This dual-layer PCB configuration not only reduces PDN losses but also maximizes PCB utilization, offering greater layout flexibility for other system components. By leveraging real-time thermal feedback, the FPTM enhances heat dissipation efficiency and ensures reliable, high-efficiency operation across varying load conditions.

At the second stage, the low output voltage leads to high output current, which in turn generates significant heat. To address this, each output stage incorporates a temperature sensor that determines when to activate the FPTM system. Unlike conventional interleaved multi-phase converters that focus primarily on current balancing, the proposed 4PFCSD hybrid converter emphasizes temperature-aware control to evenly distribute thermal load across the entire PCB. Moreover, in traditional planar power delivery designs, suppressing the electric field effects from each power stage is challenging due to high power density constraints. In contrast, the HPD 3D packaging integrates an inductor electric-field cancellation topology, effectively minimizing EMI and enabling quiet operation. The vertical stacking structure also shortens the current path and reduces the overall PCB footprint, leading to lower PDN impedance, improved thermal dissipation, and enhanced overall power density and efficiency.

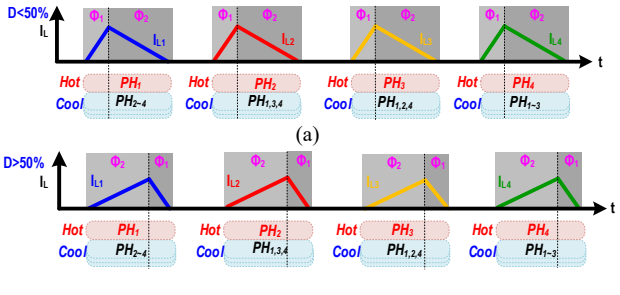


Fig. 4. Operation wave form of 4PFCSD hybrid converter in DCM (a) D < 50% (b) D > 50%.

III. Circuit Implementation

To demonstrate how the FPTM effectively resolves thermal challenges, Fig. 5 presents the 4PFCSD controller integrated with the FPTM system. Designed to optimize thermal performance and suppress EMI, the FPTM continuously monitors the temperature of each phase and dynamically adjusts current distribution via the current-balancing circuit. Phases experiencing higher temperatures are selectively throttled to allow for cooling, while the remaining phases maintain balanced current delivery with synchronized operation to ensure EMI cancellation.

A. Temperature sensor

Fig. 6(a) compares the phase-specific proportional-to-absolute-temperature (PTAT) voltage signals ($V_{PTAT1–4}$) against a hysteresis window defined by upper and lower threshold voltages, $V_{th,up}$ and $V_{th,dn}$, respectively. Fig. 6(b) presents the timing diagram of the temperature sensing and management mechanism. Each output stage includes a temperature sensor that continuously monitors its thermal condition to determine whether cooling is required. The sensor generates PTAT voltages, which are compared against the hysteresis window. When any V_{PTAT} exceeds the upper threshold ($V_{th,up}$), an overheat flag ($V_{Oh1–4}$) is asserted. This triggers the corresponding SR latch, activating the cooling signal ($V_{sleep1–4}$) and initiating the FPTM to reduce the temperature of the affected phase. To ensure sufficient cooling, each V_{sleep} signal remains active for a minimum duration of 2 ms, enforced by a 12-bit counter and decoder circuit. This guarantees that the temperature has enough time to fall below the lower threshold ($V_{th,dn}$). Once both conditions—V_{PTAT} below $V_{th,dn}$ and the elapsed minimum cooling time—are satisfied, the system deactivates the corresponding V_{sleep} signal, concluding the thermal management cycle for that phase.

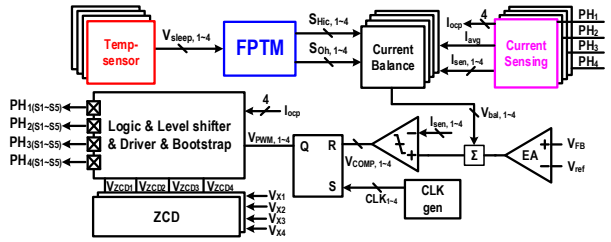
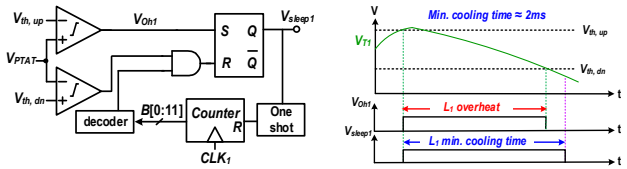


Fig. 5. The controller of 4PFCSD hybrid converter can solve heat issues and reduce EMI noises.

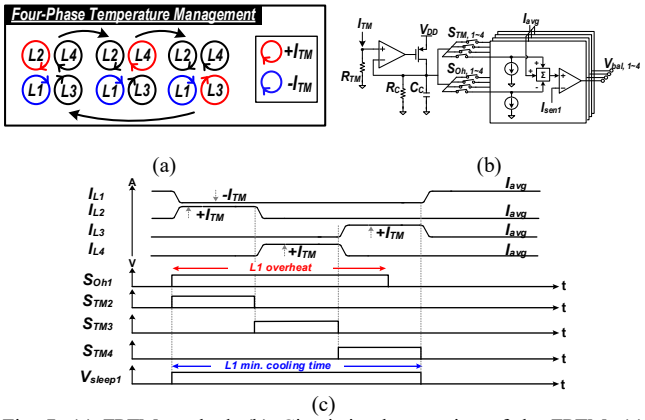


(a) (b)

Fig. 6. (a) Temperature sensor. (b) Timing diagram of the temperature sensor.

B. Four-phase Temperature Management (FPTM)

Fig. 7(a) illustrates the FPTM method. When one phase—such as Phase 1—experiences thermal stress, its inductor current is reduced by 50% to allow cooling. Meanwhile, the remaining phases (Phases 2 to 4) sequentially compensate for the reduced output, each operating for a fixed duration of 0.6 ms to prevent overheating. This current redistribution effectively lowers the thermal burden on the overheated phase while maintaining stable operation. Traditional implementations often rely on a separate constant current (CC) loop to regulate inductor current, but switching between the CC loop and the current balancing (CB) loop can cause instability due to transconductance (G_m) mismatches. Fig. 7(b) presents the FPTM circuit design, which resolves this issue by allowing both loops to share a common error amplifier—ensuring consistent loop gain and stable transitions. The current modulation is controlled by $S_{Oh,1–4}$ (for current suppression) and $S_{TM,1–4}$ (for current boost). Smooth current transitions are achieved using compensation elements R_C and C_C. Fig. 7(c) explains the FPTM control flow. When $S_{Oh,1}$ is activated, Phase 1's inductor current is suppressed by 50%. As it cools, STM signals for Phases 2 to 4 are sequentially triggered to increase their respective inductor currents, temporarily compensating for the reduced output of Phase 1. Each supporting phase is activated for a limited time (0.6 ms) to prevent thermal buildup. Through this dynamic current redistribution, FPTM ensures uniform thermal distribution across all phases and enhances the overall thermal stability of the system.



(a) (b) (c)

Fig. 7. (a) FPTM method. (b) Circuit implementation of the FPTM. (c) Operation principle of the FPTM.

IV. Experimental Results

The chip is fabricated using a 0.15 μm BCD process, with the micrographs of the first and second chips shown in Fig. 8 (left). The prototype implementation of the 4PFCSD hybrid converter is displayed in Fig. 8 (right).

Fig. 9 illustrates the operating waveforms of the 4PFCSD hybrid converter under CCM. When the input voltage is 12 V and the output voltage is 1 V, the system operates with a duty cycle below 50%. Thanks to the four-phase interleaved configuration, the phase current ripples effectively cancel out, significantly reducing output voltage ripple. This ripple suppression enhances overall efficiency and enables the system to support a maximum load current of 8 A. Under an input voltage of 6 V and an output voltage of 1.8 V, the system also reaches the same 8 A maximum load current, but the duty cycle exceeds 50%. In this scenario, each phase handles an average inductor current of 2 A, ensuring well-balanced current sharing across all four phases.

Fig. 10 presents the operating waveforms of the 4PFCSD hybrid converter in DCM. When the input voltage is 12 V and the output voltage is 1 V, the converter supports a minimum load current of 0.1 A, operating with a duty cycle below 50%. Similarly, under a 6 V input and 1.8 V output, the converter also handles a 0.1 A minimum load current, but with a duty cycle exceeding 50%. In DCM operation, each phase switches sequentially in a time-multiplexed manner, while the inactive phases enter a cooling state. This alternating operation enhances thermal management and maintains high efficiency under light-load conditions. Fig. 11(a) presents the measurement results of the FPTM. At an 8 A load current, the DC inductor current of phase one is reduced to 1 A, while the remaining phases sequentially increase their inductor currents to 3 A. This dynamic redistribution prevents phase one from overheating or triggering thermal shutdown. During FPTM operation, the output voltage experiences a minor overshoot of 32 mV. Fig. 11(b) shows the infrared thermography of the 4PFCSD hybrid converter. The FPTM effectively lowers the temperature of the overheated phase, while achieving more uniform thermal distribution across the remaining phases. This results in a more balanced die temperature and enhances the overall thermal performance and reliability of the system.

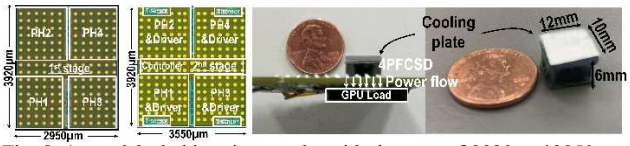


Fig. 8. 1st and 2nd chip micrographs with the area of 3920μm*2950μm and 3920μm*3550μm, respectively (left); the prototype of the 4PFCSD (right).

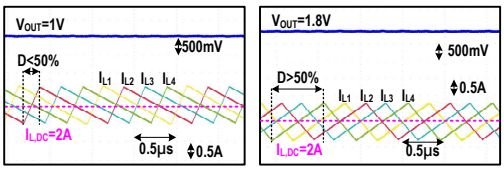


Fig. 9. Measurement results of the steady-state operation in CCM.

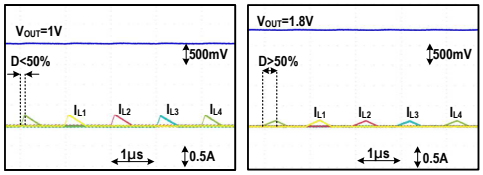
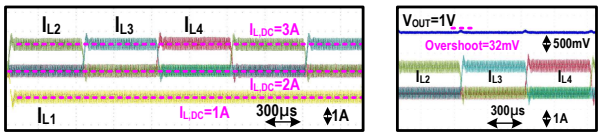
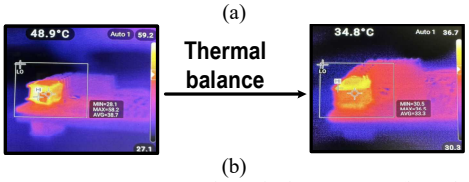


Fig. 10. Measurement results of the steady-state operation in DCM.



(a)



(b)

Fig. 11. (a) Measurement results of the FPTM. (b) The infrared thermography of the 4PFCSD.

Fig. 12 illustrates the conducted EMI noise performance of the 4PFCSD hybrid converter. By employing a vertically stacked PCB architecture, the converter achieves significant EMI suppression, particularly in the high-frequency range. Notably, the design enables the inductor current to reduce EMI noise by up to 15 dB at 1 GHz—a substantial improvement that minimizes electromagnetic interference during operation. This is especially beneficial for sensitive systems like AI servers and high-performance computing platforms, where reduced EMI enhances signal integrity, minimizes disturbances in nearby circuits, and improves overall system reliability. Fig. 13(a) demonstrates that applying FPTM across varying load currents (I_{LOAD}) increases peak efficiency by approximately 10%, primarily due to improved thermal regulation. In Fig. 13(b), FPTM effectively lowers component temperatures, contributing to an overall efficiency gain of up to 9%. Besides, the 3D PCB structure supports both two-phase and four-phase operation, mitigates magnetic coupling effects, and contributes to EMI reduction of up to 15 dB, further enhancing the converter's performance and robustness.

Table I presents a performance comparison between the proposed 4PFCSD hybrid converter and previously published designs. The 4PFCSD converter supports a wide load current range and a broad VCR, offering significant advantages over prior DCM-based solutions [3]–[5]. Unlike these earlier works, this design achieves DCM operation with a high efficiency of up to 74.2%. It also supports a VCR of D/2, enabling full duty cycle coverage from 0% to 100%. The maximum voltage stress on the power switches is limited to just 6 V, enhancing reliability. Thanks to the four-phase interleaved topology, the inductor current ripple is minimized, and the average inductor current per phase is reduced to $I_{LOAD}/4$. A key differentiator of this work is its integrated temperature management, which is absent in other architectures. Additionally, the two-stage PCB structure significantly reduces both the overall PCB area and PDN losses. This allows the system to achieve a high current density of 0.293 A/mm². When V_{IN} = 12 V and V_{OUT} = 1 V, the converter has a peak efficiency of 91.4%, showing excellent performance and thermal optimization.

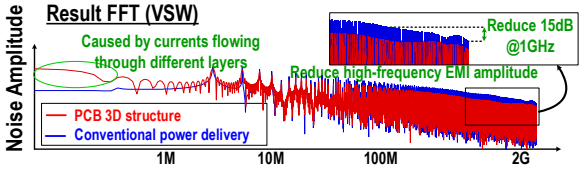
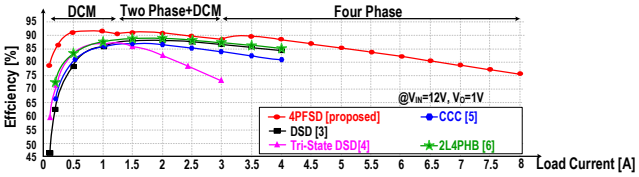
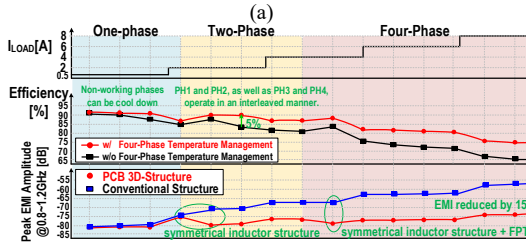


Fig. 12. Measurement result of conductive EMI noise.



(a)



(b)

Fig. 13. (a) Efficiency compared to existing technology. (b) Efficiency and EMI versus time.

Table I. Comparison with prior arts.

Parameter	JSSC 2022 [3]	ISSCC 2020 [4]	ISSCC 2022 [5]	ISSCC 2023 [6]	This work
Topology	DSD	Tri-State DSD	CCC	2L4PHB	4PFCSD
Process	180nm BCD	180nm BCD	180nm BCD	180nm BCD	150nm BCD
V_{IN} (V)	12/24	12/24	12	12	3-12
V_O (V)	1	1	0.9-1.8	1-1.8	0.3-1.8
Duty>50%	NO	NO	NO	NO	YES
$I_{LOAD,max}$ (A)	4	3	4	4	8
F_s (MHz)	1	0.1-1	2	1	1×4
L (μH)	1.8×2	0.56×2	0.74×2	1×2	1×4
Co (μF)	10	10	10.6	22	10
Maximum Voltage Stress (V)	12	6	12	11	6
Inductor Current	$I_{LOAD}/2$	$I_{LOAD}/2$	$I_{LOAD}/2$	$I_{LOAD}/2(1+D)$	$I_{LOAD}/4$
Peak η (%)@ V_{OUT}= 1V	88.3	88.3	86.8 @ 1.2V	89	91.4%
η (%)@ V_{OUT}= 1V, I_{LOAD}= 4A	85	74 @ 3A	81 @ 1.2V	85.3	88.1%
η (%)@ V_{OUT}= 1V, I_{LOAD}= 0.1A	46	58	66 @ 1.2V, 0.2A	72.2 @ 0.2A	74.2%
DCM	NO	NO	NO	YES	YES
Stage	1	1	1	1	2
Temperature management	NO	NO	NO	NO	Yes
Max I density [A/mm²]	N.A.	0.032	0.133	0.191	0.293

REFERENCES

[1] E.A. Burton et al., "FIVR — Fully integrated voltage regulators on 4th generation Intel® Core™ SoCs," *IEEE APEC 2014*, pp. 432–439, Mar. 2014.

[2] C. Hardy et al., "A Scalable Heterogeneous Integrated Two-Stage Vertical Power-Delivery Architecture for High-Performance Computing," *ISSCC*, pp. 182-184, Feb. 2023.

[3] Z. Liu et al., "A 12V/24V-to-1V PWM-Controlled DSD Converter With Delay-Insensitive and Dual-Phase Charging Techniques for Fast Transient Responses," *JSSC*, pp. 3853-3864, Dec. 2022.

[4] K. Wei et al., "A Direct 12V/24V-to-1V 3W 91.2%-Efficiency Tri-State DSD Power Converter with Online VCF Rebalancing and In-Situ Precharge Rate Regulation," *ISSCC*, pp. 190–191, Feb. 2020.

[5] T. Hu, M. Huang et al., "A 4A 12-to-1 Flying Capacitor Cross-Connected DC-DC Converter with Inserted D>0.5 Control Achieving >2x Transient Inductor Current Slew Rate and 0.73× Theoretical Minimum Output Undershoot of DSD," *ISSCC*, pp. 1-3, Feb. 2022.

[6] W. -L. Zeng et al., "A 12V-Input 1V-1.8V-Output 93.7% Peak Efficiency Dual-Inductor Quad-Path Hybrid DC-DC Converter," *ISSCC*, pp. 10-12, Feb. 2023.