A 50Mbps 0.7pJ/bit Receiver with Integrating Clock-Data-Recovery using Body-Resonance HBC for AR/VR and Wearable-AI Nodes

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***Abstract*—This paper presents the first implementation of body-resonance (BR) human body communication (HBC) receiver, operating at a data rate of 50 Mbps. An on-off-keying (OOK)-based modulation scheme has been employed to exploit the low insertion loss of the human body at the resonance peak of 100 MHz. An enhanced integrating amplifiers has been implemented, along with the employment of a novel and more robust clock data recovery architecture. These improvements have enabled the construction of the most energy-efficient human-body-communication receiver front-end to date. The implementation is fabricated in 65nm CMOS technology node and occupies an active area of $0.04mm^2$. Furthermore, it achieves an energy efficiency of 0.7pJ/b and a bit error rate (BER) of 10^{-5}.**

***Index Terms*—Human Body Communication, Augmented Reality, Virtual Reality, Body Resonance, sub-pJ/bit, Wireless Body Area Network (WBAN), Low Power**

I. Introduction

Radio frequency (RF) technologies have revolutionized wireless communication, particularly in the Internet of Things (IoT). Miniature sensors and devices implanted on the human body, interconnected through a wireless body area network (WBAN), require low power consumption for continuous operation. The battery life of these body-nodes is heavily dependent on the communication budget allocated to send and receive data from the main body hub. The severe channel loss (80-90dB) for Non-Line-of-Sight (NLoS) RF-based communication further exacerbates this issue, requiring transceivers to consume mWatts to Watts power.

Electro-quasistatic (EQS) Human Body Communication (HBC)[1, 2] was introduced as an energy-efficient and secure alternative to RF-based communication. It utilizes the conductive nature of the human body to establish a broadband channel, operational up to 20-25 MHz. Several transceivers [3, 4, 5, 6, 7, 8] have been developed which show impressive energy efficiency for communication links around the body, surpassing the $<$10 pJ/b benchmark.

However, several factors render the EQS-HBC inefficient for extending this technology to the data rate and energy efficiency of contemporary AR/VR or wearable AI nodes. The substantial insertion loss of the body channel (60-70dB) is followed by the limited channel bandwidth ($<$ 20MHz) and capacity restrictions, which limit the construction of a sub-pJ/bit body-channel communication link.

Body-Resonance (BR) Human Body Communication (HBC)[9, 10, 11] has emerged as a promising solution to support new demanding applications, as shown in Fig. 1(a), due to its higher channel capacity and 10-20 dB loss benefit over EQS-HBC. Fig. 2 shows the transfer function of the body-channel, highlighting the 16 dB peak from EQS-HBC. It introduces a possibility of improvement in energy efficiency, presenting an attractive option for enhanced connectivity by alleviating the current limitations as shown in Fig. 1(b).

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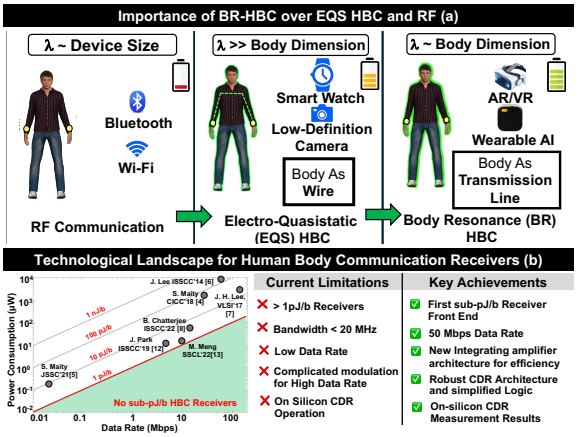

Fig. 1. (a) Importance of BR-HBC over RF and EQS HBC in supporting low power WBAN, (b) technological landscape for human body communication receivers.

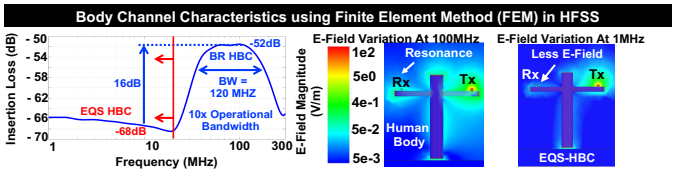

Fig. 2. Body channel characteristics using finite element method based simulation in HFSS for BR HBC and EQS HBC

Fig. 3 illustrates the evolution of various iterations of HBC receivers to the current implementation, including two magnetic-HBC implementations[12],[13]. This paper presents the first sub-pJ/b HBC receiver front-end implementation, accompanied by a novel integrating CDR architecture capable of operating at a data rate of 50 Mbps.

II. Overall Architecture

The receiver has been optimized by utilizing the 120MHz operational bandwidth centered around the resonance peak at 100MHz. A 50 Mbps data rate with an On-Off Keying (OOK)

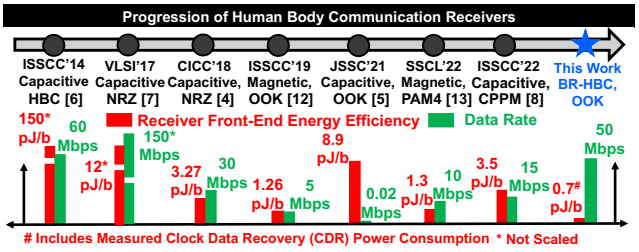

Fig. 3. Progression of human body communication receivers

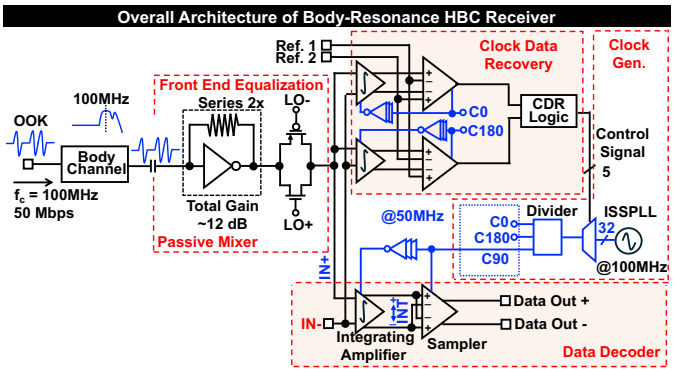

Fig. 4. Overall architecture of the implemented body-resonance human body communication receiver

modulation scheme employing a 100MHz carrier frequency has been selected to maximize the received signal. Fig. 4 depicts the overall architecture of the BR-HBC receiver.

A. Front-End Equalization

Front-end equalization comprises switchable two-stage self-biased inverters and a passive mixer, as depicted in Fig. 4. Each stage of the self-biased inverter offers a gain of 6dB. It is feasible to achieve higher gain by cascading two stages of self-biased inverters to compensate for the limitations of the passive mixer. A double-balanced passive mixer demodulates the OOK signal using a local oscillator (LO) that provides opposite phases of a 100MHz clock. The implemented double-balanced passive mixer improves the linearity and isolation, while providing an improved conversion gain.

B. Data Decoder

The implemented data decoder has been shown in Fig. 4. It is composed of an integrating amplifier, followed by a differential double tail sampler. The differential outputs of the integrating amplifier are cross-coupled and connected to the inputs of the differential double-tail sampler, thereby observing twice the overall swing before sampling, reducing the required gain from the integrating amplifier. Positioning the relative clocks of integrating amplifiers and samplers is crucial. The integrating amplifier integrates voltage differences on load capacitors during the high clock state before recharging. Hence, the sampler needs sufficient time to latch to peak-to-peak voltage before the integrating amplifier is reset.

An enhanced integrating amplifier[14] has been implemented to further improve the current efficiency for a given

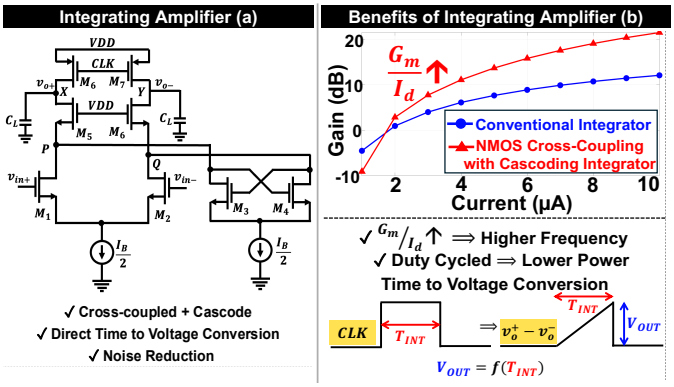

Fig. 5. (a) Cross-coupled nMOS with cascoded integrating amplifier (b) benefits of implemented integrating amplifier over the conventional counterpart

gain, as shown in Fig. 5(a). As illustrated in Fig. 5(b), the nMOS cross-coupling with cascoding offers a substantial enhancement in the amplifier's gain relative to a conventional integrating amplifier, while maintaining a comparable current consumption. This enhancement facilitates the design of a more energy-efficient receiver architecture.

The integrator also serves as a medium for transforming the time information present in the clock or input signal into voltage information at the end of the integration period. The integrated output differential voltage is a function of the integration time (T_{INT}), which is defined by the clock period in this architecture. The clock data recovery module leverages this feature to develop a novel integrating bang-bang CDR.

C. Clock Data Recovery

Integrating receivers require a unique clock positioning strategy. Conventional receivers sample data mid-bit, while integrating receivers provide an amplified eye-width at integration's end. To achieve the minimum bit error rate, the maximum data-eye width must be included during integration, ensuring the midpoint of the data bit coincides with the midpoint of the clock to avoid data and clock non-ideality.

Fig. 4 depicts the implemented CDR architecture, while Fig. 6 elucidates its operating principle. The primary design blocks in this architecture comprise a pair of previously described integrating amplifiers and differential double-tail comparators, which operate at mutually opposite clock phases.

If the clock edge is delayed with respect to the data edge, as shown in Fig. 6, the integrator on the high clock state (INT1) perceives the data as constant during integration, resulting in a ramp output that reaches the maximum integrated voltage. Two reference voltages define an acceptable region. Sampling within this region generates a 1 output. Conversely, the integrator on the opposite phase (INT2) perceives the data transition from 1 to 0, causing the integrated voltage to increase when data is 1 and decrease when data is 0, preventing it from reaching the acceptance region and resulting in a 0 output. The T1-T2 pair, 1 and 0, defines a late clock condition.

When the clock is ahead of the data, INT1 fails to integrate up to the acceptance region, outputting T1 as 0. INT2

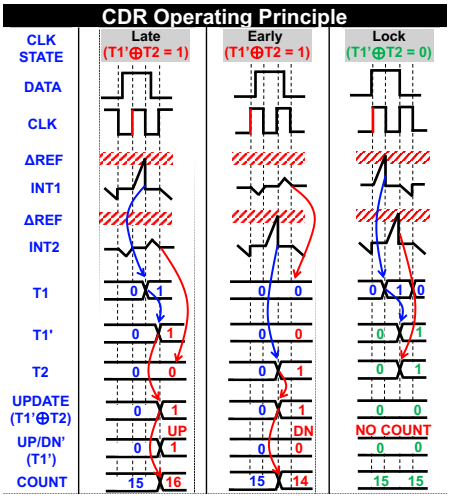

Fig. 6. CDR operating principle and timing diagram

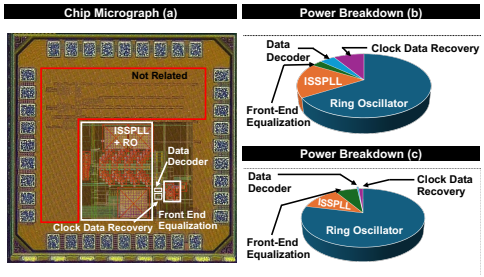

Fig. 7. (a) Chip micrograph, (b) power breakdown and (c) area breakdown of the implemented BR-HBC

integrates to the maximum amplitude and falls within the shaded area, outputting T2 as 1. This indicates that the clock is early. With this baud-rate CDR architecture, it is feasible to accurately determine the position of the clock edge relative to data without the need for data decoding. In essence, it functions similarly to a bang-bang CDR architecture without any oversampling. T1 and T2 are synchronized to generate the update and up/down signal to operate a counter which selects one of the 32 phases for data decoder.

III. Measurement Results

The body-resonance human-body communication receiver has been implemented in a 65nm CMOS process technology. Fig. 7 depicts the chip micrograph occupying $0.04mm^2$ of active area. The power and area distribution of the various components of the implemented IC are also presented.

A. On-Body Data Transmission

Transferring data through human body at a 50Mbps data rate with 100MHz OOK modulation requires a dedicated transmitter, which is beyond the scope of this paper. However, the channel characteristic can be verified using the testing setup shown in Fig. 8(a). The received signal is depicted in Fig. 8(b). This demonstrates the feasibility of data communication through the human body at a data rate of 50Mbps, which was previously unattainable using the EQS-HBC.

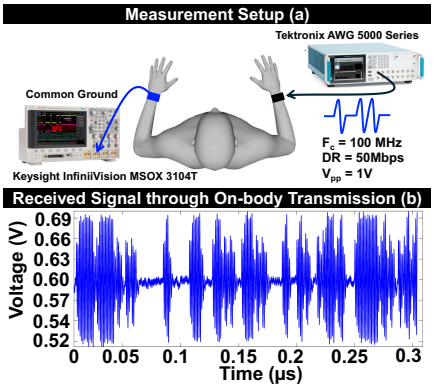

Fig. 8. (a) Measurement setup for on-body measurement and (b) measured received signal

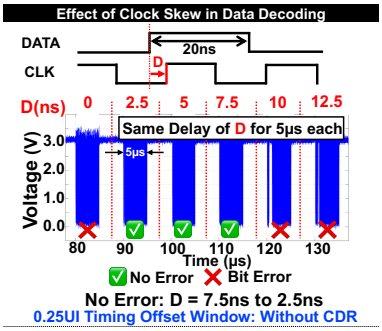

Fig. 9. Effect of clock skew on data decoding

B. Data Decoding with Clock Skew

Fig. 9 illustrates the impact of clock skew on data decoding to minimize the bit error rate (BER). In this experiment, the data has been delayed by $D(ns)$ for every $5\mu S$ period, with no data in between, to distinguish between the various cases for improved visibility. The delay has been determined by the time difference between the data edge and the clock edge.

As evident from the measured waveform, data reception is error-free when the delay is between 2.5ns and 7.5ns. The clock location, denoted as $D = 5ns$, corresponds to the midpoint of the clock state and the data bit. As previously outlined, this clock position yields the minimum bit error rate (BER), which is further corroborated by the measured results.

C. Clock Data Recovery

The integrated clock data recovery circuit has been subjected to various initial conditions. Fig. 10 illustrates the data decoder output when the CDR is operational. Initially, a 10 MHz reference clock was employed to stabilize the PLL operation frequency at 100 MHz. Subsequently, data was enabled, and the locking mechanism was tested. For the initial condition 1, the CDR required 7 data bits establish the clock position, while the second initial condition necessitated 10 bits.

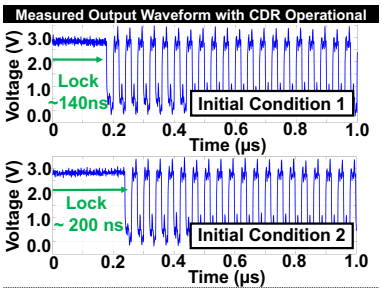

Fig. 10. Output waveform of the data decoder when the CDR is operational under different initial conditions.

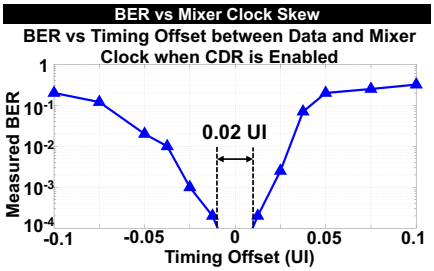

Fig. 11. Measured Bit Error Rate with the skew between the mixer local oscillator and data with CDR enabled

This is the first application-specific integrated circuit (ASIC) implementation for HBC receivers where clock data recovery has been demonstrated through silicon measurements.

D. BER vs Mixer Clock Skew

Fig. 11 illustrates the measured Bit Error Rate (BER) of the output data when the CDR is enabled while the delay between the data and mixer clock is varied. The data has been delayed using an AWG, and the CDR is provided with sufficient time to lock before measuring the BER at the output of the data decoder. As evident from the measurements, the bit error rate (BER) attains a value of 10^{-4} over a timing offset of 0.02 UI. Conversely, it reaches a value of 10^{-5} at optimal placement.

E. Power Comparison with state-of-the-art

The overall power consumption of the implemented human body communication (HBC) receiver is $227\mu W$. Excluding the clock generation, the front-end consumes only $35\mu W$. Fig. 12 compares all the HBC receivers without including clock generation. This is because some previous implementations of HBC receivers lacked clock generation topologies and a common comparison landscape is preferred.

This implementation is the first reported HBC receiver front-end to achieve the 1pJ/bit benchmark. The energy-efficient architecture of the data decoder, clock data recovery, and clock propagation enables an overall power consumption of only $35\mu W$. It is noteworthy that previous ASICs do not have silicon-operational clock-data-recovery modules in their architectures, and the clock has been manually placed to achieve the reported BER. Fig. 13 presents a comparative analysis of the performance of the implemented BR-HBC receivers with prior human body communication receivers.

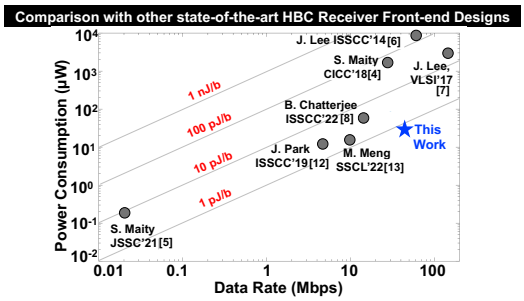

Fig. 12. Power comparison with other state-of-the-art HBC receiver front-end designs

	ISSCC'14 [6]	VLSI'17 [7]	CICC'18 [4]	ISSCC'19 [12]	JSSC'21 [5]	SSCL'22 [13]	ISSCC'22 [8]	This Work
Technology Node	65nm	65nm	65nm	65nm	65nm	65nm	65nm	65nm
Supply Voltage	1.1 V	–	1 V	0.6 V	0.5 V	0.6 V	0.75 V	1 V
Carrier Frequency	40-80 MHz	–	–	40 MHz	0.05 - 1 MHz	40-100 MHz	20 MHz	100 MHz
Data Rate (DR)	60 Mbps	100,150 Mbps	30 Mbps	5 Mbps	1-20 Kbps	10 Mbps	7.5-15 Mbps	50 Mbps
Modulation	Walsh Coding	NRZ	NRZ	OOK	OOK	PAM4	OOK + CPPM	OOK
Technique	Cap.	Cap.	Cap.	Mag.	Cap. EQS	Mag.	Adiabatic Switching	Body Resonance
Rx Power (w/o Clock Gen.)	–	2 mW	98 µW	6.3 µW	178 nW	13 µW	52.5 µW	35 µW
Rx Power (w Clock Gen.)	9.02 mW	–	–	24 µW	–	27 µW	60.6 µW	227 µW
Rx Energy Eff. (w/o Clock Gen.)	–	16.6 pJ/b	3.27 pJ/b	1.26 pJ/b	8.9 pJ/b	1.3 pJ/b	3.5 pJ/b	0.7 pJ/b
Rx Energy Eff. (w Clock Gen.)	150 pJ/b	–	–	4.8 pJ/b	–	2.7 pJ/b	4 pJ/b	4.5 pJ/b
Measured BER	10^{-5}	10^{-6}	10^{-3}	10^{-3}	10^{-3}	10^{-3}	10^{-3}	10^{-5}
Total Active Area	1.05 mm^2	0.02 mm^2	0.12 mm^2	0.12 mm^2	0.17 mm^2	0.8 mm^2	0.19 mm^2	0.04 mm^2
CDR Shown in Measurement	No	No	No	No	No	No	No	Yes

Fig. 13. Comparison with other state of the art HBC receiver front-ends

IV. Conclusion

Body-Resonance (BR) extends the capabilities of data transmission through the human body by utilizing the wider bandwidth and lower insertion loss near the resonance peak. This technology enables the BR-human body communication receiver to achieve a data rate of 50Mbps and demonstrate an energy efficiency of 0.7pJ/bit. Additionally, a novel integrating clock data recovery module has been employed to optimize the clock placement, resulting in a BER of 10^{-5}.

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