Scaled Vertical Transport Gate-All-Around Nanostructured Channel (Nanosheet/Nanowire) Technology for Advanced CMOS Devices.

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***Abstract*— This study explores a Gate-All-Around (GAA) architecture for 3nm and below nodes, introducing Vertical Transport (VT) GAA devices with nanostructured channels. We compare nanowire (NW) and nanosheet (NS) configurations, showcasing electrical performance, 3D logic cells, and design perspectives. Making the link from technology parameters to design performance metrics in a DTCO approach, we show that the VT-NS-FET device outperforms VT-NW-FETs and FinFETs, achieving up to 50x improvement in terms of Energy-Delay Product (EDP) and up to 1.5x improvement in terms of footprint. At the circuit level, we also demonstrate a 7x footprint reduction of the VT-NS-FET implementation of a 2-input XOR gate over a FinFET implementation, and a 2.8x reduction in output branch resistance over a VT-NW-FET implementation.**

Keywords*— *Gate-All-Around transistor, Vertical Transport, Nanosheet FET, Energy-Delay Product, Design-Technology Co-Optimization (DTCO)

I. Introduction

The Gate-All-Around (GAA) architecture is anticipated to replace the FinFET architecture for the 3nm node and below [1], with the aim of enhancing the device's drive current capability, improving channel control, reducing leakage currents, and lowering dynamic power. The Vertical Transport (VT) GAA device (Fig. 1) presents significant opportunities for denser devices by minimizing the contact pitch and leveraging the 3D configuration to alleviate congestion at the routing level. However, only a few hardware demonstrations of the device have partially shown

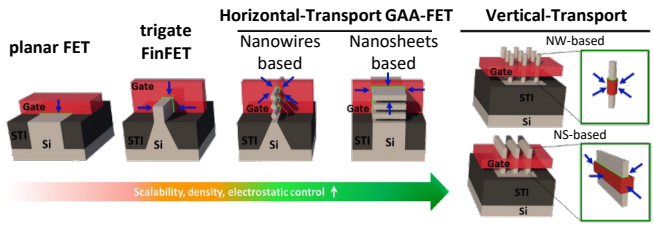

Figure 1: Device architectures evolution enabling the CMOS scaling: from planar to vertical nanostructured channel FETs.

its potential [2]-[4], as they are still limited in gate length scaling and 3D contact assessment. In this work, we demonstrate a process route that integrates sub-20 nm vertical GAA devices with nanostructured channels, allowing for a comparison of device performance based on nanowire and nanosheet configurations, including electrical comparisons, demonstration of 3D logic cells, and perspectives with advanced scaled design rules.

II. VT-FET TECHNOLOGY

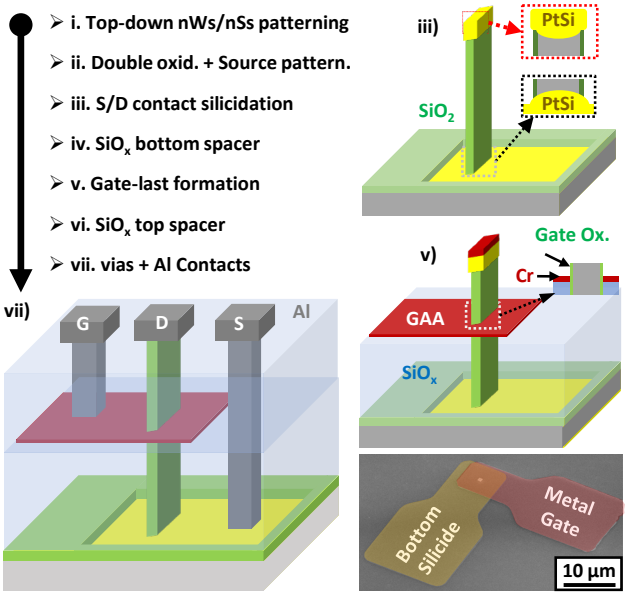

Figure 2: Process-flow of the fabrication of VT-FETs with schematic illustrations and SEM view after step v (bottom right).

Unlike the conventional gate-first approach employed in planar transistor fabrication, we developed a gate-last approach to craft nanoscale GAA (Lg~18nm) transistors in a vertical configuration, applicable to both nanowire and

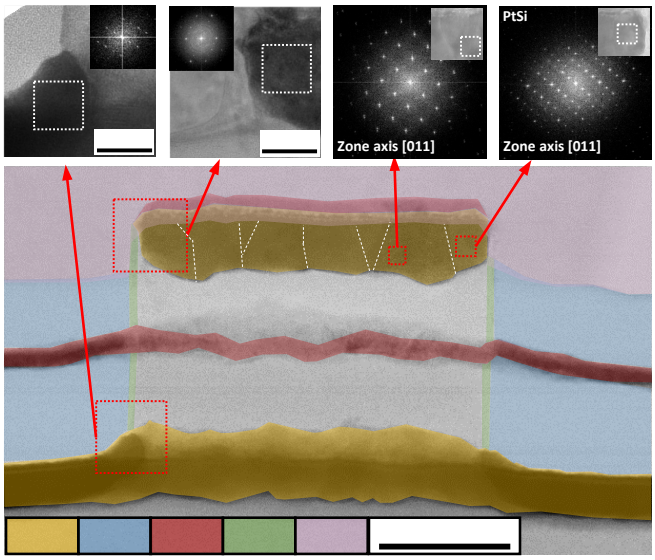

Figure 3: Cross-sectional TEM observation of a vertical nanosheet device. FFT images above demonstrate the crystallinity of the PtSi silicide.

nanosheet channel designs. The key fabrication steps (see Fig. 2) involve patterning the vertical nanostructured channel and gate-all-around material, engineering source/drain contacts, and implementing vertical spacer technology. The highly doped Si channel (4E19 at.cm-3) enables the creation of junction-less transistors, eliminating the need for complex highly doped junctions in vertical nanostructured channels. The patterning of the metal layer is based on a liftoff-free approach [5] We introduce a two-step oxidation process: (i) to pattern the bottom access lines in the field oxide (light green), and (ii) for local removal at the extremities of the gate oxide (dark green) of 4 nm to create identical silicided source/drain contacts. Fig. 3 presents the XTEM of an 18 nm GAA VT-NS junction-less device with symmetrical silicided S/D contacts, highlighted by the FFT of PtSi phase.

III. VT-FET ELECTRICAL CHARACTERISTICS

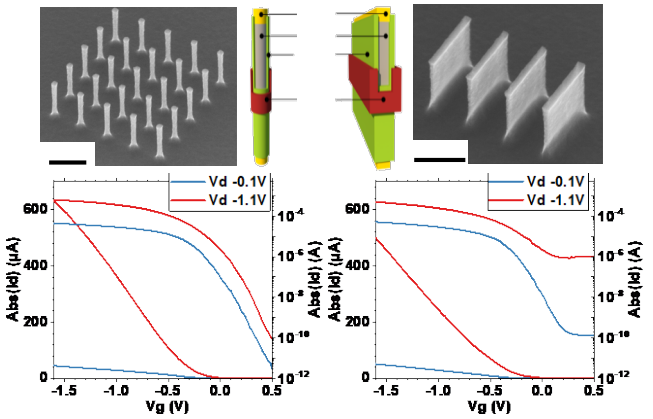

Figure 4: Comparison of nW-based (left) and nS-based (right) VT-FET with tilted SEM view before silicidation with static Id-Vg characteristics.

Fig. 4 presents examples of measured ID-VG curves for both channel configurations. Various figures of merit for NS- and NW- devices are displayed in Fig. 5 based on their width/diameter. As expected, immunity against short-channel effects (SS and DIBL) for the same 18 nm gate length is better with the NW configuration than the NS configuration due to higher electrostatic control of the gate. However, in both cases, the Ion/Ioff ratio can reach up to 5 decades. Notably, the variation of VT with the dimension follows the same trend. Finally, the technological capability to route the signal at the bottom level of the contacts is a key advantage of this proposed technology. It allows for the creation of small logic gate demonstrators, as highlighted in Fig. 6 where we demonstrate the first 2-input p-only logic cell (NAND) based on VT-NST.

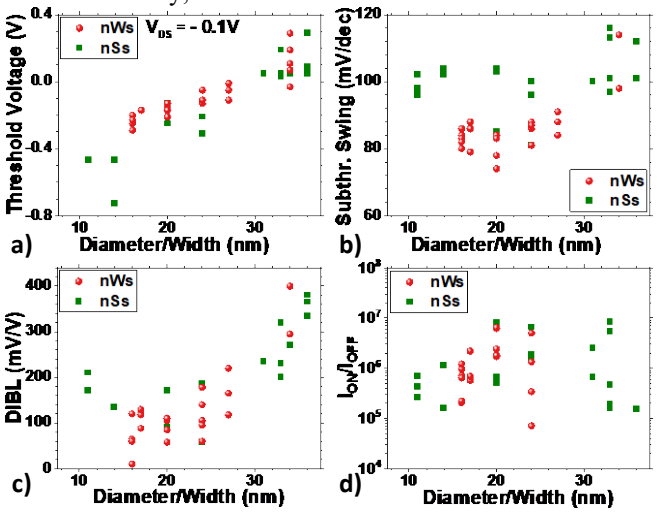

Figure 5: Comparison of VT-FETs with different nW/nS dimensions: a) Threshold voltage at Vd = -0.1 V; b) Subthreshold Swing at Vd = -1.1 V; c) DIBL at Vd = -1.1 V; d) I_{ON}/I_{OFF} at Vd = -1.1 V.

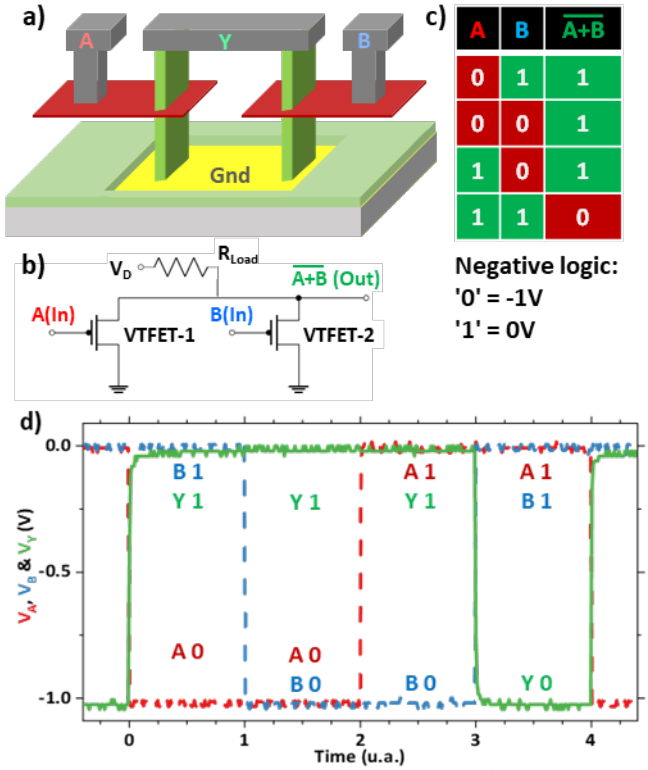

Figure 6: Schematic (a) and electrical diagram (b) of a passive NAND fabricated with two nS-VT-FETs. Truth table is visible in (c); A, B inputs and A + B outputs are shown in (d).

IV. DESIGN PERSPECTIVES WITH SCALED DESIGN RULES

In this section, we consider device- and circuit-level comparisons of the VT-NS-FET with respect to equivalent devices based on vertical nanowires (VT-NW-FET) and lateral fins (FinFET). While both vertical configurations are expected to lead to improved density (particularly for multiple gate stacking) over lateral structures, vertical nanosheet designs benefit from another key advantage over both nanowire- and fin-based devices, since their channel dimensions can be modified in a continuous design space (akin to broad nFET-pFET width) rather than the now-conventional discrete design space typical to conventional nanowires or fins. Also, nanosheet structures are generally easier to fabricate and control compared to nanowires, especially when it comes to achieving uniform dimensions and consistent performance across multiple stacked layers.

A-Device-level comparison

At this level, a meaningful metric is the Energy-Delay Product (EDP) which captures both energy-efficiency and computation speed. EDP is computed as CL2VDD3 / Isat, where: CL represents the load capacitance of the device, taken to be equal to the input gate capacitance CG of an identical device; VDD the supply voltage; Isat saturation on-current. EDP comparisons between devices can be established considering (i) equivalent device drive strength

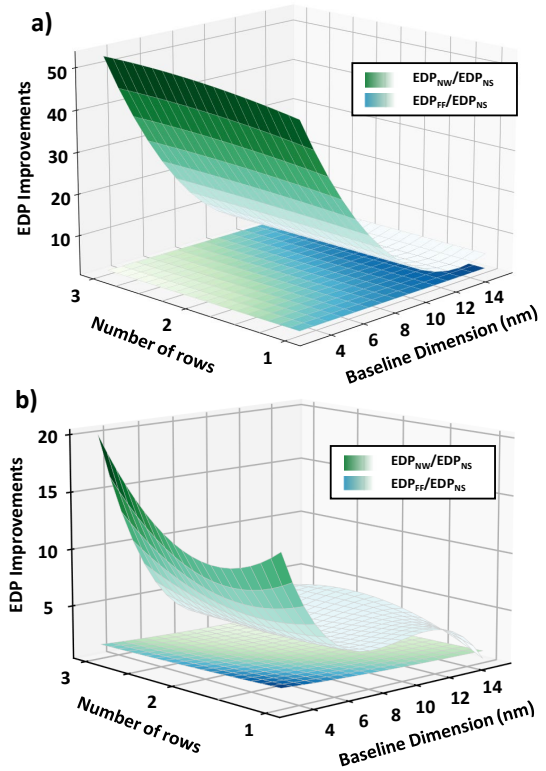

Fig.7: Comparisons between VT-NS-FETs (NS) as compared to VT-NW-FETs (NW) and FinFETs (FF) over a range of base dimension values (fin width w_f, nanowire diameter $2r_v$, nanosheet width W_2) from 3 nm to 15 nm, and over a range of number of rows from 1 to 3. EDP gain evaluated for equivalent drive strength as EDP_{NW}/EDP_{NS} and EDP_{FF}/EDP_{NS} (a) and for equivalent footprint as EDP_{NW}/EDP_{NS} and EDP_{FF}/EDP_{NS} (b).

or (ii) equivalent footprint and are independent of supply voltage.

For equivalent device drive strength comparison: We start with a baseline FinFET [6] of specific dimensions (height hf = 108 nm and width wf = 7 nm) thus considering an equivalent conductive area of 2hf+wf. We consider fin width wf to be the baseline dimension and therefore set nanowire diameter 2rv and nanosheet width W2 equal to wf. We then compute, using geometric expressions for drain on-current, the necessary number N of nanowires and the necessary nanosheet depth W1 such that device drive strength is identical. Geometric and material parameters (including spacers) are then used to compute device gate capacitance CG and ultimately the EDP comparisons.

For equivalent footprint comparison: We again take as baseline footprint the FinFET device up to source and drain contacts. We then design nanowire- and nanosheet-based devices by finding N and W2 such that the devices occupy an identical lateral footprint. We then compute Isat and gate capacitance CG for these dimensions, and calculate the EDP comparisons.

Discussion: Fig. 7 highlights that NS is superior both in terms of EDP (up to 50x improvement) and of footprint (up to 1.5x improvement) as compared to NW and FinFET. Indeed, as compared specifically to the VT-NW-FET, the VT-NS-FET can provide a larger effective channel width, resulting in higher drive current per footprint, since nanosheets have a wider cross-sectional area than cylindrical nanowires, allowing for more current flow. Further, the GAA structure of nanosheet transistors provides better control over the channel compared to nanowires, and this enhanced control leads to improved performance and reduced short-channel effects.

B-Circuit-level comparison

The physical design of logic cells from elementary devices implies the use of 3D wiring to achieve a minimal footprint with corresponding on-power/performance metrics due to

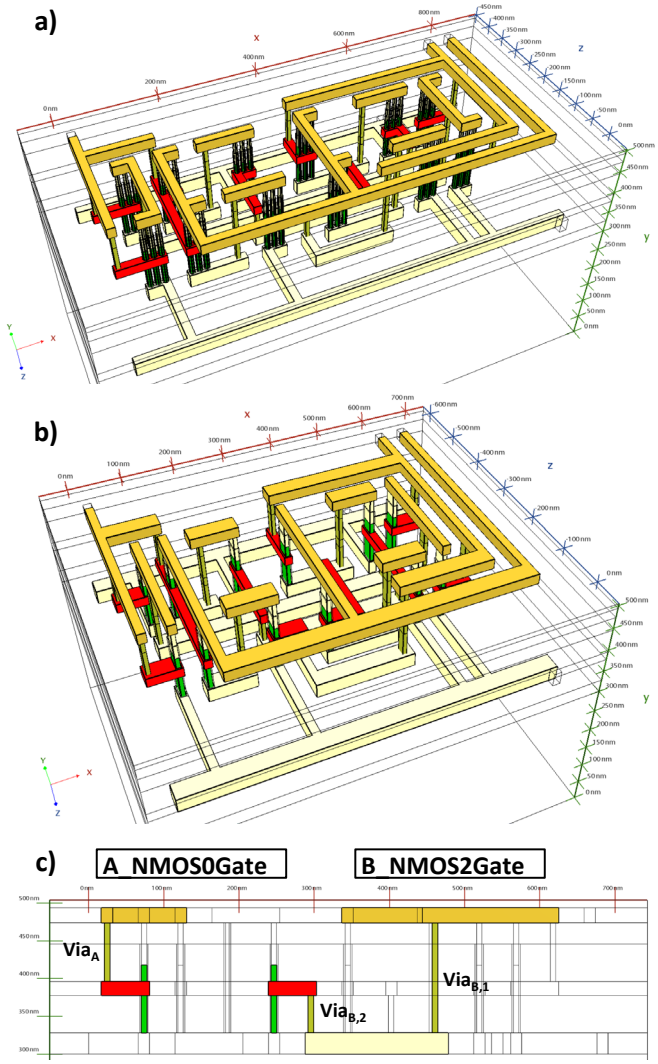

Fig. 8: Two-input XOR designed using TCAD-based physical design tools (GTS Cell Designer). (a) 3D view of VT-NW-FET implementation using 2 rows of 3 parallel nanowires (b) 3D view of VT-NS-FET implementation using 1 rows of nanosheets (c) side view of the XOR with 1 NS transistor configuration (green) highlighting the resistance path from inputs A (left) and B (right) to the gates (red). With vertical stacking of all three device terminals, it is straightforward to achieve a reduced footprint from a device perspective alone, and this is propagated to the circuit level as long as routing planes are clearly identified (e.g. one layer for power rails – here on the lowest metal layer, another for data input/output, as well as any clock and/or configuration inputs – here on the topmost metal layer).

the minimized parasitic resistances and capacitances both within and between logic cells. Based on the design and technology specifications, we generate the layout of an XOR2 gate, a critical Boolean logic operator in the context of mathematical computations heavily used in AI such as matrix-vector multiplication in convolutional neural networks and distance estimation in associative search. We used an existing open-source tool [7] available as a satisfiability modulo theories (SMT)-based many-tier

vertical device standard cell (SDC) synthesis framework that provides minimum-sized cell layouts by performing concurrent P&R of FETs. This prior work relies on horizontal/vertical relative positioning constraints and a dummy gate control scheme to model the cell architecture. It also uses efficient objective functions for pin-accessibility as well as limiting the use of vertical routing, due to higher resistance. The tool was extended and enhanced with a Python script to adapt the approach to the considered technologies. Fig. 8 shows 3D views of an example 2-input XOR gate implemented with VT-NW-FETs and VT-NS-FETs. We then used the automatic 3D parasitic extraction (PEX) tool integrated within the device solver Minimos-NT [8] to obtain the full SPICE netlist of the XOR2 cell including parasitics.

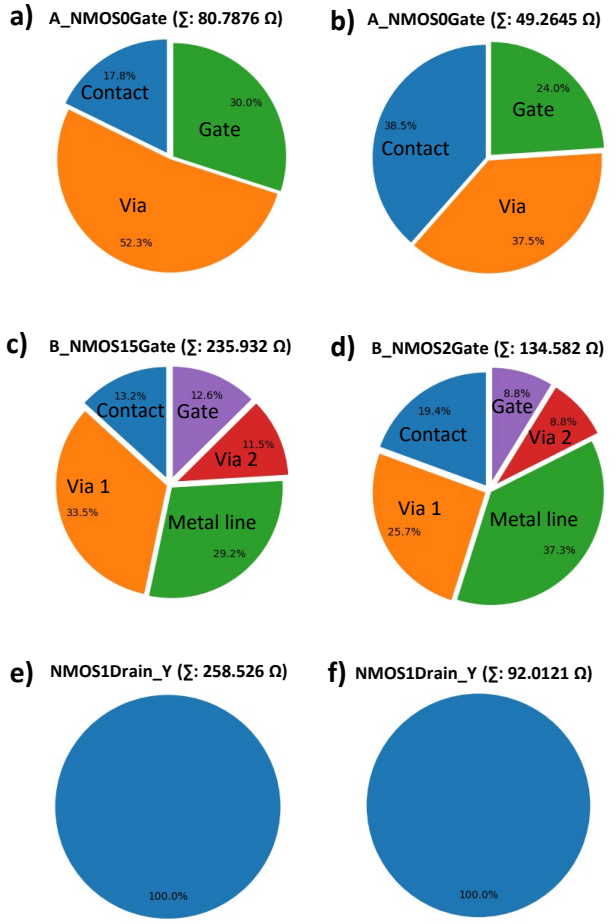

Fig. 9: Resistance breakdown for the two-input XOR gate of Fig. 8. (a) (c) (e) Resistance breakdown to pull-down inputs A, B and output Y for the VT-NW-FET implementation (b) (d) (f) Resistance breakdown to pull-down inputs A, B and output Y for the VT-NS-FET implementation.

Discussion: The generated layout enables direct comparisons in terms of footprint (Table I). We considered the SLT (Super Low Threshold) cases in the 7 nm FinFET library since the saturation current values are closest to the explored vertical cases, and compared with respect to the 1x variant (3 fins per cell). The area gains are around 7X for the VT-NS-FET and around 6X for the VT-NW-FET. We also considered the impact of the parasitic network (resistance and capacitance) on the EDP. While we see slight parasitic capacitance improvements of VT-NS-FET implementations over VT-NW-FET implementations corresponding to the slightly lower area, the main improvement originates from the reduction in parasitic resistance. In Fig. 9 we show the breakdowns in resistance values for inputs A, B and outputs Y considering the pull-down network in the gates in both VT-NW-FET and VT-NS-FET cases. In particular, it is worth noting that the resistance from the output transistor drain terminal to the output is all silicide. Consequently, this output resistance is approximately 2.8x higher in the NW implementation as compared to that of the NS implementation.

Cell	w (µm)	h (µm)	Area (µm²)	Area gain wrt XOR2x1
XOR2x1_ASAP7_75t_SL	2.59	1.08	2.80	-
XOR_NS_1	0.69	0.57	0.39	7.09
XOR_NW_1	0.77	0.57	0.44	6.41

Table I: XOR cell size (width w, height h) and relative area gain of the VT-FET implementation for nanosheet and nanowire transistors as compared to the 7 nm FinFET library.

V. CONCLUSION

We proposed a process route compatible with both vertical NW and NS configuration with scaled GAA and silicided top and bottom S/D contacts enabling to compare their electrical performance, 3D logic cells, and design perspectives. In both EDP and footprint at the device level, the efficiency of VT-NS-FET is highlighted compared to NW and FinFETs, achieving up to 50x improvement in terms of EDP and up to 1.5x improvement in terms of footprint. Further gains are achieved at the circuit level, showcasing a 7x footprint reduction (and consequent parasitic capacitance reduction) of the VT-NS-FET implementation of a 2-input XOR gate over a FinFET implementation, and a 2.8x reduction in output branch resistance over a VT-NW-FET implementation.

ACKNOWLEDGEMENTS

This work was supported by the EU H2020 FVLLMONTI project (N◦101016776) and Renatech French network.

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