A 152fs$_{rms}$ Ring-VCO-Based Injection-Locked PLL Using Multi-Phase Injection with Injection Timing and Pulsewidth Calibration

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***Abstract*—This paper introduces an injection-locked phase-locked loop (ILPLL) with multi-phase injection and background self-calibrated. By employing multi-phase injection to enhance injection strength, the noise suppression bandwidth is extended and thus achieving low jitter. Moreover, with injection timing and pulsewidth calibration, the noise suppression bandwidth is further improved, while achieving low spur. The proposed ILPLL is fabricated in a 28-nm CMOS, achieving 152 fs RMS jitter with -66.5 dBc spur and -247.4 dB FoM$_{jitter}$ at 2.4 GHz working frequency. The total power consumption is 7.8 mW from 0.9 V supply voltage.**

***Keywords*—multi-phase injection, ILPLL, ring oscillator, self-calibrated injection pulse**

I. Introduction

Ring voltage-controlled oscillator (RVCO)-based phase-locked loops (PLLs) have gained widespread adoption in system-on-chip (SoC) applications due to their wide tuning range, compact footprint, and multiphase output capability [1-2]. However, the inherent poor phase noise performance of RVCOs impose significant limitations on further applications in high-data-rate wireline communication systems [3-6]. Extending the loop bandwidth is an effective methodology for suppressing the phase noise of RVCOs, but at the expense of potential stability degradation [7]. Recently, injection-locked phase-locked loops (ILPLLs) have attracted considerable attention for achieving extremely low jitter by periodically clearing accumulated jitter [8-14]. For ILPLLs, optimal jitter can only be obtained when the injection pulse is completely aligned with the oscillator and the pulsewidth reaches optimum. [9] proposed an ILPLL incorporating both injection timing and pulsewidth calibration, as shown in Fig. 1(a). However, the calibration process is time-consuming, requiring 35μs to stabilize, which makes it difficult to achieve real-time background calibration. To achieve real-time optimization of pulsewidth and eliminate injection phase deviation, an adaptive pulsewidth adjustment combined with phase-error cancellation technique is introduced in [10], as illustrated in Fig. 1(b). While this approach achieves low jitter through pulsewidth optimization and complementary injection, the replication-based methodology introduces additional power. Moreover, although the complementary pulse injection scheme can enhance injection strength and improve jitter performance, the wide-pulse would disturb the zero-crossing points in the injection-adjacent edges, consequently degrading the spur performance.

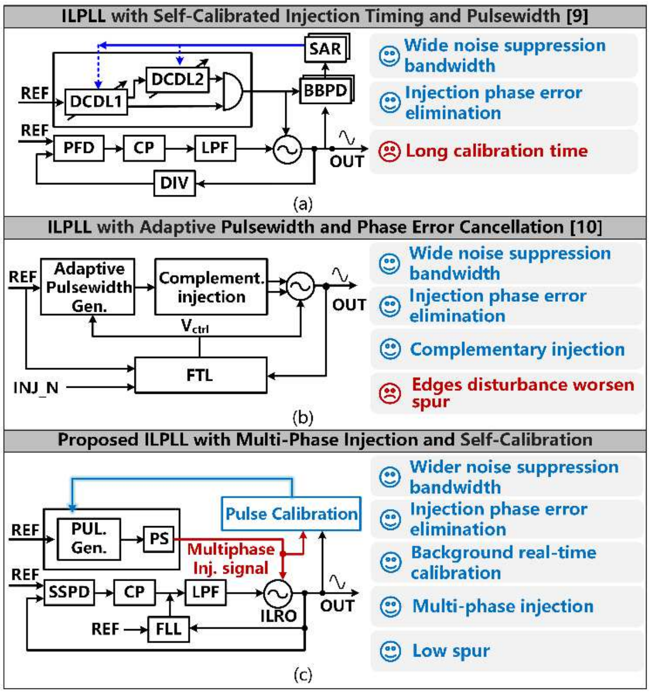


Fig. 1. Comparison of different ILPLLs.

To address these challenges, we propose a multi-phase injection ILPLL with pulse timing and width co-calibration, as shown in Fig. 1(c). The multi-phase injection technique boosts injection strength, which widens noise suppression bandwidth and consequently reduces jitter. Compared to conventional approaches that rely on increasing injector sizes to enhance injection strength, the proposed distributed multi-node small size injection scheme can effectively reduces reference spur while maintaining unrestricted operating frequency. In addition, the proposed calibration technique effectively eliminates the phase misalign across varying operating conditions while maintaining optimal injection pulsewidth.

II. Proposed Architecture

Fig. 2 depicts the detail of the multi-phase injection ILPLL, which consists of an injection path, two pulse calibration paths, a sub-sampling phase-locked loop (SSPLL), and a frequency-locked loop (FLL). In the injection path, digital-controlled delay line (DCDL1) is used for control the

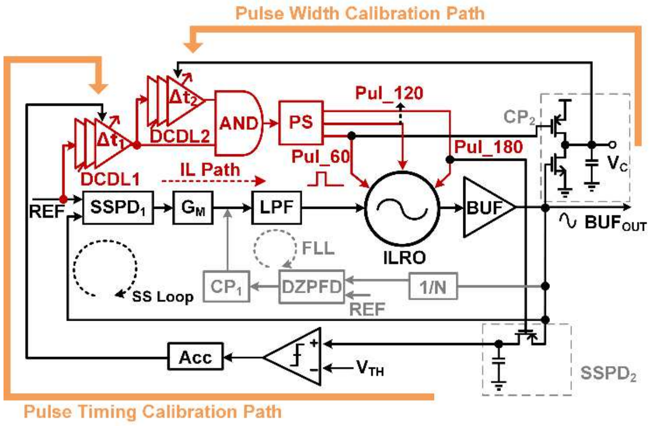


Fig. 2. The proposed multi-phase injection ILPLL.

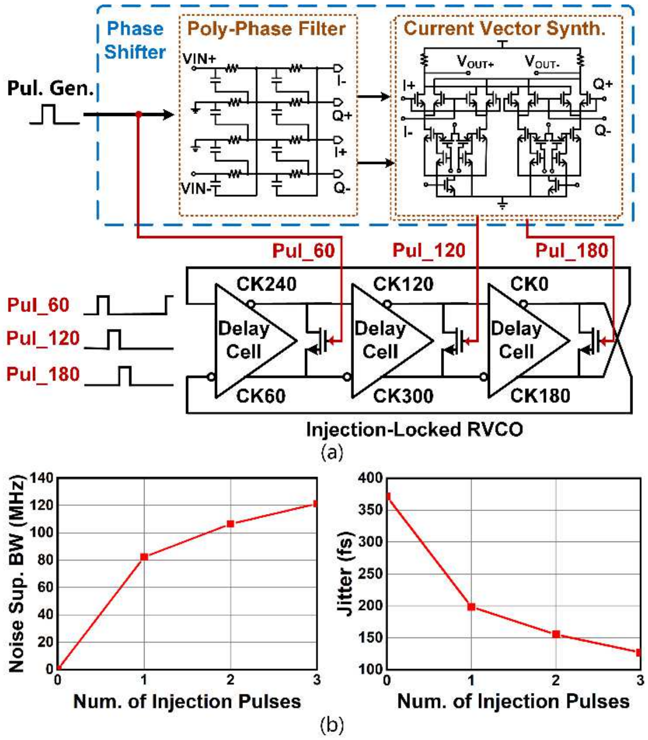


Fig. 3. (a) Principle of the multi-phase injection. (b) Simulated noise suppression bandwidth and jitter under different injection pulse numbers.

injection timing of the injected pulses, while DCDL2 is utilized to adjust the pulsewidth. The phase shifter (PS) consists of poly-phase filter (PPF) and current vector synthesizer, that generates two signals with 60° phase difference from the generated pulses. The background self-calibration circuits controls pulse timing and width to improve the injection strength, thus eliminating jitter and reducing reference spur.

A. Multi-Phase Injection

To extend the noise suppression bandwidth of ILPLL for improved jitter performance, a multi-phase injection technique is proposed in this work. Fig. 3(a) depicts the multi-phase injection injection-locked ring oscillator (ILRO) composed of three-stage pseudo-differential delay cells and three injectors. The PS employs the vector synthesis structure, where the PPF generates I/Q signals and then vectorially summed by Gilbert cells. By synchronously injecting the three pulses with 60° phase difference into ILRO, the injection strength is enhanced and noise suppression bandwidth is extended consequently. Fig. 3(b) demonstrates noise suppression bandwidth and jitter before and after applying the proposed multi-phase injection scheme. The simulation results indicate that maintaining optimal pulsewidth while increasing the number of injection pulses achieves greater than 30% enhancement in noise suppression bandwidth and more than 50% reduction in jitter.

It is noteworthy that any deviation from the nominal 60° phase difference among the three injection pulses will reduce the noise suppression bandwidth, consequently degrading the jitter performance. The phase shift error in our PS is less than 0.9° which effectively minimizes its impact to jitter. This low mismatch limits variations in the noise suppression bandwidth within 5%, thereby ensuring the ILPLL preserves excellent jitter performance and spur suppression.

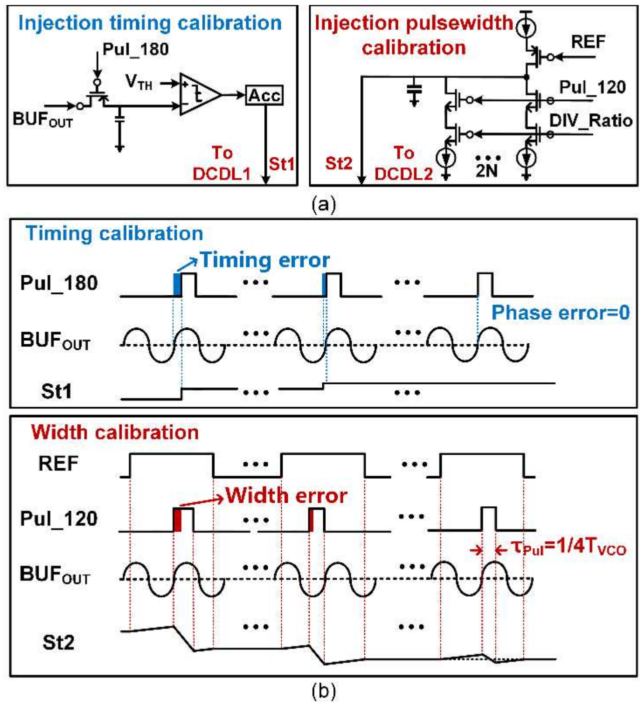
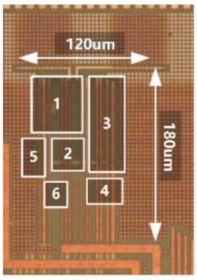


Fig. 4. (a) Calibration circuit. (b) Timing diagram of injection timing and pulsewidth calibration.

B. Injection Timing and Pulsewidth Calibration

For eliminate phase misalignment between injection pulses and the oscillator while achieving optimized pulse-width for further extending noise-suppression bandwidth, an injection timing and pulsewidth co-calibration circuit is employed. As illustrated in Fig. 4, the calibration circuit is divided into two parts: injection timing calibration and pulsewidth calibration.

The injection timing and pulsewidth can be independently controlled by adjusting the delay values of DCDL1 and



Power Consumption (mW)		
1	ILRO+BUF	5.6
2	$SSPD_1+G_M$	0.9
3	LPF	0
4	FLL	0.6
5	DCDL1+DCDL2+PS	0.3
6	Calibration Circuit	0.4
	Total	7.8

Fig. 5. Die photograph and power breakdown.

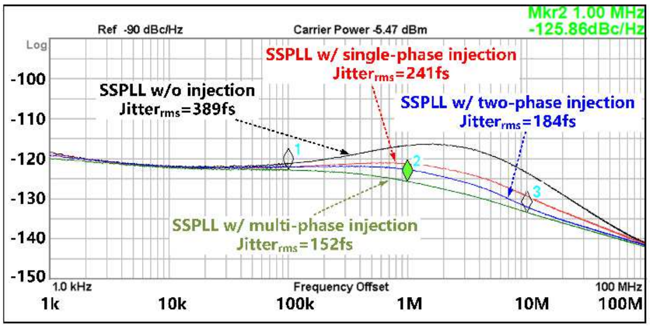


Fig. 6. Measured phase noise and RMS jitter.

DCDL2 in the pulse generator, respectively. In injection timing calibration, when the rising edge of Pul_180 is misaligned with the zero-crossing of BUF_{OUT}, an error voltage is generated by $SSPD_2$. The error signal is subsequently quantized by a comparator and accumulator (Acc), generating control code St1 that dynamically adjusts the delay of DCDL1. When the injection timing is aligned, the output of $SSPD_2$ becomes zero, and the control signal produced by the Acc no longer changes. The calibration timing diagram is shown in Fig. 4(b). In injection pulsewidth calibration, when the pulsewidth deviates from the optimal value ($1/4T_{VCO}$), CP_2 performs charging and discharging to generate a pulse width error signal. This fluctuation is converted to St2 for adjusting the delay of DCDL2. To achieve optimal pulsewidth, the CP_2 must maintain 1:2N current ratio between its sourcing and sinking branches, N is division ratio. The majority of calibration circuits employ digital and passive components with low power consumption of 0.4 mW.

III. Measurement Results

The proposed ILPLL is fabricated in the 28-nm CMOS process. Its die photograph is shown in Fig. 5, which occupies a core area of 0.022 mm^2. The reference clock is 100 MHz, supplied by R&S SMA100B signal generator. The phase noise and spectrum is measured by Keysight N9030A. The ILPLL consumes 7.8 mW power from a 0.9 V supply when operating at 2.4 GHz, with RVCO dominating the power budget at 60% of total consumption.

Fig. 6 shows the phase noise and jitter measured under different injection conditions. Compared to conventional single-phase scheme, the proposed multi-phase injection

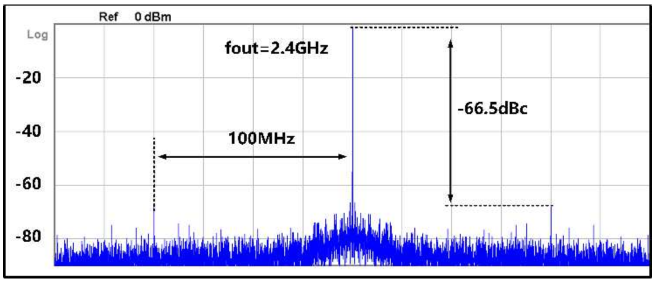


Fig. 7. Measured spectrum.

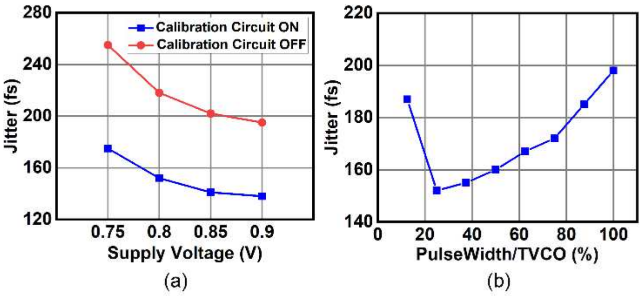


Fig. 8. Measured jitter under different (a) supply voltage; (b) pulsewidth.

technique can reduces the phase noise from -121.2 dBc/Hz to -125.8 dBc/Hz at 1 MHz offset, and the jitter integrated from 1 k to 100 MHz under four different injection conditions is 389 fs, 241 fs, 184 fs, and 152 fs, respectively. The measured spectrum presented in Fig. 7 demonstrates a reference spur of -66.5 dBc. This low spur confirms the effectiveness of the calibration circuit in suppressing phase misalignment between the injection signal and oscillator.

Fig. 8(a) shows that the proposed calibration circuit can ensure the proposed ILPLL maintains optimal jitter performance at different supply voltages. Fig. 8(b) verifies the effect of different injection pulsewidths on jitter. It can be seen that although the injection pulse is aligned with oscillator, the changing pulsewidth of the injection signal still leads to jitter degradation of over 30%.

The performance summary and the relevant prior state-of-the-art PLLs is listed in Table I. Thanks to the proposed multi-phase injection and calibration technique, the implemented ILPLL achieves the lowest RMS jitter and spur at a competitive power consumption, thus obtaining the best FoM_{jitter}.

IV. Conclusion

A low jitter ILPLL with multi-phase injection and injection pulse self-calibrated is proposed in this work. The multi-phase injection technology can expand the noise suppression bandwidth, thereby achieving low jitter. In addition, by injecting timing and pulsewidth calibration, the noise suppression bandwidth is further improved and the reference spur is reduced. The fabricated ILPLL achieves a state-of-the-art FoM_{jitter} of -247.4 dBc/Hz.

TABLE I. PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART ILPLL.

	This Work	X. Jin JSSC'20 [9]	B. Liu SSCL'20 [11]	S. Yoo JSSC'21 [3]	Z. Wang JSSC'25 [10]	Y. Cho JSSC'25 [14]
Technology (nm)	28	28	5	65	28	40
Architecture	ILPLL	ILPLL	ILPLL	ILCM	ILCM	MDLL
Oscillator Type	Ring	Ring	Ring	Ring	Ring	Ring
Fractional-N	No	No	Yes	No	No	No
Supply Voltage (V)	0.9	1.0	0.75	1.1	0.9	1.0
Reference Freq. (MHz)	100	125	100	100	3000	120
Output Freq. (GHz)	2.40	4.00	1.00	2.40	6.00	12.24
Divider Ratio N	24	32	10	24	2	102
PN@1MHz (dBc/Hz)	-125.8	-112.3	-120.2	-129.0	-128.6	-116.5
RMS Jitter (fs)	152 (1k-100MHz)	710 (10k-30MHz)	740 (10k-10M)	140 (1k to 30MHz)	43.9 (1k to 100MHz)	122 (1k to 100MHz)
Total Power (mW)	7.8	11.4	0.52	11	14.5	14.7
*FoM_{jitter} (dB)	-247.4	-232.4	-245.5	-246.7	-255.5	-246.6
**FoM_N (dB)	-261.2	-247.4	-255.5	-260.5	-258.5	-266.7
Reference Spur (dBc)	-66.5	-61.6	-30.9	-72	-59	-60
Core Area (mm^2)	0.022	0.090	0.003	0.055	0.133	0.066
Injection Timing	Self-Calibrated	Self-Calibrated	-	Self-Calibrated	Self-Calibrated	Self-Calibrated
Injection Pulsewidth	Self-Calibrated	Self-Calibrated	-	-	Adaptive Adj.	-
*FoM_{jitter}=20log$_{10}$(jitter/1S)+10log10(Power/1mW) ** FoM_N=FoM+10log10(1/N), Normalized to N.						

ACKNOWLEDGMENT

This work was supported in part by the National Natural Science Foundation of China under Grant 62204205, in part by the Postdoctoral Fellowship Program of China Postdoctoral Science Foundation under Grant GZC20233508.

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