RingAmp-based Area-efficient 500MSa/s Fully Differential Switched Capacitor Filters in 65nm CMOS

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***Abstract*—This work proposes a generalized fully differential filter design technique using a modified Ring-Amplifier (MRA) for any switched capacitor filter (SCF). A RingAmp-based fully differential integrator (RAI) is proposed to enable the use of MRA in SCF design. The MRA-based prototype 3-pole lowpass filter (LPF) and 4-pole bandpass filter (BPF) are implemented in 65nm CMOS technology operating at 1V supply. The LPF accurately achieves 20MHz bandwidth at 500MSa/s, dissipating 3.4mW occupying 0.043mm^2 area. The BPF accurately achieves 1.6MHz center frequency and 0.8MHz bandwidth at 200MSa/s dissipating 4.36mW while occupying 0.069mm^2 area. The simplicity and scalability of MRA enable high-frequency SC filter operation.**

***Index Terms*—Filter, integrator, RingAmp, switched-capacitor.**

I. Introduction

Switched-capacitor filters (SCF) have been actively researched in the last few decades starting with seminal works in [1]–[3]. The SCFs have been demonstrated with robust performance over process, voltage, and temperature (PVT) variations using ratioed capacitors matched to 0.1% accuracy for precision frequency response. The precision SC filter implementation avoids extra trimming and calibration circuits. Conventional SCFs are implemented using an opamp-based switched-capacitor (SC) integrator. As shown in Fig. 1(a), the SC integrator uses two non-overlapping clock phases $\phi_{1,2}$ and early clock phases $\phi_{1A,2A}$ to mitigate signal-dependent charge-injection. The non-inverting input V_{IN1} and the inverting input V_{IN2} are sampled at ϕ_1 and ϕ_2 clock phases, respectively. The virtual ground at the inverting input of the opamp removes the effect of the parasitic capacitance of the sampling capacitor C_I. For accurate frequency response, the opmap UGF should be 20 times higher than the sampling frequency (f_s). Therefore, the conventional opamp-based SC integrator suffers from higher power consumption as we increase f_s. The opamp gain decreases with technology scaling as the transistor intrinsic gain reduces, making precision filter design challenging in deep sub-nanometer CMOS.

Switched-current (SI) integrators are reported in the literature for high-frequency current-mode filter design [4]. The integrator constant of SI integrators is dependent on transistor matching and, hence, sensitive to mismatches. Discrete-time charge-sharing based IIR (CS-IIR) filter presented in [5] achieves high bandwidths up to 13.3MHz. However, the absence of a closed-loop amplifier makes the filter response sensitive to the PVT variations and capacitor parasitics.

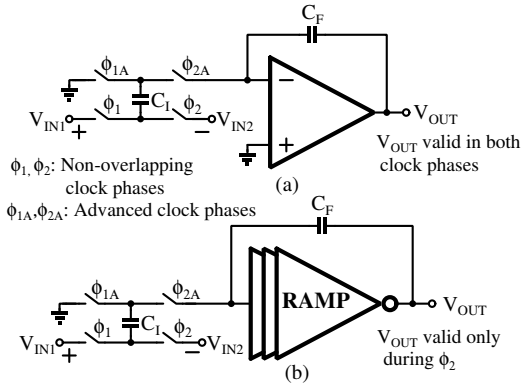

Fig. 1. Single-ended representation of (a) opamp-based SC integrator, and (b) proposed RAMP-based SC integrator.

In this work, we propose to replace the opamp in conventional SC integrators with a Ring amplifier (RAMP) to enable precision high-frequency filter design, as shown in Fig. 1(b) (a single-ended representation is shown for simplicity). In recent state-of-the-art (SOTA), the RAMP is demonstrated in analog-to-digital converters (ADC), which alleviates the aforementioned fundamental challenges in conventional opamps while achieving high linearity [6]. The RAMP is an inverter-based dynamic amplifier that uses a reset phase (to set the input common-mode voltage) and an amplification phase. During the amplification phase, the RAMP dynamically modifies UGF for initial fast slewing followed by output stabilization, providing a good phase margin in the steady state condition [7]. The RAMP does not require a high quiescent current for slewing, and it has both PMOS and NMOS contributing to the effective transconductance, making it power efficient than opamps [8]. Here, we note that the RAMP output is valid only during the amplification phase (ϕ_2 in Fig. 1(b)).

The fundamental challenge of incorporating RAMP in SCF is that the RAMP output is valid in only one clock phase.

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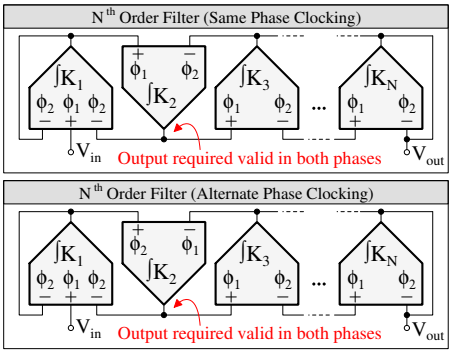


Fig. 2. Conventional SCF with integrator outputs valid in both the clock phases. Integrator K_1 and K_3 sample the K_2 output in ϕ_2, and ϕ_1, respectively.

To overcome this, we present a RAMP-based SC integrator (RAI) that can sample input in either clock phase, enabling the use of RAI in SCFs. To the author's knowledge, this is the first reported fully differential RAMP-based SCF design technique that can be extended to implement any generalized filter response. To demonstrate this RAMP-based generalized filter design methodology, we present design of a 3rd order low-pass filter (LPF) and a 2nd order band-pass filter (BPF) in 65nm CMOS technology.

The rest of this paper is organized as follows: Section II describes the design of proposed RAI and RAMP-based filter prototypes. The measurement results and quantitative comparison with state-of-the-art (SOTA) are explained in Section III, followed by conclusions in Section IV.

II. Proposed RAMP-based SCF design with Circuit Implementation

A. Proposed RAMP-based SC integrator (RAI)

Conventional SCFs [2] use the same or alternate phase clocking techniques using non-overlapping clock phases ϕ_1 and ϕ_2 (Fig. 2). These techniques need integrator output to be valid in both ϕ_1 and ϕ_2 phases. The RAMP-based integrators cannot be used to implement conventional SCF with outputs valid only during one clock phase. In [11], the RAMP-based filter re-samples the capacitor output in an invalid phase. The use of series switches for re-sampling makes precision higher-order filter design impractical. The single-ended RAMP-based integrator in [13] needs a feedback capacitor pair to operate differential circuits in a pseudo-pseudo-differential configuration. This loop filter operates at a much lower f_s (=5.8MSa/s) as the integrator is used twice to process each differential sample.

In this work, the RAMP is enabled for the high-frequency generalized SCF implementation. Fully differential signaling facilitates inversion by interchanging the positive and negative components of the differential signals. Based on this, we propose a differential RAI (Fig. 3(a)) that enables inverting and non-inverting input sampling in both ϕ_1 and ϕ_2 clock phases. This allows sampling of the valid RAI output by all subsequent stages in the same phase, enabling new RAI-based SCF. The symbol of the RAI is shown in Fig. 3(b). Here, the ϕ annotation at the input and output represent the sampling phase and the valid-output phase, respectively.

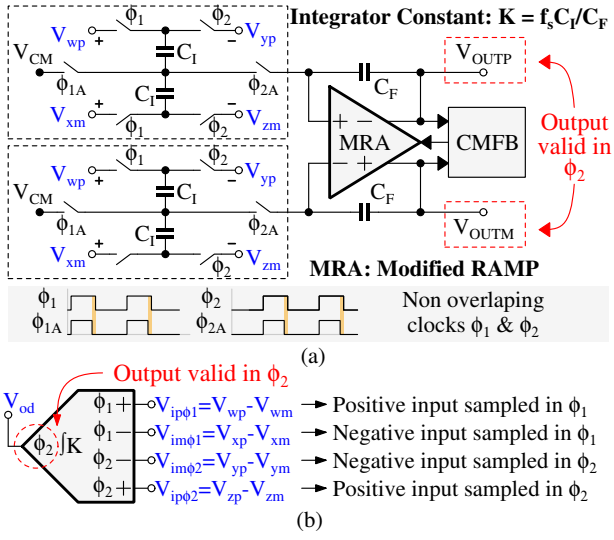


Fig. 3. Proposed (a) differential RAMP-based integrator (RAI) and (b) RAI symbol. The switches connected to virtual short nodes and V_{CM} are NMOS switches. The rest are CMOS pass-gate switches.

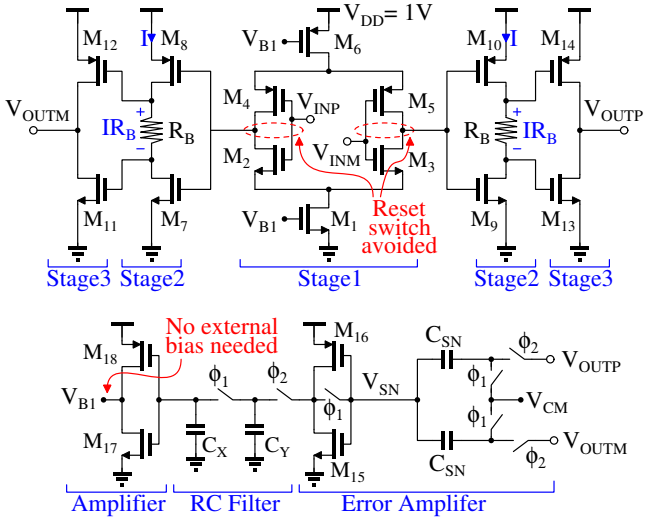


Fig. 4. Modified RAMP (MRA) (top) with CMFB circuit (bottom) in the proposed RAI without any reset switch or external current sources.

B. Modified RAMP (MRA) circuit

In [6], a reset switch is required to define RAMP input bias voltage during the sampling phase. The RAMP used in [8] avoids the reset switch but requires an external bias current generator. In the proposed RAI-based SCF, the RAMP output is sampled only during the valid phase, and voltages at the RAMP inputs are close to common-mode voltage (V_{CM}). As the modified RAMP (MRA) input in Fig. 3(a) is isolated during phase ϕ_1, the charge at the MRA input node remains unchanged due to continuous feedback through C_F. This ensures the RAMP input voltages are near V_{CM}; hence, the reset switch is not required.

Fig. 4 shows the transistor-level schematic of the MRA used in the RAI. During the phase ϕ_1 (Fig. 3), the input sampling capacitors (C_I) are isolated from the MRA. Input to the MRA is updated at the start of the amplification phase ϕ_2. For the MRA shown in Fig. 4, due to the high gain from input to stage-

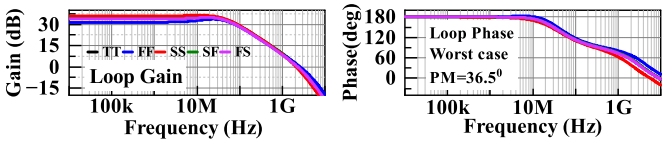


Fig. 5. Simulated MRA differential-mode loop gain (left) and phase (right) responses over process variations

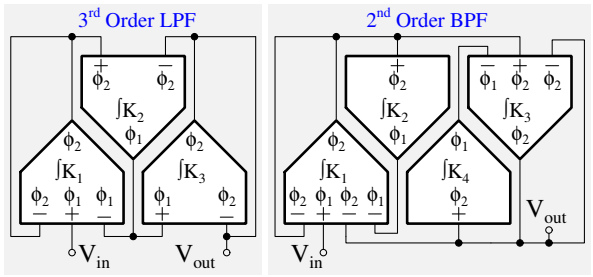


Fig. 6. RAI-based third-order LPF (left) and second-order BPF (right).

2 output, one of the transistors in stage-3 ($M_{11,14}/M_{12,13}$) turns ON with high overdrive voltage, providing a large output slewing current. This changes the MRA input through integrating/feedback capacitor C_F of the RAI (Fig. 3) and gives rise to oscillations. The oscillations are damped using an IR_B drop. As a result, the transistors $M_{11\text{-}14}$ get reduced overdrive in each successive oscillation, eventually entering the cut-off region to settle the output. As the transistors $M_{11\text{-}14}$ are OFF, the higher output resistance and the dominant load capacitance produce a stable single-pole equivalent response [7]. In phase ϕ_1, $M_{11\text{-}14}$ remain in OFF condition. Our proposed filter architecture ensures sampling only during the amplification phase (ϕ_2), and therefore, integrated output charge is retained on C_F.

The common-mode feedback (CMFB) circuit shown in Fig. 4 senses the output average on C_{SN} capacitors during the amplification phase (ϕ_2) only. The error between output average and V_{CM} is amplified and filtered using a switched-capacitor (RC) low-pass filter. Transistors $M_{17\text{-}18}$ improve common mode loop gain. The simulated MRA differential-mode (DM) loop gain plots in Fig. 5 illustrate stable operation over process variations with the worst-case phase margin of 36.5° in the SS corner. In typical corner Monte-Carlo mismatch simulations, the worst-case closed-loop differential and common-mode phase margins of 50^0 and 44^0 are obtained, respectively, showing robust stability over mismatches.

C. Filter prototypes using the proposed RAI

A 3-pole LPF and a 4-pole BPF (Fig. 6) are synthesized using the proposed RAI. Fig. 7 shows simulated process-insensitive LPF and BPF frequency responses. The MRAs and switch networks occupy less than 10% of the total area. The filters can further drive high load capacitance, eliminating the need for an on-chip buffer. In contrast, a conventional SCF with an f_s of 500MSa/s will require an opamp with 10GHz UGF ($20 \times f_s$) consuming significantly larger area and power.

III. Measurement Results

The LPF and BPF are fabricated in a 65nm CMOS technology, occupying an active area of 0.043mm^2 and 0.069mm^2,

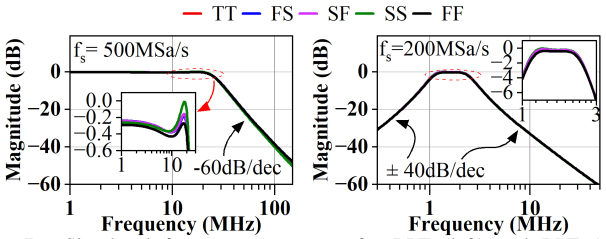
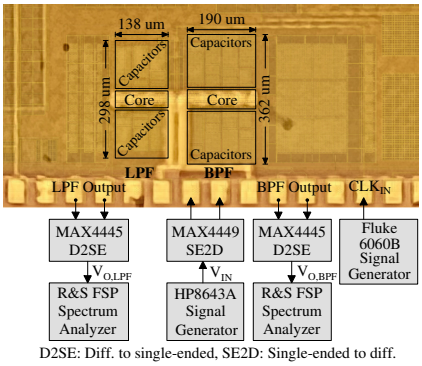


Fig. 7. Simulated frequency responses for LPF (left) and BPF (right) independent of process variations.



D2SE: Diff. to single-ended, SE2D: Single-ended to diff.

Fig. 8. Die photo with layout overlay and measurement setup. Fully symmetric layout done for precise differential signals.

while consuming 3.4mW and 4.36mW power from a 1V supply, respectively. The die micrograph and the test setup are shown in Fig. 8. The MAX4449/MAX4445 ICs on the PCB convert the single-ended/differential to differential/single-ended voltages for the interface between the filters and the test equipments. The measured LPF and BPF frequency responses are shown in Fig. 9 for various f_s, which closely match simulation results in Fig. 7. The LPF and BPF noise measurements are shown in Fig. 10, with the output integrated noise values of 357.56μ_{rms} (20MHz BW) and 164.2μV_{rms} (0.8MHz BW), respectively.

The LPF and BPF measured spectrum for single and two-tone inputs are shown in Fig. 11. For the LPF, an HD_3 of 47.7dBc at 200m$V_{pp,diff}$ input, and an IM_3 of 39.4dBc at two-tone 205m$V_{pp,diff}$ (each tone) input is observed. Similarly, for BPF, an IM_3 of 50dBc at two-tone 440m$V_{pp,diff}$ (each tone) input is observed. The fully symmetric filter layouts (Fig. 8) ensure suppressed even-order harmonics in post-layout simulations. The measured spectrum in Fig. 11(a)-(b) shows a second-order harmonic component with -60dBm power level

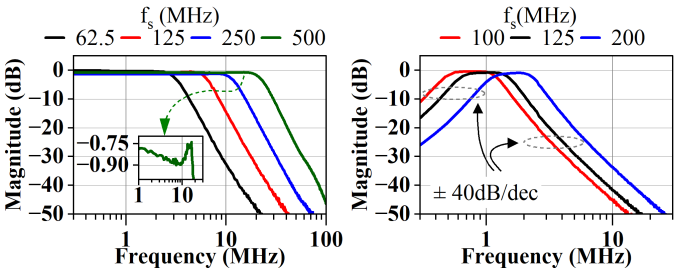


Fig. 9. Measured LPF (left) and BPF (right) frequency response.

TABLE I
COMPARISON WITH STATE-OF-THE-ART

	TCAS-I'18 [5]	VLSI'18 [14]*	ISSCC'22 [13]*	JSSC'21 [15]*	This Work	
Tech. (nm)	180	65	180	28	65	65
Supply (V)	1.8	1.2	1.1	1	1	1
Type	LPF (CS-IIR)	LPF	LPF	LPF	LPF	BPF
Order	4	1	3	2	3	2
f_s (MSa/s)	300	200	5.8	520	500	200
BW (MHz)	13.3	12.5	0.02	5	20	1.2 - 2
THD (dB)	-	-	-	-	45.4 @-8dBm	N.A.
IM_3 (dBc)	-	-	-	-	39.4 @-2dBm	50 @-2dBm
Power (mW)	4.3	-	0.073	8.99	3.4	4.36
Area (mm^2)	2.9	-	$\approx$ 0.009 †	-	0.043	0.069

*Loop filter in discrete-time delta-sigma modulator, †Estimated from the paper, N.A. : Not Applicable

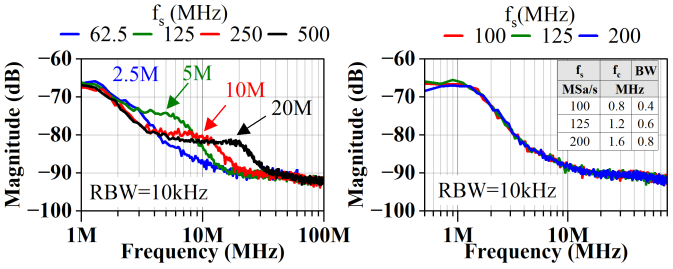


Fig. 10. Measured LPF and BPF noise plot.

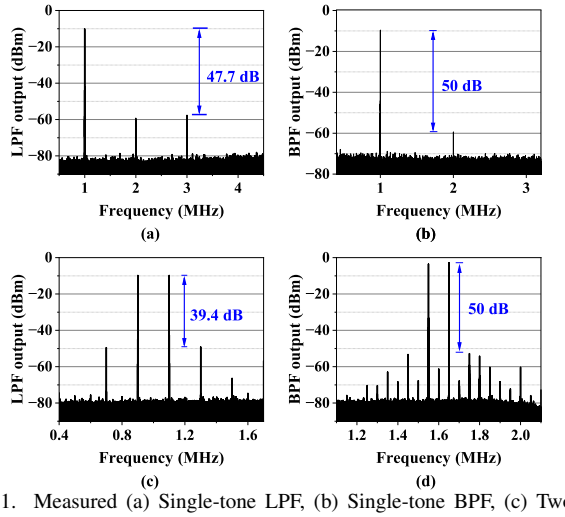


Fig. 11. Measured (a) Single-tone LPF, (b) Single-tone BPF, (c) Two-tone LPF, and (d) Two-tone BPF spectrum

traced back to a mismatch in the interface circuit on the PCB. The filter performances are tabulated and compared with the SOTA filters in Table I. The RAMP-based LPF achieves a high bandwidth of 20MHz with better power efficiency as compared to SOTA SCFs with similar f_s. The THD and IM_3 for SCFs are unavailable in recent literature and are not reported in the table.

IV. CONCLUSION

A RAMP-based SCF design methodology is presented to implement any precision generalized filter response. A differential RAI is proposed to replace conventional opamp with RAMP to achieve higher SCF bandwidths with good area and power efficiency. The prototype RAMP-based LPF and BPF designs are presented. The LPF achieves 20MHz bandwidth with better area and power efficiency than the SOTA SCF operating at similar f_s. As the proposed filters are constructed using MRA, the overall performance can be improved with technology scaling. As per the RAMP survey [9], this is the first fully differential RAMP-based SCF design that enables generalized high-frequency filter implementations.

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